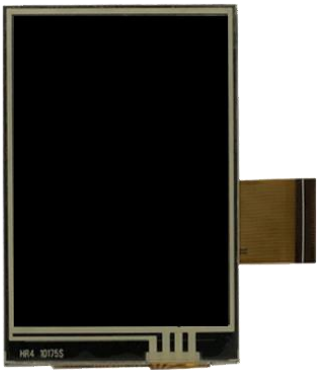
DisplayModule



# DM-TFT26-443

## 2.6" 320x432 TRANSFLECTIVE DISPLAY PANEL WITH RESISTIVE TOUCH– MCU/SPI/RGB

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# 1 Revision History

| Date | Changes |
|---|---|
| 2022-06-29 | First release |

# 2 Main Features

| Item | Specification | Unit |
|---|---|---|
| Size | 2.6 | Inch |
| Resolution | 320(RGB) x 432 | pixel |
| Module Dimension | 46.76 x 65.85 x3.91 | mm |
| Display area | 39.84(H)*53.78（V) | mm |
| Pixel pitch | 0.1245(H)*0.1245(V) | mm |
| TFT Controller IC | ILI9488 | - |
| Interface | 8/9/16/18Bit MCU Interface<br>3/4SPI+16/18Bit RGB Interface<br>3-line/4-line Serial Interface | - |
| Display Color | 65K/262K/16.7M | colors |
| View Direction | ALL | O'clock |
| Display mode | Transflective /Normally Black | - |
| Weight | 20 | g |
| Operating temperature | -30~+85 | ℃ |
| Storage temperature | -40~+85 | ℃ |

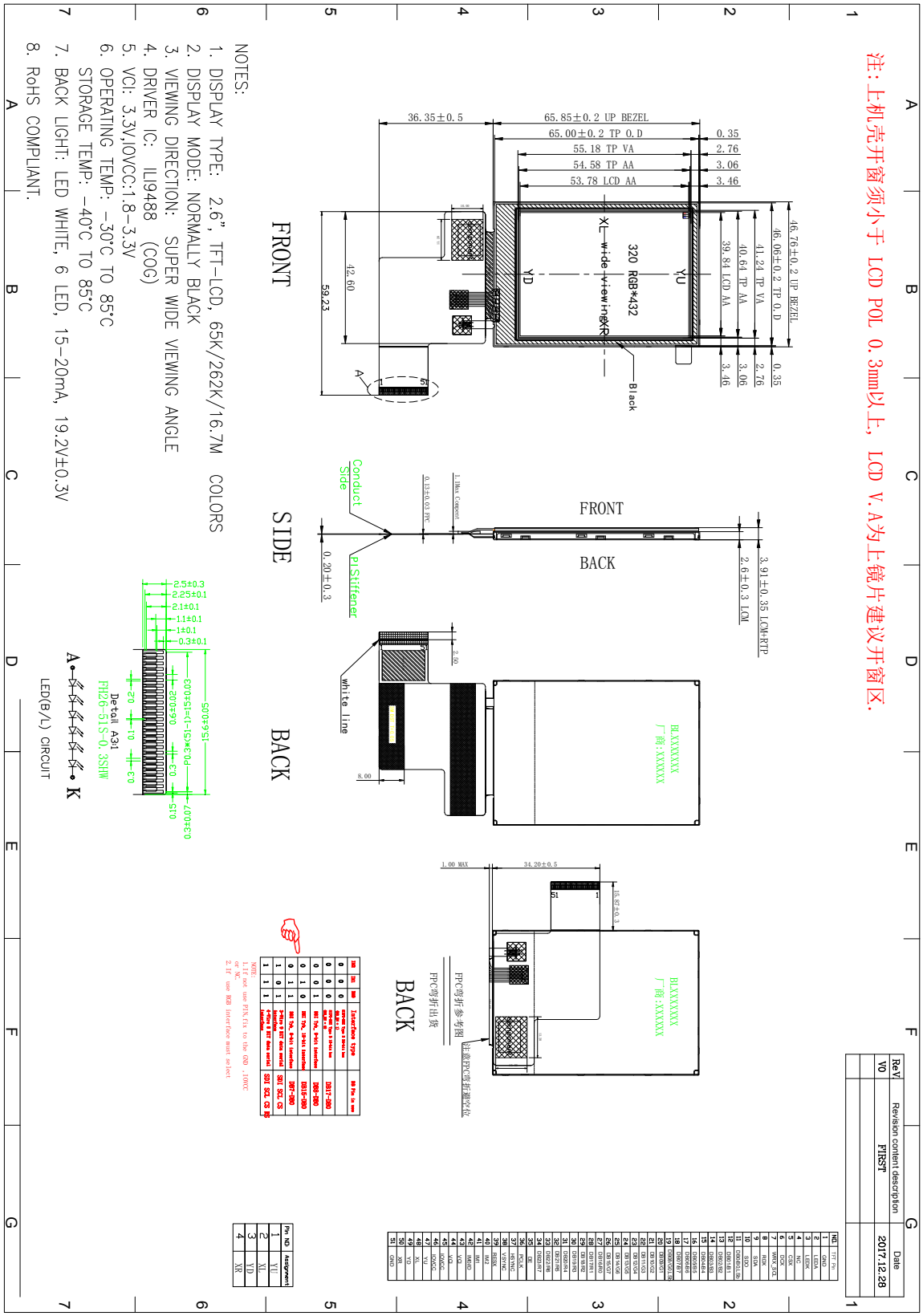
# 3 Pin Description

| No. | Symbol | Description |
|---|---|---|
| 1 | GND | Ground. |
| 2 | LEDA | Cathode pin of backlight. |
| 3 | LEDK | Cathode pin OF backlight. |
| 4 | NC | -- |
| 5 | CSX | Chip select input pin ("Low" enable).<br>fix this pin at VCI or GND when not in use. |
| 6 | DCX | Display data/command selection pin |
| 7 | WR(SPI-SCL) | DBI Type B: WRX pin, serves as a write signal<br>DBI Type C: SCL pin as Serial Clock when operates in the seri al |

| | | |
|---|---|---|
| | | interface |
| 8 | RDX | Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use. |
| 9 | SDA | Serial input signal.The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND. |
| 10 | SDO | Serial data output pin in serial bus system interface.<br>If not used, please open this pin. |
| 11-34 | DB0-DB23 | 24-bit parallel bi-directional data bus for MCU system and RGB interface mode .<br>Fix to GND level when not in use. |
| 35 | DE | Data enable signal for RGB interface operation.<br>fix this pin at VCI or GND when not in use. |
| 36 | PCLK | Dot clock signal for RGB interface operation<br>Fix this pin at VCI or GND when not in use. |
| 37 | HSYNC | Line synchronizing signal for RGB interface operation.<br>fix this pin at VCI or GND when not in use. |
| 38 | VSYNC | Frame synchronizing signal for RGB interface operation.<br>fix this pin at VCI or GND when not in use. |
| 39 | RESX | This signal will reset the device and must be applied to properly initialize the chip. |
| 40 | IM2 | MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND. |
| 41 | IM1 | |
| 42 | IM0 | |
| 43 | VCI | Supply voltage(3.3V) |
| 44 | VCI | |
| 45 | IOVCC | Supply voltage For IO(1.8-3.3V) |
| 46 | IOVCC | |
| 47 | YU | Touch panel Top Film Terminal |
| 48 | XL | Touch panel LEFT Glass Terminal |
| 49 | YD | Touch panel Bottom Film Terminal |

| | | |
|---|---|---|
| 50 | XR | Touch panel Right Glass Terminal |
| 51 | GND | Ground |

# 4 Mechanical Drawing



# 5 Electrical Characteristics

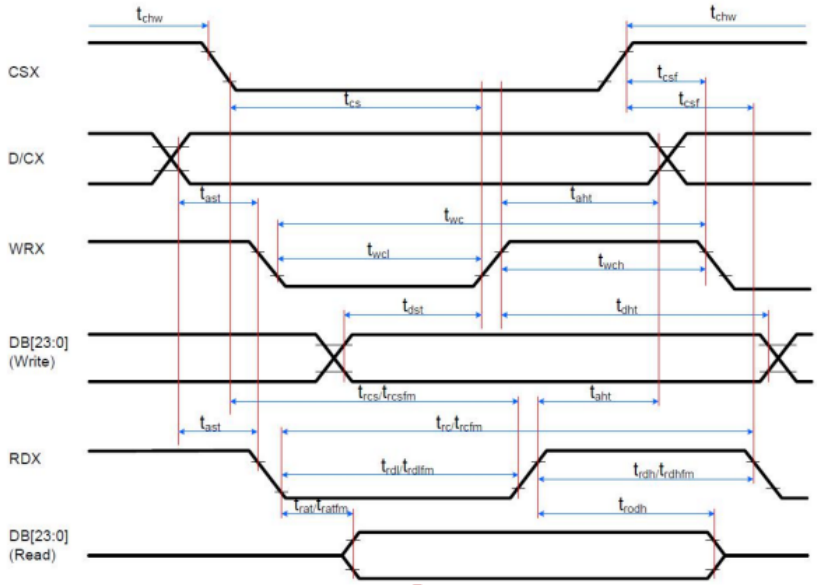
| Item | | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Digital Supply Voltage | Absolute Maximum Rating | VCI | -0.3 | | 3.3 | V |
| Digital interface supple Voltage | Absolute Maximum Rating | IOVCC | -0.3 | | 3.3 | V |
| Operating Temperature | Absolute Maximum Rating | TOP | -30 | | +85 | ℃ |
| Storage Temperature | Absolute Maximum Rating | TST | -40 | | +85 | ℃ |
| Digital Supply Voltage | | VCI | 2.5 | 2.8 | 3.3 | V |
| Digital interface supple Voltage | | IOVCC | 1.65 | 1.8 | 3.3 | V |
| Normal mode Current | | IDD | -- | 14 | -- | mA |
| Level input voltage | | $V_{IH}$ | 0.7*IOVCC | -- | IOVCC | V |
| | | $V_{IL}$ | -0.3 | -- | 0.3*IOVCC | V |
| Level output voltage | | $V_{OH}$ | 0.8*IOVCC | -- | IOVCC | V |
| | | $V_{OL}$ | GND | -- | 0.2*IOVCC | V |

# 6 Optical Characteristics

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Forward Current | $I_F$ | 15 | 20 | - | mA |
| Forward Voltage | $V_F$ | -- | 19.2 | - | V |
| LCM Luminance | LV | 360 | 425 | - | cd/m2 |
| LED life time | $H_r$ | 50000 | -- | - | Hour |
| Uniformity | Avg | 80 | -- | - | % |

# 7 AC Characteristics

## 7.1 DBI Type B Timing Characteristics



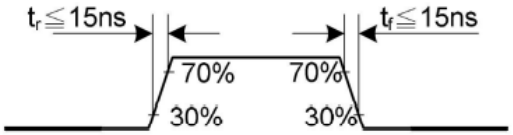

| | Symbol | Parameter | Spec | | Unit. | Description |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| DCX | $t_{ast}$ | Address setup time | 0 | -- | ms | |
| | $t_{hat}$ | Address hold time (Write/Read) | 0 | -- | us | |
| CSX | $t_{chw}$ | CSX "H" pulse width | 0 | -- | ns | |
| | $t_{cs}$ | Chip Select setup time (Write) | 15 | -- | % | |
| | $t_{rcs}$ | Chip Select setup time (Read ID) | 45 | -- | ns | |
| | $t_{rcsfm}$ | Chip Select setup time (Read FM) | 355 | -- | ns | |
| | $t_{csf}$ | Chip Select Wait time (Write/Read) | 0 | -- | ns | |
| WRX | $t_{wc}$ | Write cycle | 40 | -- | ns | |
| | $t_{wrh}$ | Write Control pulse H duration | 15 | -- | ns | |
| | $t_{wrl}$ | Write Control pulse L duration | 15 | -- | ns | |
| RDX(FM) | $t_{rcfm}$ | Read Cycle (FM) | 450 | -- | ns | When read from Frame Memory |
| | $t_{rdhfm}$ | Read Control H duration (FM) | 90 | -- | ns | |
| | $t_{rdlfm}$ | Read Control L duration (FM) | 355 | -- | ns | |
| RDX(ID) | $t_{rc}$ | Read cycle (ID) | 160 | -- | ns | When read ID data |

| | | | | | | |
|---|---|---|---|---|---|---|
| | $t_{rdh}$ | Read Control pulse H duration | 90 | -- | ns | |
| | $t_{rdl}$ | Read Control pulse L duration | 45 | -- | ns | |
| DB[23:0], DB[17:0], DB[15:0], DB [8:0], DB [7:0] | $t_{dst}$ | Write data setup time | 10 | -- | ns | For maximum, CL=30pF<br>For minimum, CL=8pF |
| | $t_{dht}$ | Write data hold time | 10 | -- | ns | |
| | $t_{rat}$ | Read access time | -- | 40 | ns | |
| | $t_{ratfm}$ | Read access time | -- | 340 | ns | |
| | $t_{rod}$ | Read output disable time | 20 | 80 | ns | |

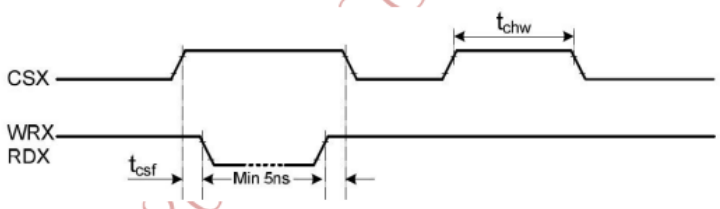
*Note: 1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V*

*2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.*

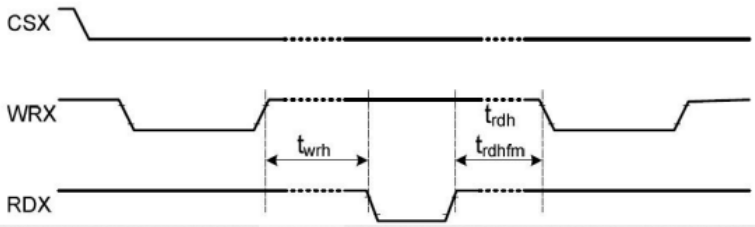
*3. Input signal rising time and falling time.:*



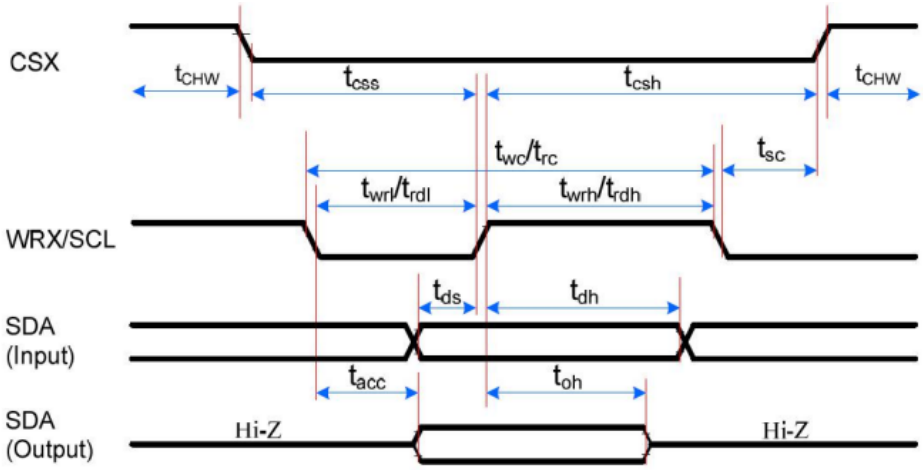

*4.The CSX timing:*




*5. The Write to Read or the Read to Write timing:*

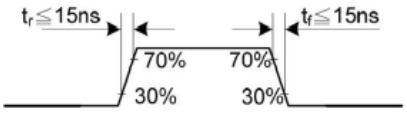


## 7.2 DBI Type C Option 1 (3-Line SPI System) Timing Characteristics

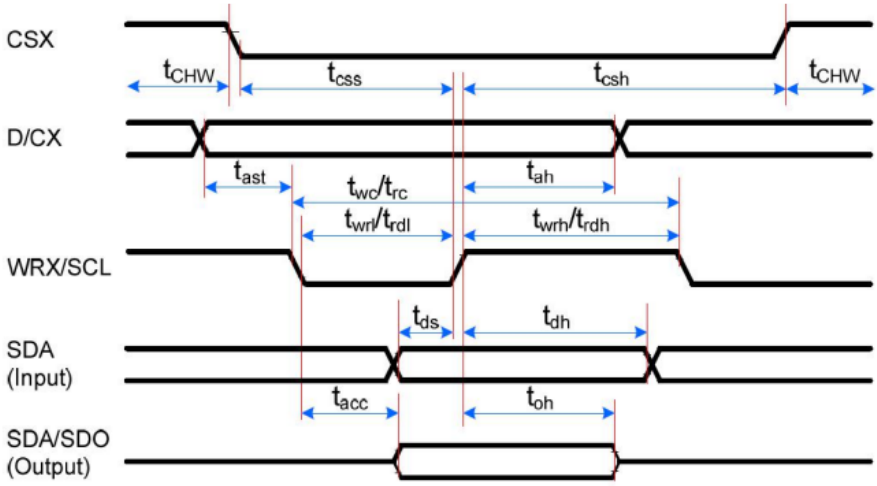



| Signal | Symbol | Parameter | Spec | | Unit. | Description |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| CSX | $t_{sc}$ | SCL-CSX | 15 | -- | ns | |
| | $t_{chw}$ | CSX H Pulse Width | 40 | -- | ns | |
| | $t_{css}$ | Chip select time (Write) | 60 | -- | ns | |
| | $t_{csh}$ | Chip select hold time (Read) | 65 | | | |
| SCL | $t_{wc}$ | Serial clock cycle (Write) | 66 | -- | ns | |
| | $t_{wrhf}$ | SCL H pulse width (Write) | 15 | -- | ns | |
| | $t_{wrl}$ | SCL L pulse width (Write) | 15 | -- | ns | |
| | $t_{rc}$ | Serial clock cycle (Read) | 150 | -- | ns | |
| | $t_{rdh}$ | SCL H pulse width (Read) | 60 | -- | ns | |
| | $t_{rdl}$ | SCL L pulse width (Read) | 60 | -- | ns | |
| SDA (Input) | $t_{ds}$ | Read cycle (ID) | 10 | -- | ns | |
| | $t_{dh}$ | Read Control pulse H duration | 10 | -- | ns | |
| SDA/SDO (Output) | $t_{acc}$ | Write data setup time | 10 | 50 | ns | For maximum CL=30pF |
| | $t_{od}$ | Write data hold time | 15 | 50 | ns | |

*NOTES: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns*



## 7.3 DBI Type C Option 3 (4-Line SPI System) Timing Characteristic

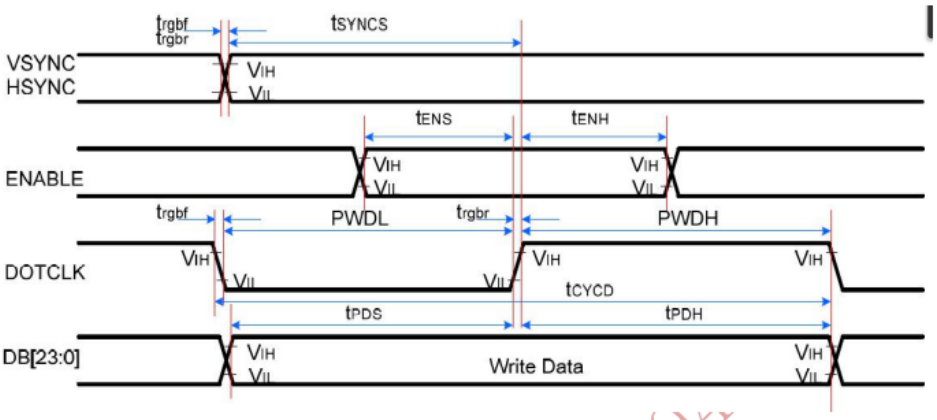



| Signal | Symbol | Parameter | Spec | | Unit. | Description |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| CSX | $t_{css}$ | Chip select time (Write) | 15 | -- | ns | |
| | $t_{csh}$ | Chip select hold time (Read) | 15 | -- | ns | |
| | $t_{chw}$ | CS H pulse width | 40 | -- | ns | |
| SCL | $t_{wc}$ | Serial clock cycle (Write) | 50 | -- | ns | |
| | $t_{wrhf}$ | SCL H pulse width (Write) | 10 | -- | ns | |
| | $t_{wrl}$ | SCL L pulse width (Write) | 10 | -- | ns | |
| | $t_{rc}$ | Serial clock cycle (Read) | 150 | -- | ns | |
| | $t_{rdh}$ | SCL H pulse width (Read) | 60 | -- | ns | |
| | $t_{rdl}$ | SCL L pulse width (Read) | 60 | -- | ns | |
| D/CX | $t_{as}$ | D/CX setup time | 10 | -- | ns | |
| | $t_{ah}$ | D/CX hold time (Write/Read) | 10 | -- | ns | |
| SDA (Input) | $t_{ds}$ | Read cycle (ID) | 10 | -- | ns | |
| | $t_{dh}$ | Read Control pulse H duration | 10 | -- | ns | |
| SDA/SDO (Output) | $t_{acc}$ | Write data setup time | 10 | 50 | ns | For maximum CL=30pF |
| | $t_{od}$ | Write data hold time | 15 | 50 | ns | For minimum CL=8pF |

1. *Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.*

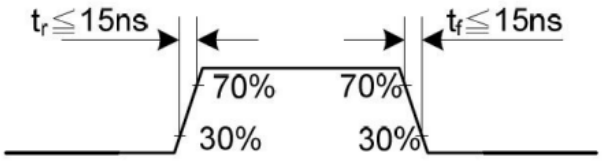
2. *Does not include signal rising and falling times.*

## 7.4 DPI (Display Parallel 16-/18-/24-bit interface) Timing Characteristics




| Signal | Symbol | Parameter | Spec | | Unit. | Description |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| VSYNC/ HSYNC | $t_{SYNCS}$ | VSYNC/HSYNC setup time | 15 | -- | ns | 16-/18-/24-bit bus RGB interface mode |
| | $t_{SYNCH}$ | VSYNC/HSYNC hold time | 15 | -- | ns | |
| ENABLE | $t_{ENS}$ | ENABLE setup time | 15 | -- | ns | |
| | $t_{ENH}$ | ENABLE hold time | 15 | -- | ns | |
| DB[23:0] | $t_{POS}$ | Data setup time | 15 | -- | ns | |
| | $t_{POH}$ | Data hold time | 15 | -- | ns | |
| DOTCLK | PWDH | DOTCLK high-level period | 20 | -- | ns | |
| | PWDL | DOTCLK low-level period | 20 | -- | ns | |
| | $t_{CYCD}$ | DOTCLK cycle time | 50 | -- | ns | |
| | $t_{rgbr}$,$t_{rgbr}$ | DOTCLK,HSYNC,VSYNC rise/fall time | -- | 15 | ns | |

*NOTES: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns*



## 7.5 Reset input Timing

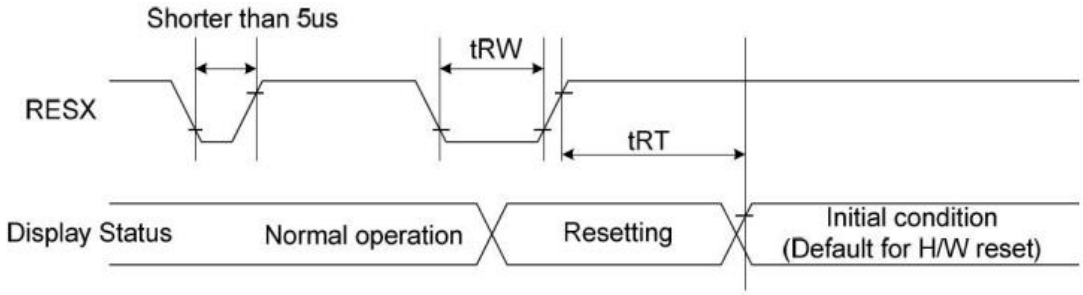



**Table 39: Reset Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | tRW | Reset pulse duration | 10 | | uS |
| | tRT | Reset cancel | | 5 (note 1,5) | mS |
| | | | | 120 (note 1,6,7) | mS |

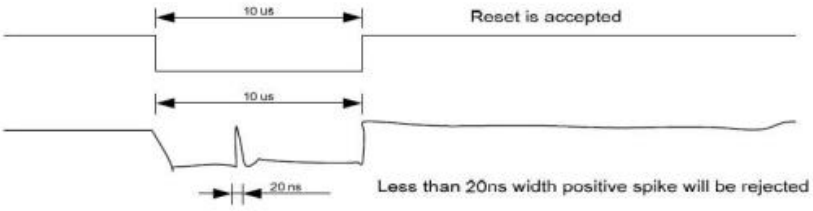
**Notes:**

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

**Table 40: Reset Description**

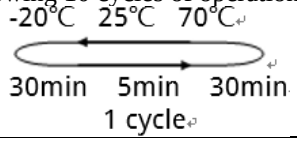
| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:




5. When Reset is applied during the Sleep In Mode.
6. When Reset is applied during the Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. The Sleep Out command also cannot be sent in 120msec.

# 8 Reliability

| Test Item | Content of Test | Test Condition | Note |
|---|---|---|---|
| High Temperature Storage | Endurance test applying the high storage temperature for a long time. | 80℃<br>200hrs | 2 |
| Low Temperature Storage | Endurance test applying the high storage temperature for a long time. | -30℃<br>200hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time. | 70℃<br>200hrs | - |
| Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time. | -20℃<br>200hrs | 1 |
| High Temperature/ Humidity Operation | The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature. | 60℃,90%RH<br>96hrs | 1,2 |
| Thermal Shock Resistance | The sample should be allowed stand the following 10 cycles of operation.<br>  <br> | -20℃/70℃<br>10 cycles | - |
| Vibration Test | Endurance test applying the vibration during transportation and using. | Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes. | 3 |
| Static Electricity Test | Endurance test apply the electric stress to the terminal. | VS=800V, RS=1.5kΩ, CS=100pF, 1 time. | - |

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

# 9 Warranty and Conditions

http://www.displaymodule.com/pages/faq