DisplayModule

DM-TFT26-382

2.6" IPS 240x320 DISPLAY PANEL WITH CAPACITIVE TOUCH –SPI ,MCU, RGB

Contents

1 Revision History

Date	Changes
2018-11-19	First release

2 Main Features

Item	Specification	Unit
Size	2.6	Inch
Resolution	240(RGB) x 320	pixel
Module Dimension	46.0 x 64.0 x 4.03	mm
Display area	39.6 x 52.8	mm
Pixel pitch	0.165 x 0.165	mm
TFT Controller IC	ST7789V	-
CTP Driver IC	FT6336G	-
Interface	8/9/16/18 Bit MCU 3/4SPI+16/18bit RGB 3-line/4-line Serial	-
Display Color	65K/262K	colors
View Direction	ALL	O'clock
Touch mode	Single point and Gestures	-
Display mode	Transmissive /LED Normally Black	-
Weight	TBD	g

3 Pin Description

3.1 TFT

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>GND</td><td>Ground.</td></tr>
<tr><td>2</td><td>VCI</td><td>Supply voltage(3.3V).</td></tr>
<tr><td>3</td><td>VCI</td><td>Supply voltage(3.3V).</td></tr>
<tr><td>4</td><td>IM2</td><td rowspan="3">
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>DB pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Type_8bit interface</td><td>DB7-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Type_16bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Type_9bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Type_18bit interface</td><td>DB17-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-wire 9Bit data serial</td><td>SDA SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4-wire 8Bit data serial</td><td>DSA SCL CS RS</td></tr>
</table>
Interface selection</td></tr>
<tr><td>5</td><td>IM1</td></tr>
<tr><td>6</td><td>IM0</td></tr>
<tr><td>7</td><td>RESET</td><td>This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active.</td></tr>
<tr><td>8</td><td>CS</td><td>System bus select signal. Low: Select (Accessible). High: Not select (Inaccessible).</td></tr>
<tr><td>9</td><td>RS(SPI-SCL)</td><td>(D/CX): This pin is used to select “Data or Command” in the parallel interface. When DCX = 1, data is selected. When DCX = 0, command is selected. (SCL): This pin is used as the serial interface clock in 3wire 9bit/4wire 8bit serial data interface. If not used, this pin should be connected to VDDI</td></tr>
<tr><td>10</td><td>WR(SPI-RS)</td><td>(WRX) 8080/8080 Ⅰ Ⅱ system: Serves as a write signal and writes data at the rising edge. (D/CX) 4line system: Serves as the selector of command or parameter. Fix to VDDI level when not in use.</td></tr>
<tr><td>11</td><td>RD</td><td>Read strobe signal. Data are read when RDX is low. If not used, please connect this pin to VCI.</td></tr>
<tr><td>12</td><td>VSYNC</td><td>Frame synchronous signal. Low active. Connect to I GND when DPI is not selected.</td></tr>
<tr><td>13</td><td>HSYNC</td><td>Line synchronous signal. Low active. Connect to GND when DPI is not selected.</td></tr>
<tr><td>14</td><td>ENABLE</td><td>Data enable signal in DPI operation. Low: Select (Accessible) High: Not select (Inaccessible) Connect to GND when DPI is not selected.</td></tr>
<tr><td>15</td><td>DOTCLK</td><td>Pixel clock signal. The data input timing is set on the rising edge. Connect to GND when DPI is not selected.</td></tr>
<tr><td>16</td><td>SDA</td><td>Serial data input/output pin in DBI Type C operation.</td></tr>
</table>

17-34	DB0~DB17	Data bus. In 16 Bit RGB Interface mode, use DB1-DB11,DB13-DB17 In 18 Bit RGB Interface mode, use DB0-DB17 Connect to GND when is not used.
35	SDO	This pin is enabled when SDOE=1 and DBI Type C is used. With this setting, SDA can be used as an input pin and SDO pin can be used as an output pin without bidirectional bus to exe cute serial communication. If not used please open.
36	LEDA	Anode pin of backlight
37-42	LEDK1-6	Cathode pin of backlight
43	XR	Touch panel Right Glass Terminal
44	YU	Touch panel Top Film Terminal
45	XL	Touch panel LIFT Glass Terminal
46	YD	Touch panel Bottom Film Terminal
47-50	GND	Ground

3.2 CTP

No.	Symbol	Description
1	GND	Ground
2	VDDIO	I/O power supply voltage
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

4 Mechanical Drawing

NO.	Pin Name
1	GND
2	VCI
3	VCI
4	TM2
5	IM1
6	IM0
7	RESET
8	CS
9	RS (SCL)
10	WR (D/C)
11	RD
12	VSYNC
13	HSYNC
14	ENABLE
15	DOTCLK
16	SDA
17	DB0
18	DB01
19	DB02
20	DB03
21	DB04
22	DB05
23	DB06
24	DB07
25	DB08
26	DB09
27	DB10
28	DB11
29	DB12
30	DB13
31	DB14
32	DB15
33	DB16
34	DB17
35	SDO
36	LEDA
37	LEDK1
38	LEDK2
39	LEDK3
40	LEDK4
41	LEDK5
42	LEDK6
43	XR
44	YU
45	XL
46	YD
47	GND
48	GND
49	GND
50	GND

NC	DB1	DB0	Interface Type	DB Pin in use
0	0	0	16\ Sys_ 18-bit interface	DB7-DB0
0	0	1	8BI Sys_ 16-bit interface	DB15-DB8
0	1	0	8BI Sys_ 9-bit interface	DB8-DB0
0	1	1	8BI Sys_ 18-bit interface	DB17-DB0
1	0	1	4-Wire 8 BIT data serial interface	SDA SCL CS
1	1	0	3-Wire 8 BIT data serial interface	SDA SCL CS RS

5 Electrical Characteristics

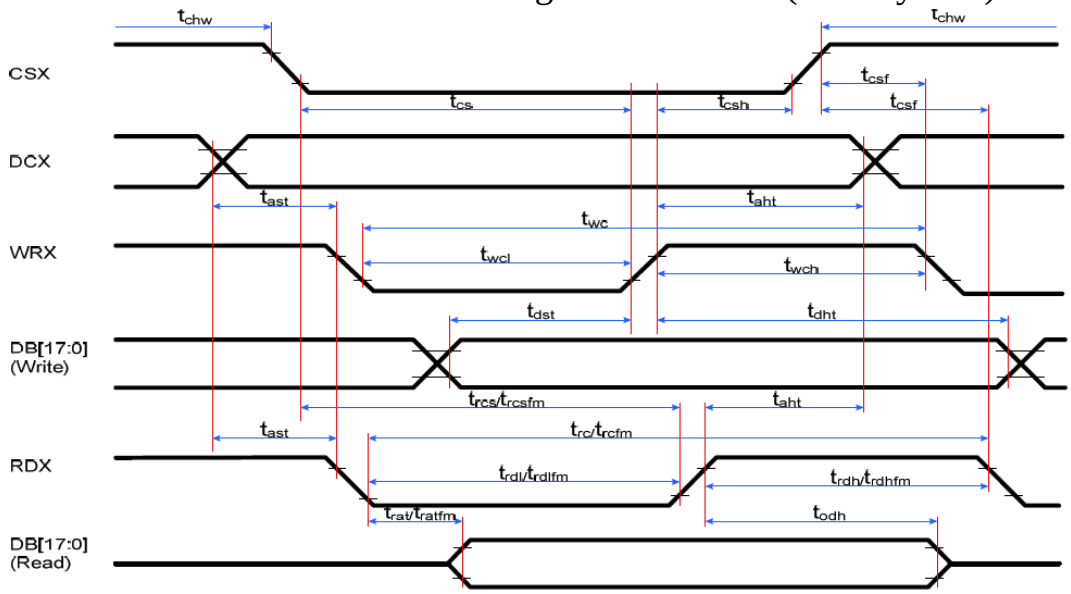
Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VCI		2.5	3.3	3.6	V
Normal mode Current	IDD		-	10	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃
LED Forward Current	If		90	120	-	mA
LED Forward Voltage	Vf		-	3.2	-	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	ΘU	-	80	-	deg
View Angles Bottom	ΘD	-	80	-	deg
View Angles Right	ΘR	-	80	-	deg
View Angles Left	ΘL	-	80	-	deg
Response Time	Tr +Tf		35	50	ms
Contrast Ratio	CR	400	500	-	--
LCM Luminance	Lv	300	350	-	cd/m^2

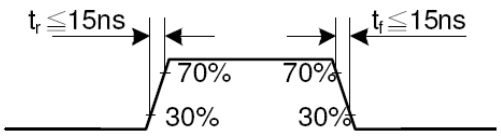
7 AC Characteristics

7.1 Parallel 8/9/18bit interface Timing Characteristics(8080 system)

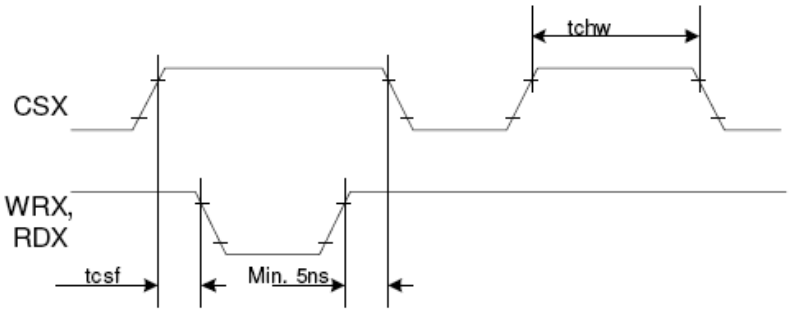


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, GND=0V

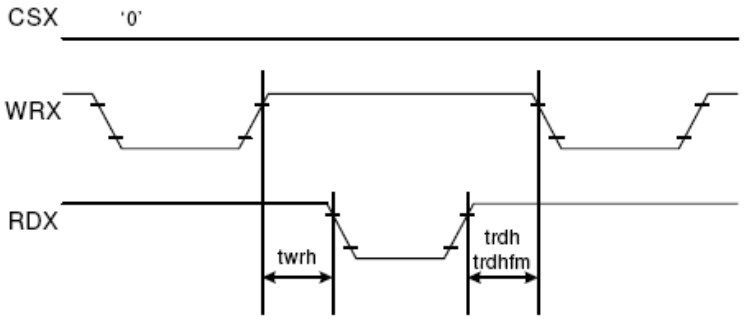


CSX timings :



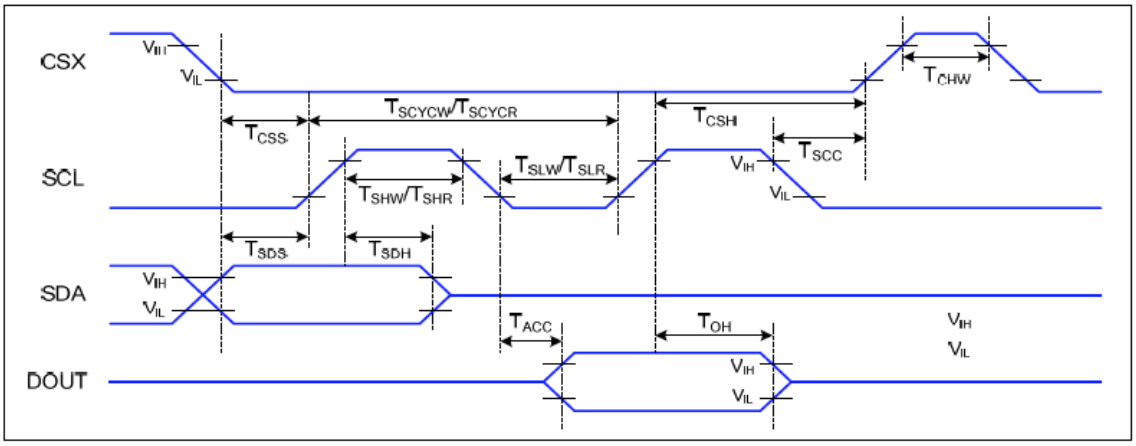
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

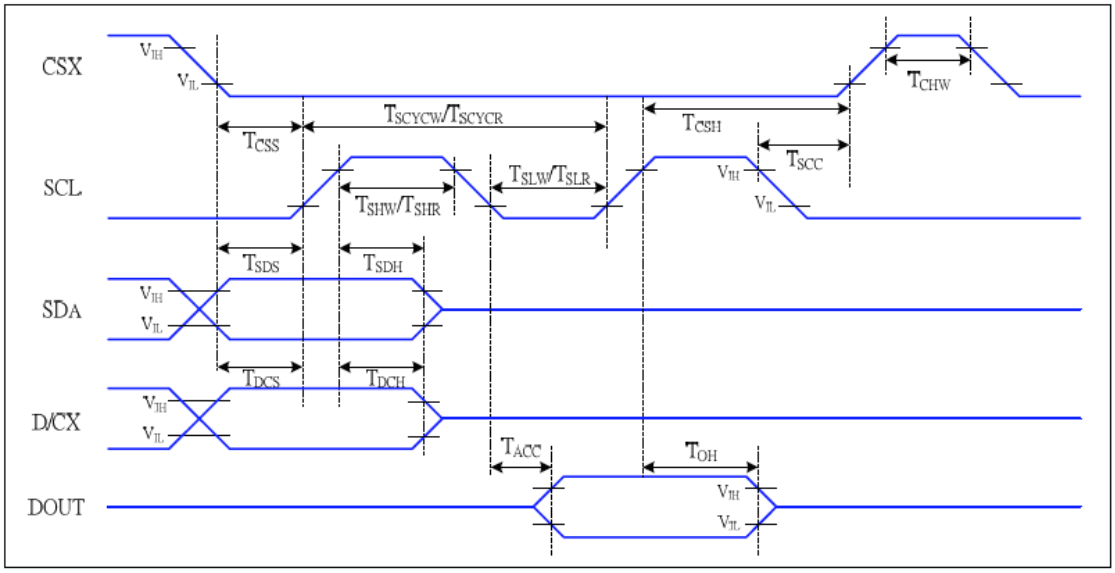
7.2 Serial Interface (3-line SPI system) Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

7.3 Serial interface (4-line SPI system) Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

7.4 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

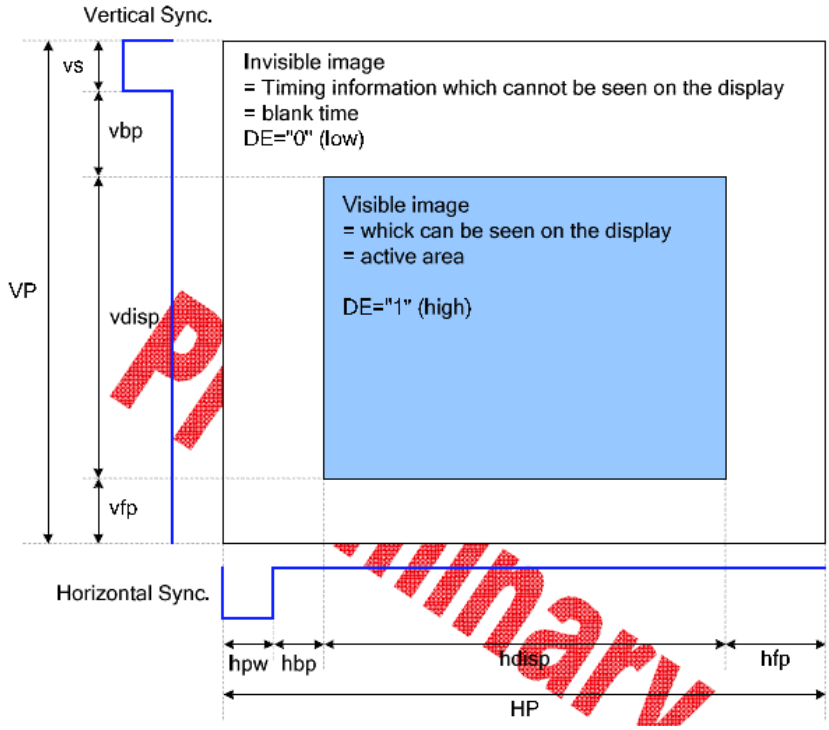


Figure 24 DRAM Access Area by RGB Interface

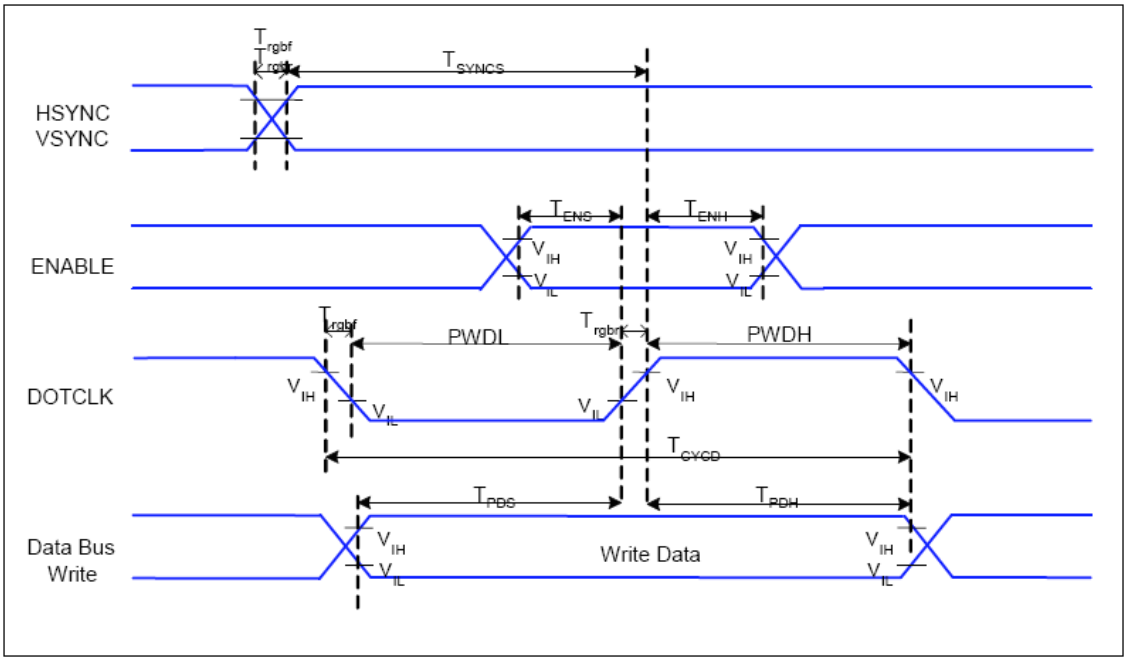
Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	10	hpw+hbp=31	Clock
Horizontal Sync. Back Porch	hbp	4	10		Clock
Horizontal Sync. Front Porch	hfp	2	38	-	Clock
Vertical Sync. Width	vs	1	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	1	4		Line
Vertical Sync. Front Porch	vfp	1	8	-	Line

Note:

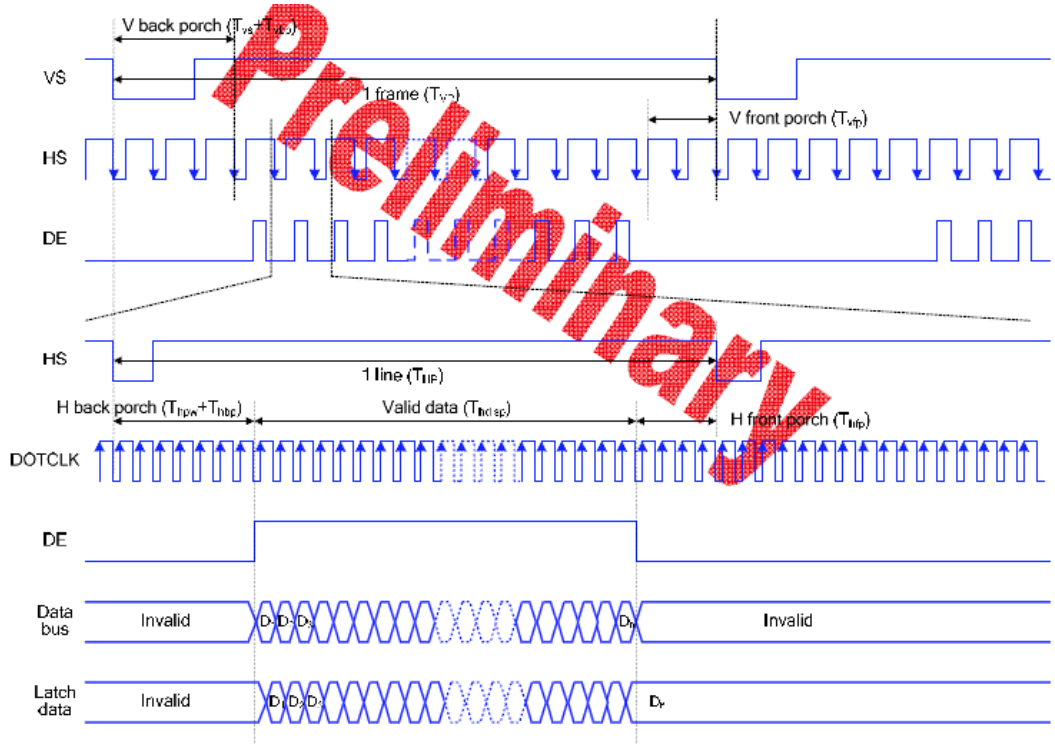
1. *Typical value are related to the setting of dot clock is 7MHz and frame rate is 70Hz..*
2. *If the setting of hpw is 10 dot clocks and hbp is 10 dot clocks, the setting of HBP in command B1h is 20 dot clocks*
3. *In with ram mode, hpw+hbp+hfp≧22*

7.5 RGB Interface Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

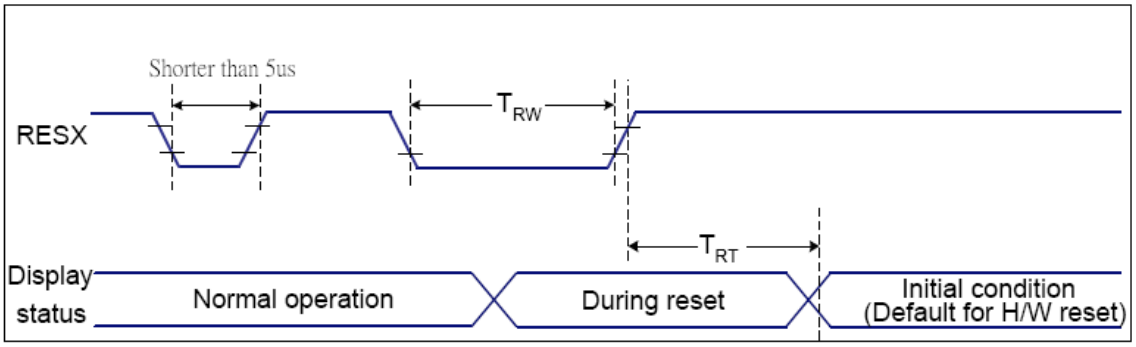
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 25 Timing Chart of Signals in RGB Interface DE Mode

7.6 Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

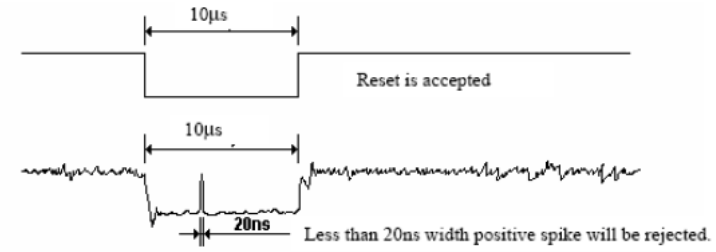
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 CTP Specification

8.1 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		2.8	3.3	3.6	V
Normal mode Current			-	4	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃

NOTES:

If used beyond the absolute maximum ratings, FT6336G may be permanently damaged. It is strongly recommanded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device

8.2 AC Characteristics

Item	Condition	Min	Typ	Max	Unit
OSC clock	AVDD=2.8V;Ta=25° C	34.65	35	35.35	MHz

AC characteristics of Oscillators

I2C interface:

The I2C is always configured in the Slave mode, The data transfer format is shown in Figure4-1:

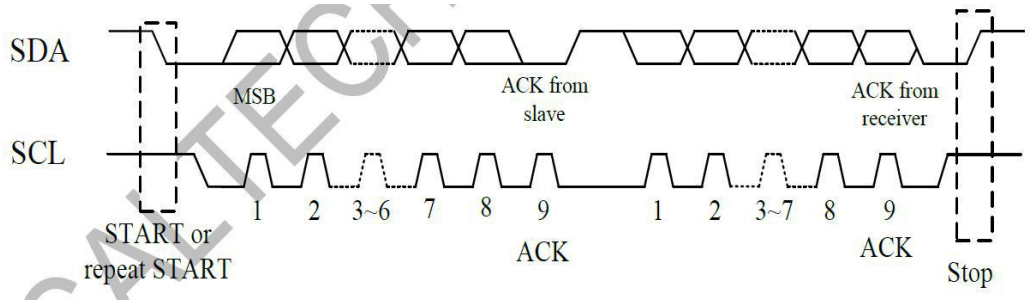


Figure 4-1 I2C Serial Data Transfer Format

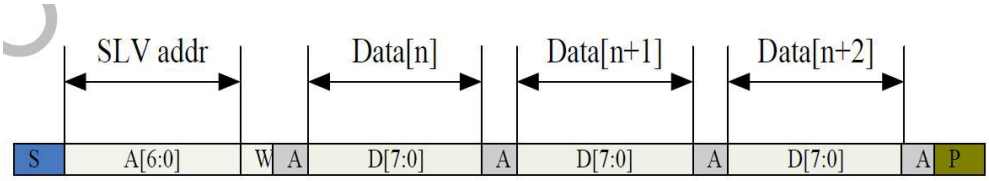


Figure 4-2 I2C master write, slave read

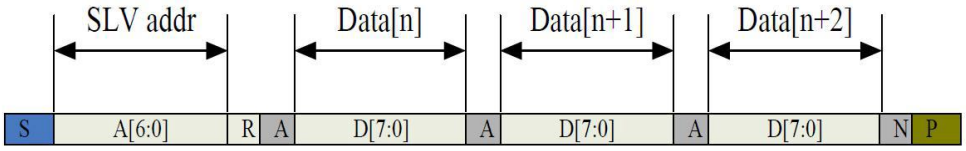


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

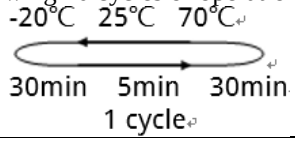
Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq