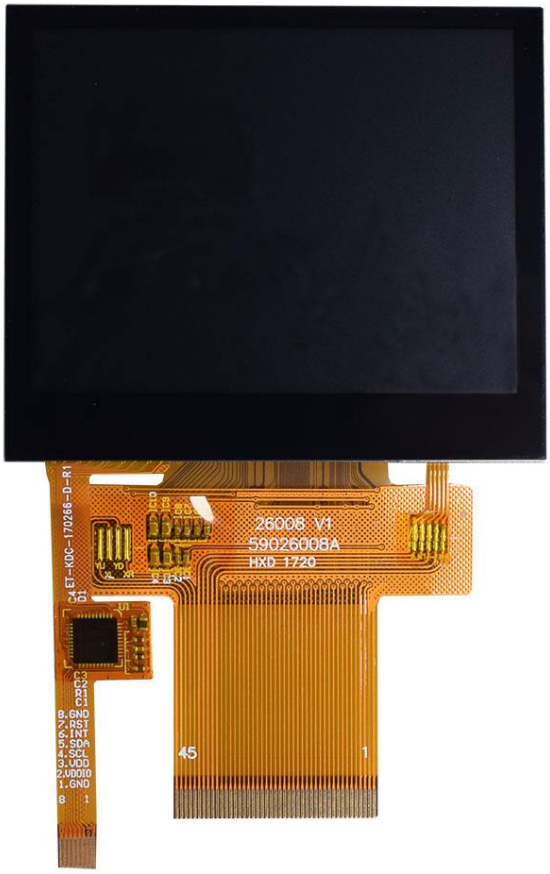
DisplayModule



DM-TFT26-381

2.6" 320x240 DISPLAY PANEL WITH CAPACITIVE TOUCH – SPI ,MCU, RGB

Contents

1 Revision History

Date	Changes
2018-11-16	First release

2 Main Features

Item	Specification	Unit
Size	2.6	Inch
Resolution	320(RGB) x 240	pixel
Module Dimension	60.3 x 51.15 x 4.05	mm
Display area	52.8 x 39.6	mm
Pixel pitch	0.165 x 0.165	mm
TFT Controller IC	ILI9342	-
CTP Driver IC	FT6336G	-
Interface	8/9/16/18 Bit MCU 3/4SPI+16/18bit RGB 3-line/4-line Serial	-
Display Color	65K/262K	colors
View Direction	6	O'clock
Touch mode	Single point and Gestures	-
Display mode	Transmissive /LED Normally white	-
Weight	TBD	g

3 Pin Description

3.1 TFT

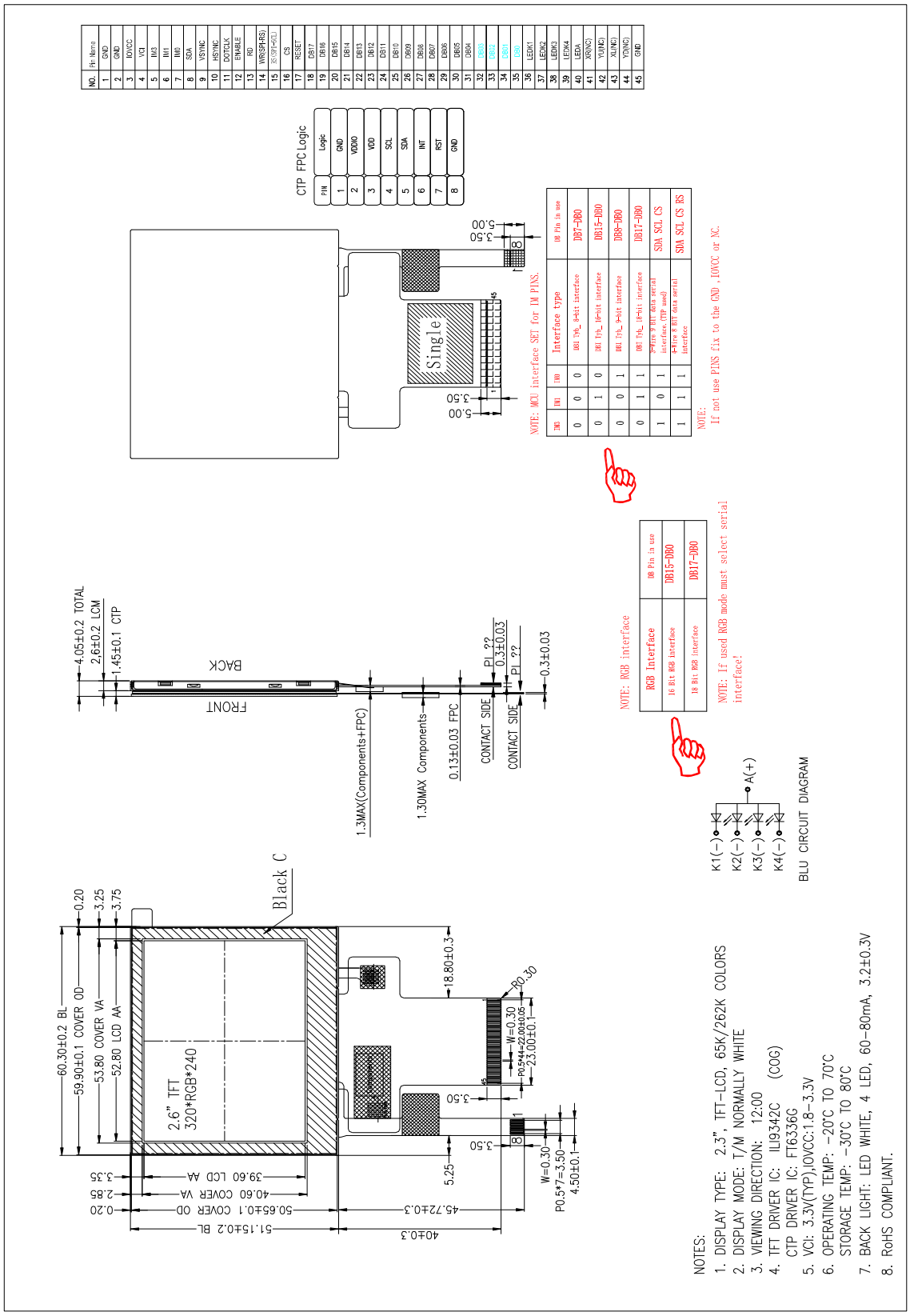
<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>GND</td><td>Ground.</td></tr>
<tr><td>2</td><td>GND</td><td>Ground.</td></tr>
<tr><td>3</td><td>IOVCC</td><td>Supply voltage(1.65-3.3V)</td></tr>
<tr><td>4</td><td>VCI</td><td>Supply voltage(3.3V).</td></tr>
<tr><td>5</td><td>IM3</td><td rowspan="3">
<table>
<tr><th>IM3</th><th>IM2</th><th>IM0</th><th>Interface type</th><th>DB pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Type_8bit interface</td><td>DB7-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Type_16bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Type_9bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Type_18bit interface</td><td>DB17-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-wire 9Bit data serial</td><td>SDA SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-wire 8Bit data serial</td><td>DSA SCL CS RS</td></tr>
</table>
Interface selection</td></tr>
<tr><td>6</td><td>IM2</td></tr>
<tr><td>7</td><td>IM0</td></tr>
<tr><td>8</td><td>SDA</td><td>Serial input signal. The data is applied on the rising edge of the SCL signal.
If not used, fix this pin at VCI or GND.</td></tr>
<tr><td>9</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>10</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use</td></tr>
<tr><td>11</td><td>DOTCLK</td><td>Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>12</td><td>ENABLE</td><td>Data enable signal for RGB interface operation. Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>13</td><td>RD</td><td>Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>14</td><td>WR(SPI-RS)</td><td>(WR): Serves as a write signal and writes data at the rising edge. 4-line system (RS): Serves as command or parameter select. Fix to IOVCC or GND level when not in use.</td></tr>
<tr><td>15</td><td>RS(SPI-SCL)</td><td>This pin is used to select “Data or Command” in the parallel interface. When RS = ’1’, data is selected.
When RS = ’0’, command is selected.
This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to IOVCC or GND.</td></tr>
</table>

		RS_SCL1 is equal to RS(SCL).
16	CS	Chip select input pin (“Low” enable). This pin can be permanently fixed “Low” in MPU interface mode only. CSX1 is equal to CSX.
17	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. RESX1 is equal to RESX.
18-35	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode .Fix to GND level when not in use
36-39	LEDK1-4	Cathode pin of backlight
40	LEDA	Anode pin of backlight
41	XR	Touch panel Right Glass Terminal
42	YU	Touch panel Top Film Terminal
43	XL	Touch panel LIFT Glass Terminal
44	YD	Touch panel Bottom Film Terminal
45	GND	Ground

3.2 CTP

No.	Symbol	Description
1	GND	Ground
2	VDDIO	I/O power supply voltage
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

4 Mechanical Drawing



5 Electrical Characteristics

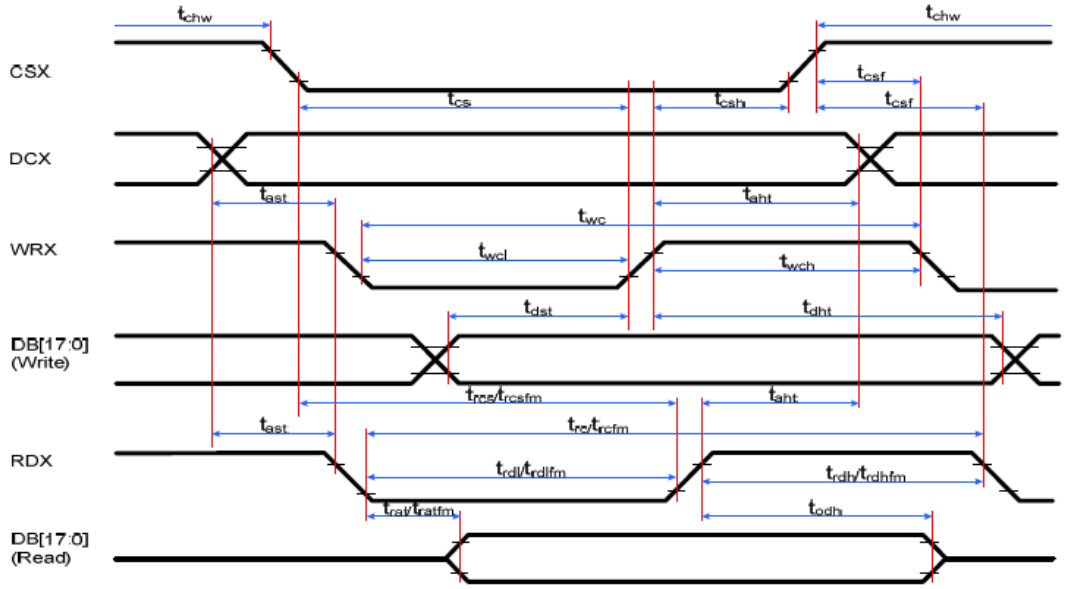
Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VCI		2.5	2.8	3.3	V
Normal mode Current	IDD		-	3	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃
LED Forward Current	If		70	80	-	mA
LED Forward Voltage	Vf		-	3.2	-	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	ΘU	-	35	-	deg
View Angles Bottom	ΘD	-	15	-	deg
View Angles Right	ΘR	-	45	-	deg
View Angles Left	ΘL	-	45	-	deg
Response Time	Tr +Tf		35	50	ms
Contrast Ratio	CR	-	300	-	--
LCM Luminance	Lv	270	-	-	cd/m^2

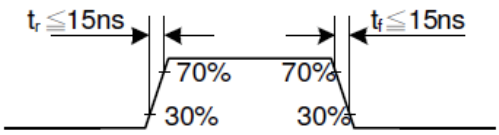
7 AC Characteristics

7.1 Parallel 8/9/18bit interface Timing Characteristics(8080 system)

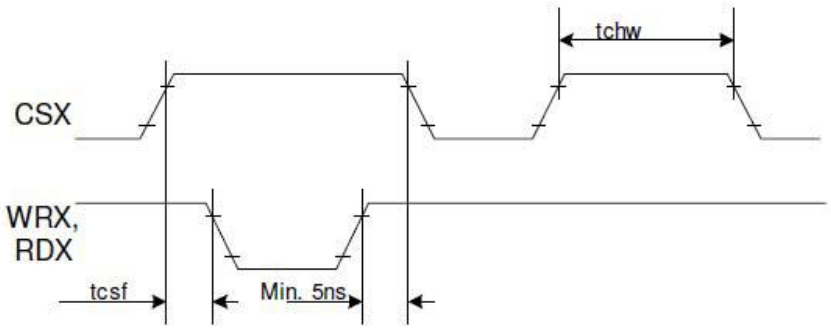


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, GND=0V.

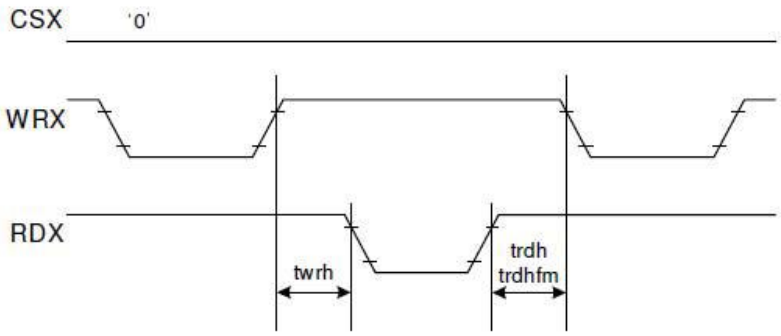


CSX timins :



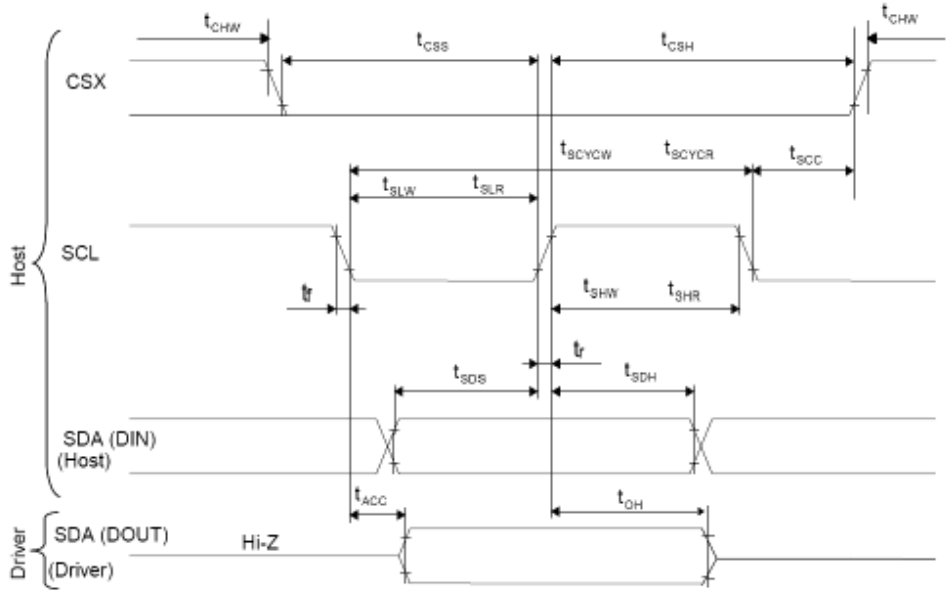
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



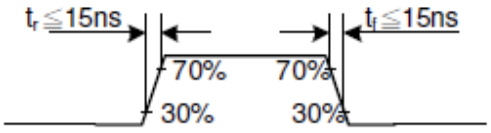
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.2 Serial Interface (3-line SPI system) Timing Characteristics

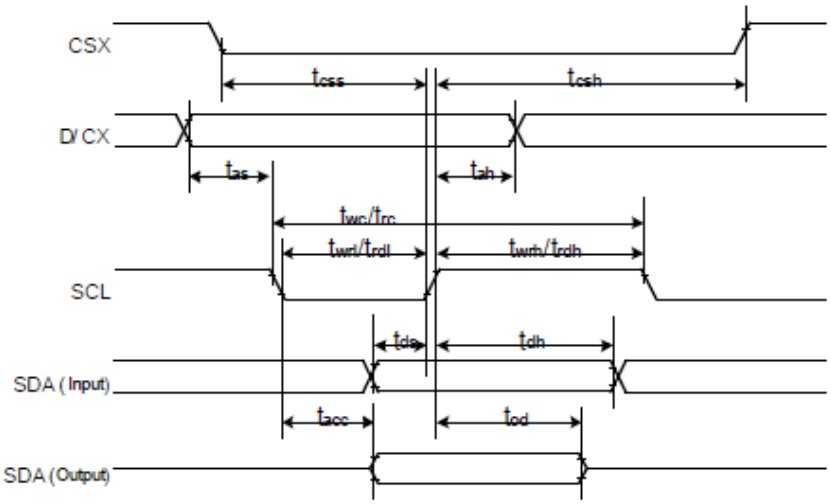


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	35	-	ns	
	tslw	SCL "L" Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time(write)	30	-	ns	
	tcsh		30	-	ns	

Note: Ta = 25 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V

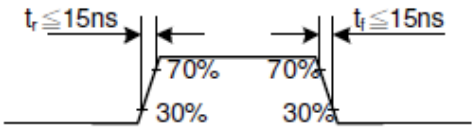


7.3 Serial interface (4-line SPI system) Timing Characteristics

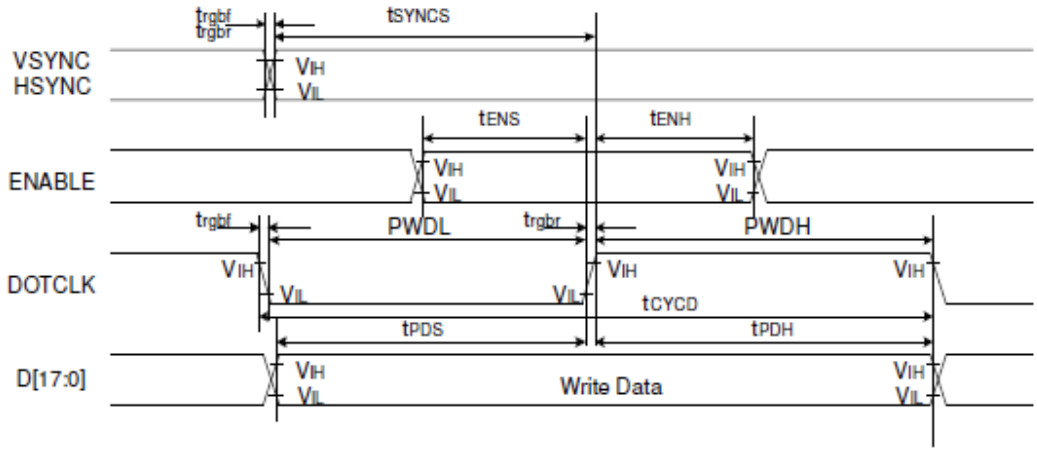


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	30	-	ns	
	tcsh	Chip select hold time (write)	30	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	35	-	ns	
	twrl	SCL "L" pulse width (Write)	35	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	-	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V

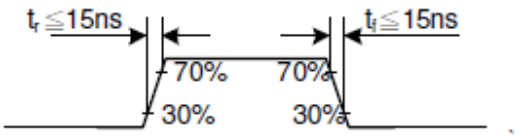


7.4 Display Parallel(16/18 bit interface) Timing Characteristics

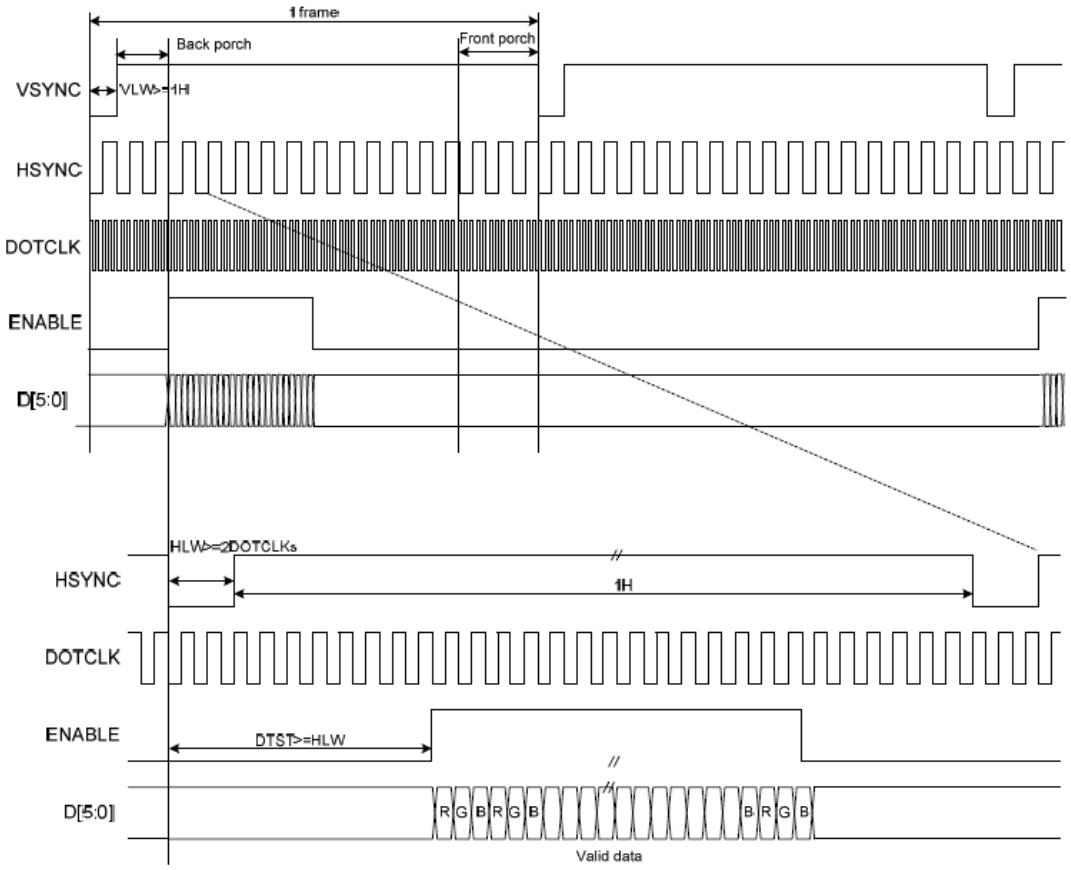


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

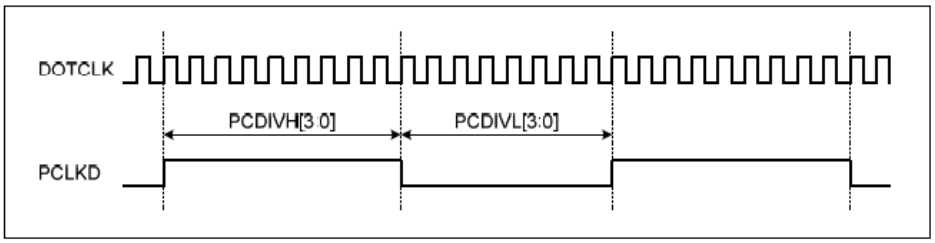
Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V



7.5 RGB Interface Timing Characteristics



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

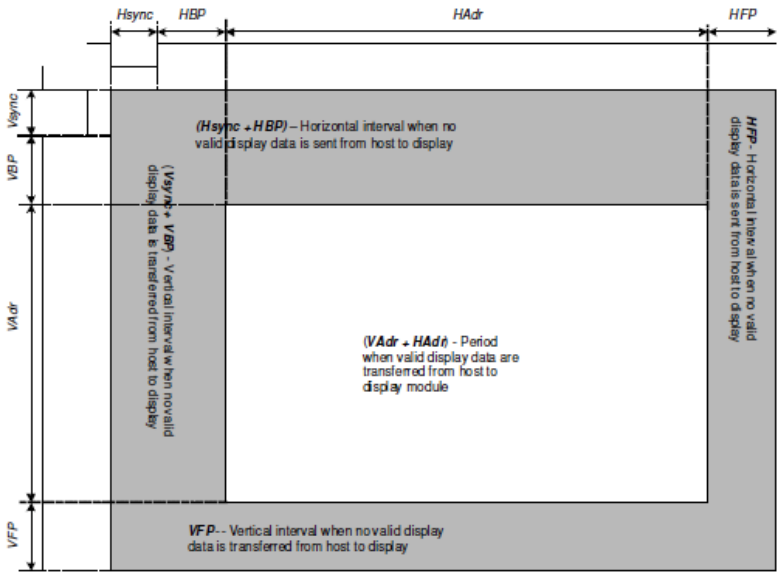


Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

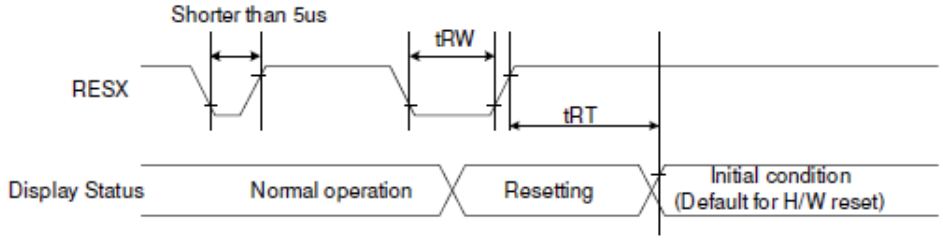
Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Back Porch(By pass mode)*	HBP(BP)		58	68	200	DOTCLK
Horizontal Address	HAdr		-	320	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line

7.6 Reset Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

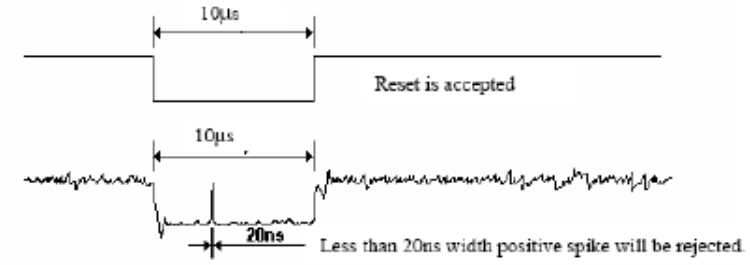
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 CTP Specification

8.1 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		2.8	3.3	3.47	V
Normal mode Current			-	4	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃

NOTES:

If used beyond the absolute maximum ratings, FT6336G may be permanently damaged. It is strongly recommanded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device

8.2 AC Characteristics

Item	Condition	Min	Typ	Max	Unit
OSC clock	AVDD=2.8V;Ta=25° C	34.65	35	35.35	MHz

AC characteristics of Oscillators

I2C interface:

The I2C is always configured in the Slave mode, The data transfer format is shown in Figure4-1:

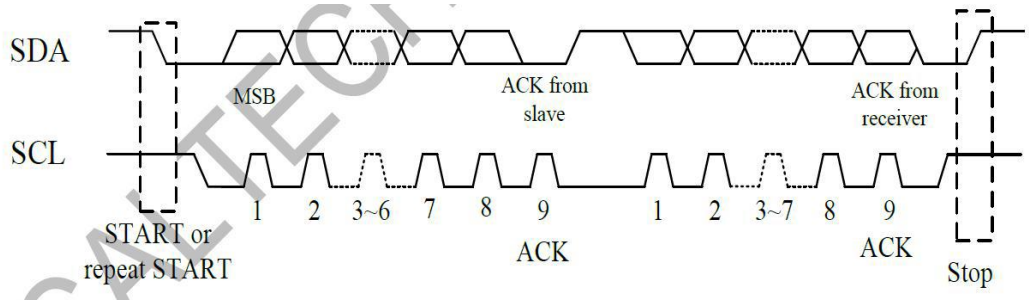


Figure 4-1 I2C Serial Data Transfer Format

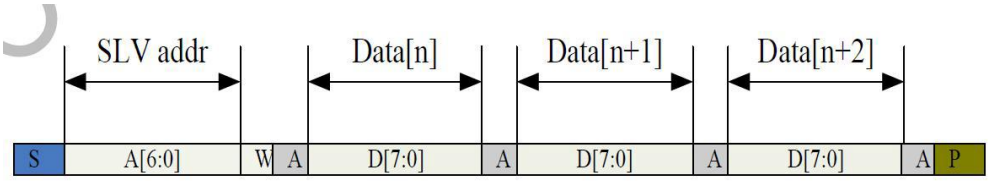


Figure 4-2 I2C master write, slave read

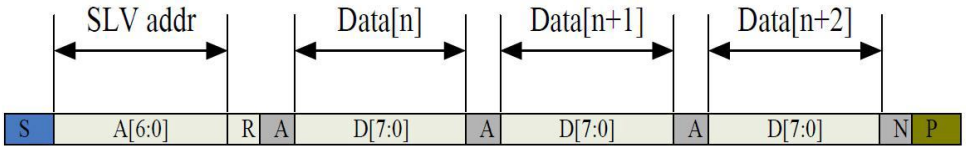


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

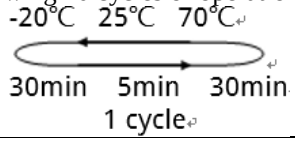
Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq