DisplayModule

DM-TFT24-442

2.4" 240x320 TRANSFLECTIVE DISPLAY PANEL WITH RESISTIVE TOUCH– MCU/SPI/RGB

Contents

1 Revision History

Date	Changes
2022-06-29	First release

2 Main Features

Item	Specification	Unit
Size	2.4	Inch
Resolution	240(RGB) x 320	pixel
Module Dimension	42.92 x 60.26 x3.55	mm
Display area	36.72(H) *48.96(V)	mm
Pixel pitch	0.153 (H) x 0.153 (V)	mm
TFT Controller IC	ST7789V	-
Interface	8/9/16/18Bit MCU Interface 3/4SPI+16/18Bit RGB Interface 3-line/4-line Serial Interface	-
Display Color	65K/262K	colors
View Direction	SUPER WIDE	O'clock
Display mode	Transflective /Normally Black VA	-
Weight	TBD	g
Operating temperature	-20~+70	℃
Storage temperature	-30~+80	℃

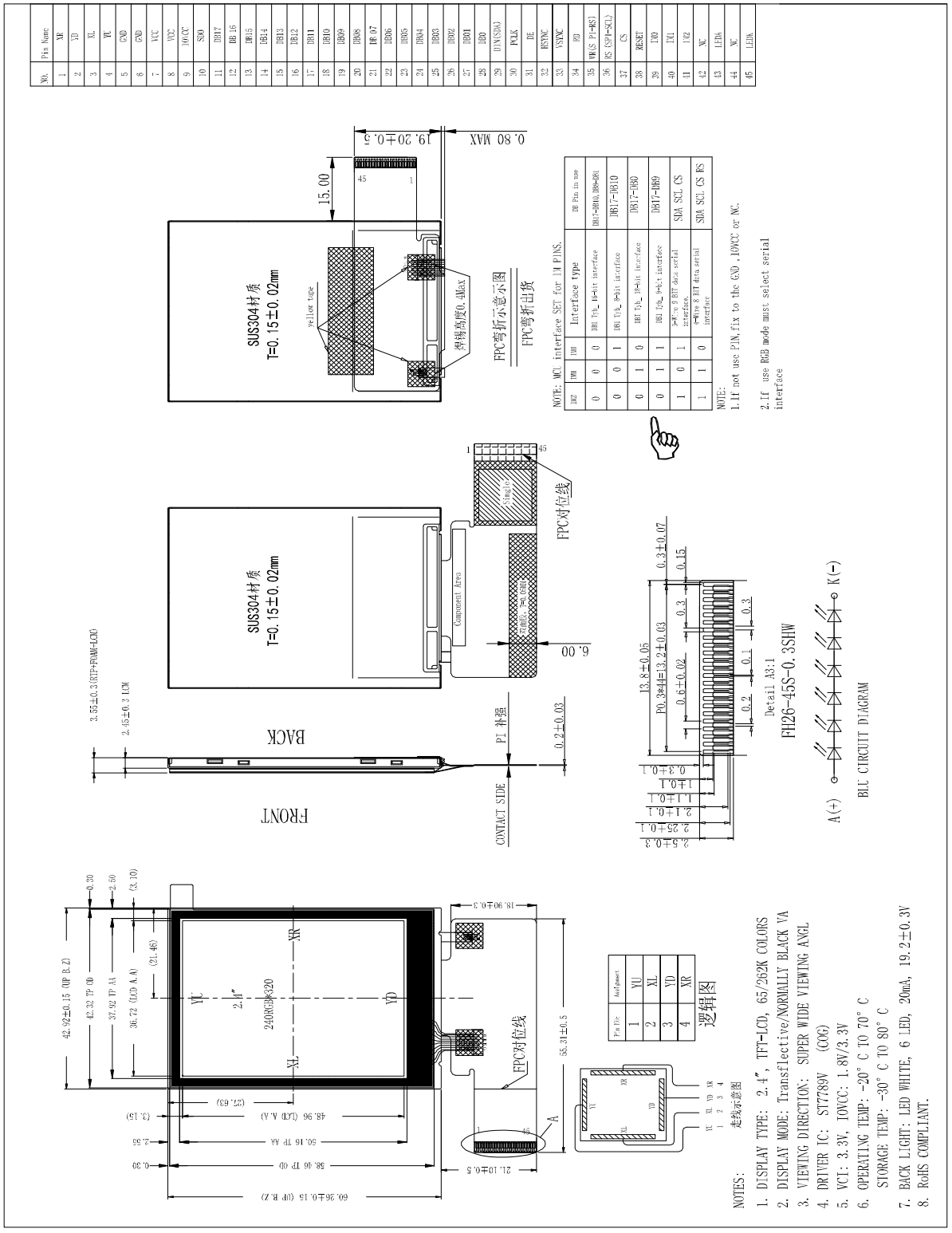
3 Pin Description

No.	Symbol	Description
1	XR	Touch panel Right Glass Terminal
2	YD	Touch panel Bottom Film Terminal
3	XL	Touch panel LIFT Glass Terminal
4	YU	Touch panel Top Film Terminal
5	GND	Ground.
6	GND	Ground.
7	VCC	Supply voltage(3.3V).
8	VCC	Supply voltage(3.3V).

9	IOVCC	Power Supply for I/O System.
10	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.
11-28	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode. Fix to GND level when not in use
29	DIN(SDA)	Serial input signal. The data is latched on the rising edge of the SCL signal. fix this pin at IOVCC or GND when not in use.
30	PCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
31	DE	Data enable signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.
32	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.
33	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.
34	RD	Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at IOVCC or DGND.
35	WR(SPI-RS)	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at IOVCC or DGND.
36	RS(SPI-SCL)	-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock. RS=’1’: display data or parameter. RS=’0’: command data. -If not used, please fix this pin at IOVCC or DGND.
37	CS	Chip select input pin (“Low” enable).

		fix this pin at IOVCC or GND when not in use.
38	RESET	This signal will reset the device and must be applied to properly initialize the chip.
39	IM0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode. Fix to GND level when not in use
40	IM1	
41	IM2	
42	NC	--
43	LEDA	Anode pin of backlight
44	NC	--
45	LEDK	Cathode pin OF backlight

4 Mechanical Drawing



5 Electrical Characteristics

Item		Symbol	Min	Typ.	Max	Unit
Digital Supply Voltage	Absolute Maximum Rating	VCC	-0.3		4.6	V
Supply Voltage (Logic)	Absolute Maximum Rating	IOVCC	-0.3		4.6	V
Operating Temperature	Absolute Maximum Rating	TOP	-20		+70	℃
Storage Temperature	Absolute Maximum Rating	TST	-30		+80	℃
Digital Supply Voltage		VCC	2.4	3.3	3.6	V
Digital interface supple Voltage		IOVCC	1.65	1.8	3.3	V
Normal mode Current		IDD	--	7.3	--	mA
Level input voltage		V_{IH}	0.7*IOVCC	--	IOVCC	V
		V_{IL}	GND	--	0.3*IOVCC	V
Level output voltage		V_{OH}	0.8*IOVCC	--	IOVCC	V
		V_{OL}	GND	--	0.2*IOVCC	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
Forward Current	I_F	15	20	-	mA
Forward Voltage	V_F	--	19.2	-	V
LCM Luminance	LV	240	290	-	cd/m2
LED life time	H_r	50000	--	-	Hour
Uniformity	Avg	80	--	-	%

7 AC Characteristics

7.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

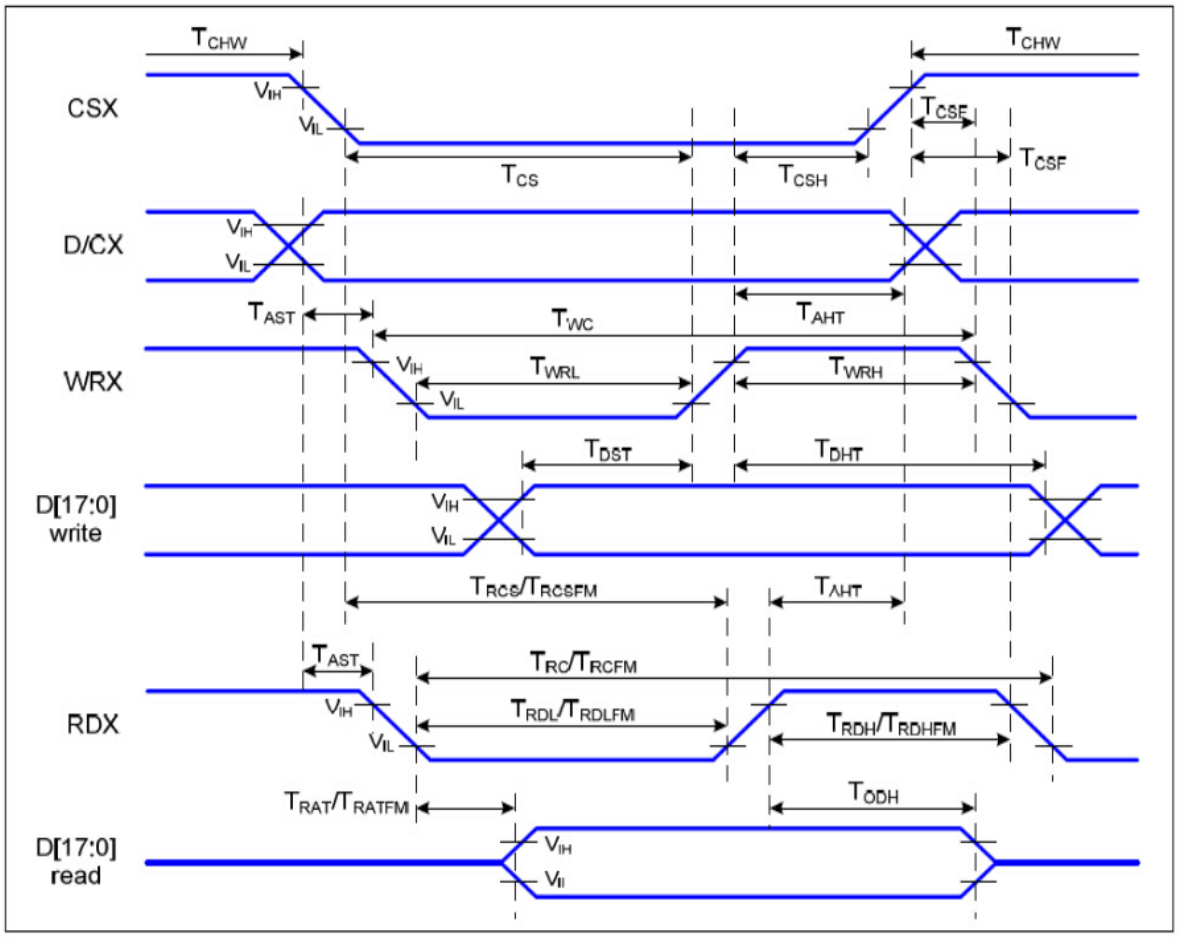


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

	T_{DHT}	Data hold time	10		ns
	T_{RAT}	Read access time (ID)		40	ns
	T_{RATFM}	Read access time (FM)		340	ns
	T_{ODH}	Output disable time	20	80	ns

Table 4 8080 Parallel Interface Characteristics

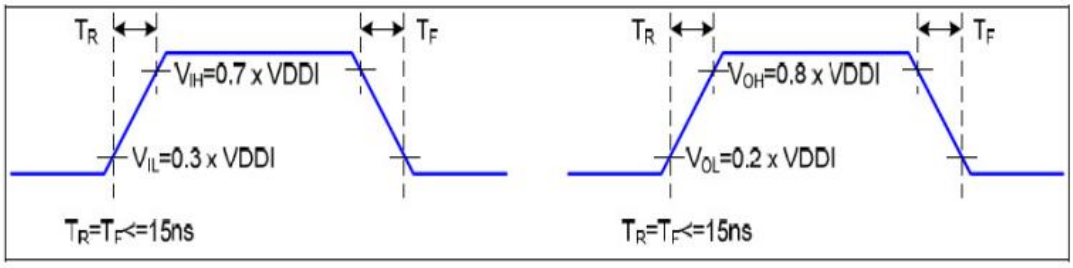


Figure 2 Rising and Falling Timing for I/O Signal

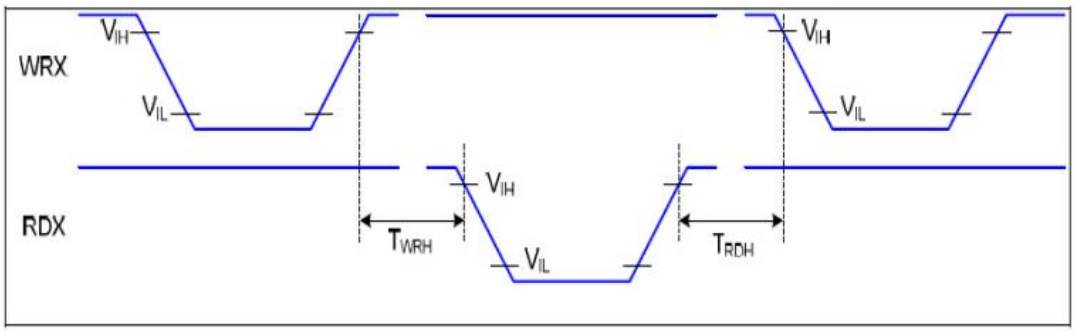


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.2 Serial Interface Characteristics (3-line serial)

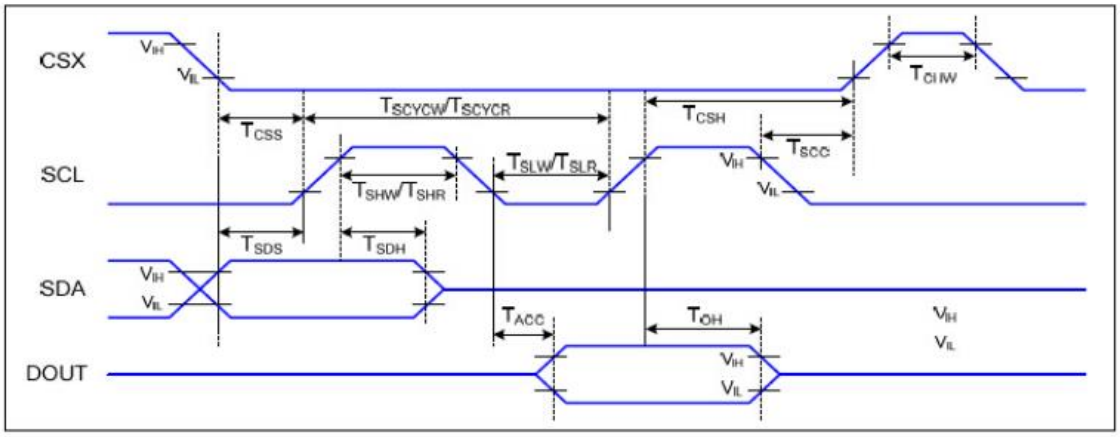


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.3 Serial Interface Characteristics (4-line serial)

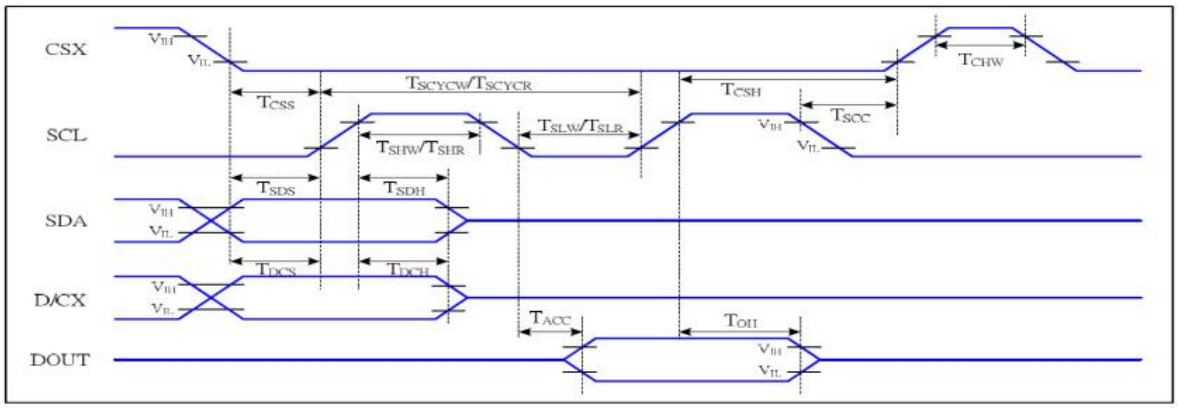


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as

7.4 RGB Interface Characteristics

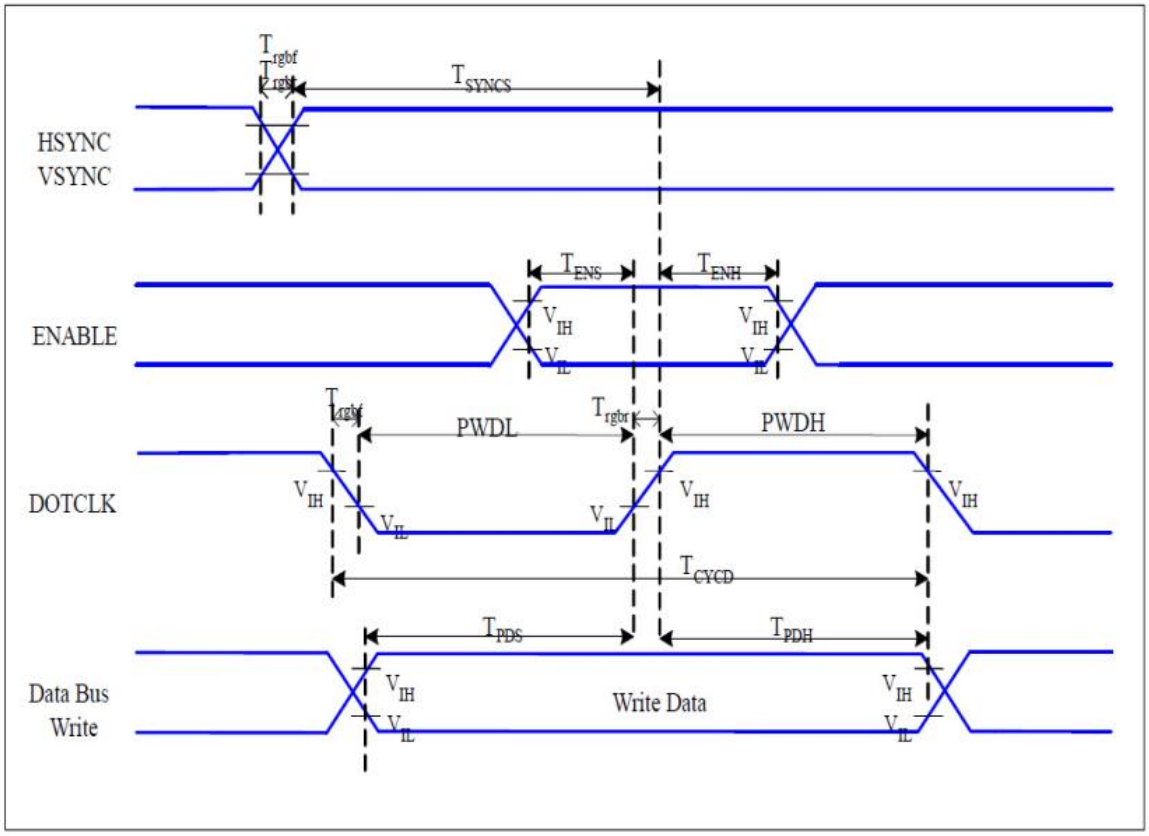


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	25	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	

	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	25	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	25	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	55	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	25	-	ns	
	T_{PDH}	PD Data Hold Time	25	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

7.5 Reset Timing

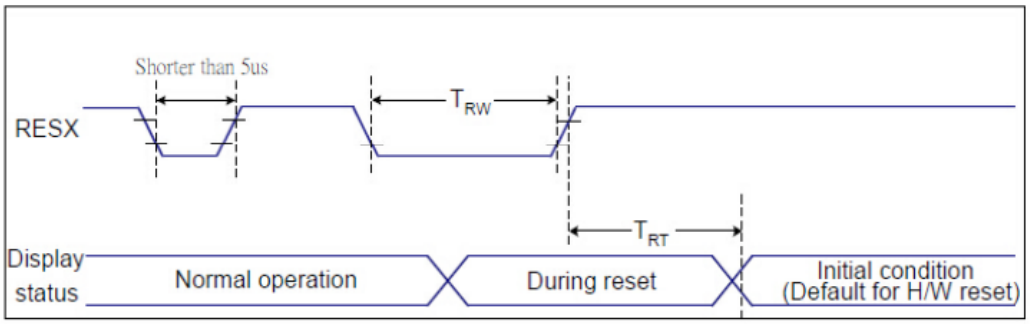


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

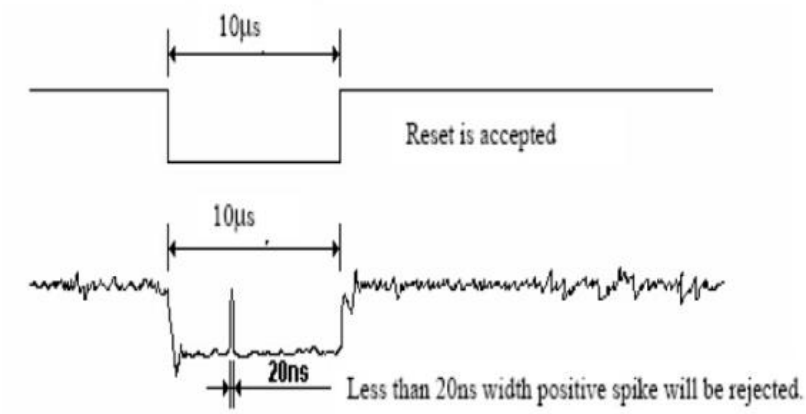
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. -20℃ 25℃ 70℃ 30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz;	3

		One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq