



**DM-TFT24-432**  
**2.4" IPS 480x480 HIGH BRIGHTNESS**  
**TFT DISPLAY PANEL –MIPI**

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## 1 Revision History

Date	Changes
2022-05-16	First release

## 2 Main Features

Item	Specification	Unit
Size	2.4	Inch
Resolution	480(RGB) x 480	pixel
Module Dimension	69.19 x 71.74 x 2.5	mm
Display area	62.64 x 62.64(circle)	mm
Pixel pitch	0.1305 x 0.1305	mm
TFT Controller IC	ST7701S	-
Interface	2-lane MIPI	-
Display Color	65K/262K/16.7M	colors
Pixel arrangement	RGB 2domain stripe	
View Direction	Free	O'clock
Display mode	Transmissive /Normally Black	-
Weight	20	g

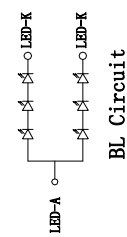
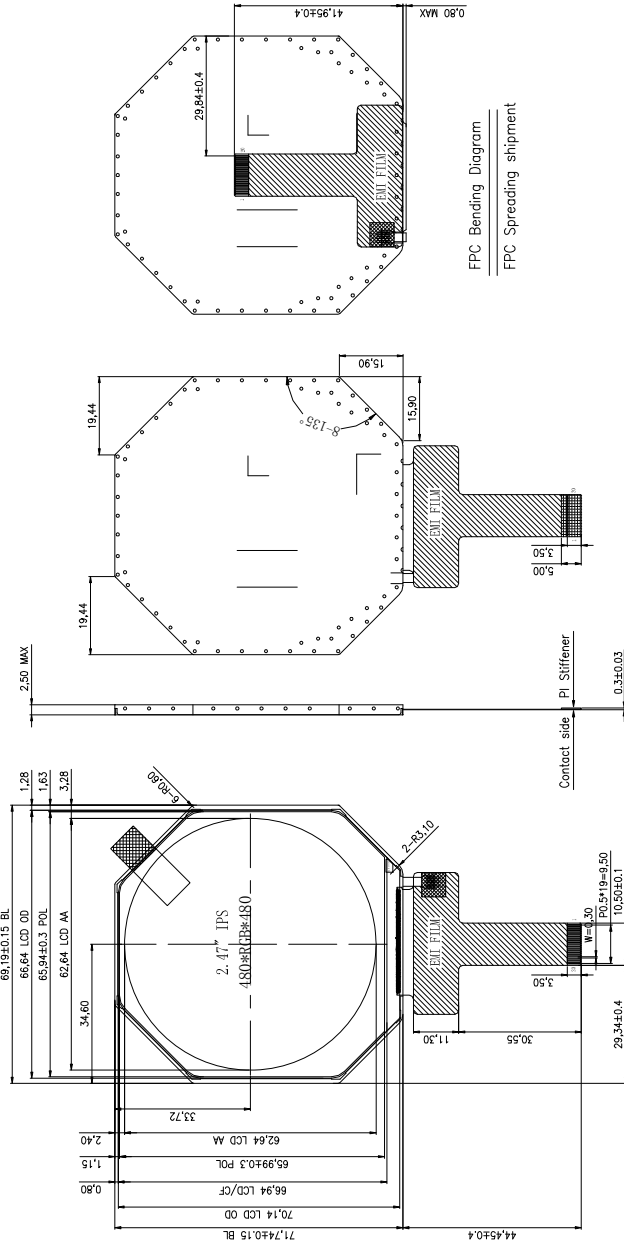
## 3 Pin Description

### 3.1 TFT

No.	Symbol	Description
1	NC	-
2	LEDK	Cathode pin of backlight.
3	NC	-
4	LEDA	Anode pin of backing.
5	NC	-
6	VCI	Supply voltage (3.3V).
7	IOVCC	I/O power Supply Voltage.
8	TE	-Tearing effect output Leave the pin to open when not in use.
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
10	GND	Ground.
11	MIPI_D1P	MIPI DSI differential data pair(DSI-Dn+/-). If MIPI are not used, they should be connected to DGND
12	MIPI_D1N	
13	GND	Ground.
14	MIPI_CLP	MIPI DSI differential clock pair(DSI-CLK+/-). If MIPI are not used, they should be connected to DGND.
15	MIPI_CLN	
16	GND	Ground,
17	MIPI_D0P	MIPI DSI differential data pair(DSI-Dn+/-). If MIPI are not used, they should be connected to DGND
18	MIPI_D0N	
19	GND	Ground.
20	GND	Ground.

# 4 Mechanical Drawing

No.	Pin Name
1	NC
2	LEDK
3	NC
4	LEDA
5	NC
6	VDD/VCI
7	IOVCC
8	TE
9	RESET
10	GND
11	MIPL_D1P
12	MIPL_D1N
13	GND
14	MIPL_C1P
15	MIPL_C1N
16	GND
17	MIPL_D0P
18	MIPL_D0N
19	GND
20	GND



- NOTES:
1. DISPLAY TYPE: 2.47" TFT-LCD, 16.7M COLORS
  2. DISPLAY MODE: NORMALLY BLACK
  3. VIEWING DIRECTION: FREE
  4. LCM DRIVER IC: S17701S (COG)
  5. LCM Interface: 2LANE-MIPI
  6. Touch Mode: Non
  7. Touch Driver: Non
  8. Touch Interfac: Non
  9. Touch and LCM Bonding technology: Non
  10. VDD/VCI: 3.3V; LCM IOVCC:1.8~3.3V
  11. OPERATING TEMP: -10°C TO 60°C  
STORAGE TEMP: -30°C TO 70°C
  12. BACK LIGHT: LED WHITE, 6 LED, 40mA, 9.3±0.3V
  13. RoHS COMPLIANT.

## 5 Optics & Electrical Characteristics

### 5.1 Optics Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles TOP	∅U	-	85	-	deg	CR ≥ 10
View Angles Bottom	∅D	-	85	-	deg	
View Angles Right	∅R	-	85	-	deg	
View Angles Left	∅L	-	85	-	deg	
C.I.E(White)	(x)	0.2571	0.2971	0.3371	-	∅=0 Normal viewing angle
	(y)	0.2848	0.3248	0.3648	-	
C.I.E(Red)	(x)	0.6030	0.6230	0.6430	-	
	(y)	0.3228	0.3428	0.3628	-	
C.I.E(Green)	(x)	0.3049	0.3249	0.3449	-	
	(y)	0.5678	0.5878	0.6078	-	
C.I.E(Blue)	(x)	0.1298	0.1498	0.1698	-	
	(y)	0.0474	0.0674	0.0874	-	
Uniformity	S(%)	65	70	-	%	C-light
Response Time	T <sub>R</sub> + T <sub>F</sub>	-	-	35	ms	-
Contrast Ratio	CR	-	800	1000	--	-

- Measuring surrounding: dark room
- Ambient temperature: 25±2°C
- 15min. warm-up time.

### 5.2 Absolute Maximum Ratings

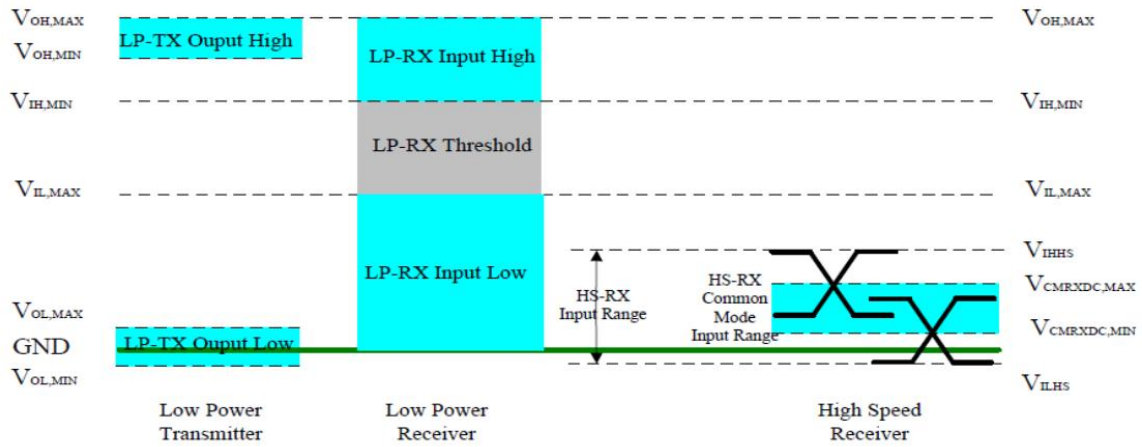
Item	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	V <sub>CI</sub>	-0.3	-	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	-	4.6	V
Operating Temperature	T <sub>OP</sub>	-10	-	+60	°C
Storage Temperature	T <sub>ST</sub>	-30	-	+70	°C

Note 1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

### 5.3 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Supply Voltage	V <sub>CI</sub>	2.5	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current	IDD	--	15	--	mA	
Differential Input High Threshold Voltage	V <sub>IT+</sub>	-	0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	V <sub>IT-</sub>	-50	-		mV	
Single-ended Receiver Input Operation Voltage Range	V <sub>IR</sub>	0.5	-	1.2	V	

## 5.4 MIPI DC Electrical Characteristics



Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	$V_{LPH}$	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	$V_{IL,HS}$	-40	-	-	mV
Single-ended input high voltage	$V_{IH,HS}$	-	-	460	mV
Common-mode voltage	$V_{CM,HS}$	70	-	330	mV
Differential input impedance	$Z_{ID}$	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	$V_I$	-50	-	1350	mV
Logic 0 input threshold	$V_{IL}$	0-	-	550	mV
Logic 1 input threshold	$V_{IH}$	880	-	1350	mV
Output low level	$V_{OL}$	-50	-	50	mV
Output high level	$V_{OH}$	1.1	1.2	1.3	V

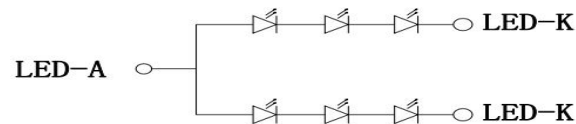
## 5.5 LED Backlight Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	IF	-	40	-	mA	
Forward Voltage	VF	-	9.3	-	V	
LCM Luminance (IF =20mA)	LV	380	430	-	cd/m <sup>2</sup>	Note3
LED life time	Hr	-	50000	-	Hour	Note1,2
Uniformity	Avg	80	-	-	%	Note3

The back-light system is edge-lighting type with 6 chips LED.

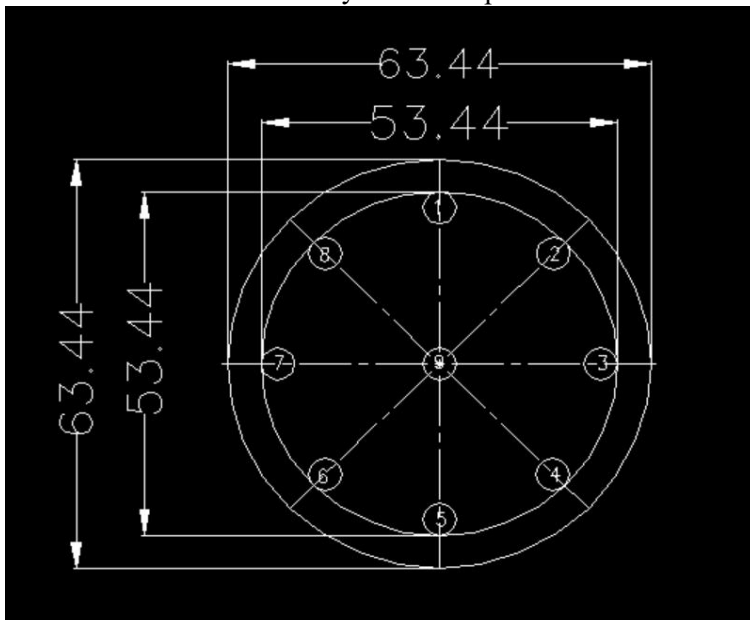
Note1:LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note2:The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



**BL Circuit**

Note3:Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\min \text{ luminance in } 9 \text{ points}}{\max \text{ luminance in } 9 \text{ points}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of } 9 \text{ points}}{9}$$



## 6 AC Characteristics

### 6.1 MIPI Interface Characteristics:

#### 6.1.1 High Speed Mode

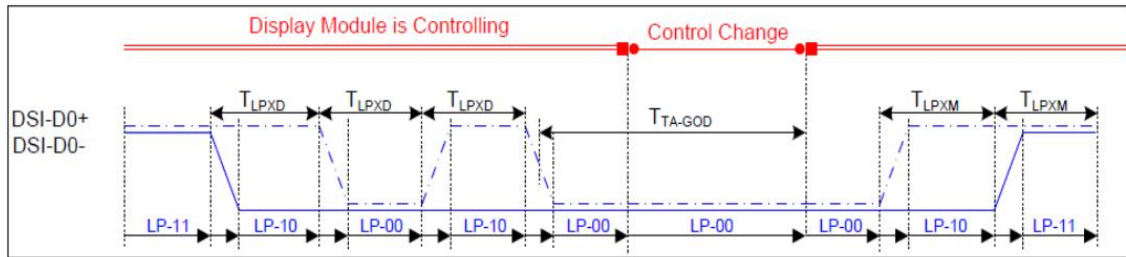


DSI clock channel timing

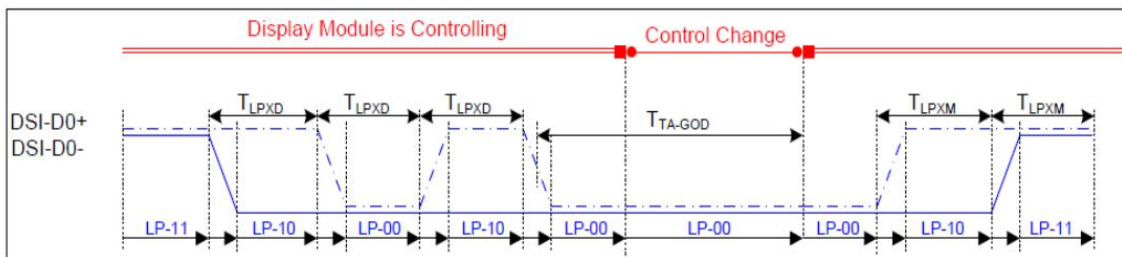
Signal	Symbol	Description	Min	Max	Unit	Remark
DSI-CLK+/-	$2 \times UI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	$UI_{INSTA}$ $UI_{INSTB}$	UI instantaneous halves	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	$t_{DS}$	Data to clock Setup Time	0.15	-	UI	
DSI-Dn+/-	$t_{DH}$	Data to clock hold time	0.15	-	UI	

#### \*Mipi Interface-High SpeedMode Timing Characteristics

## 6.1.2 Low Power Mode



\*Bus Turnaround (BTA) from MPU to display module Timing

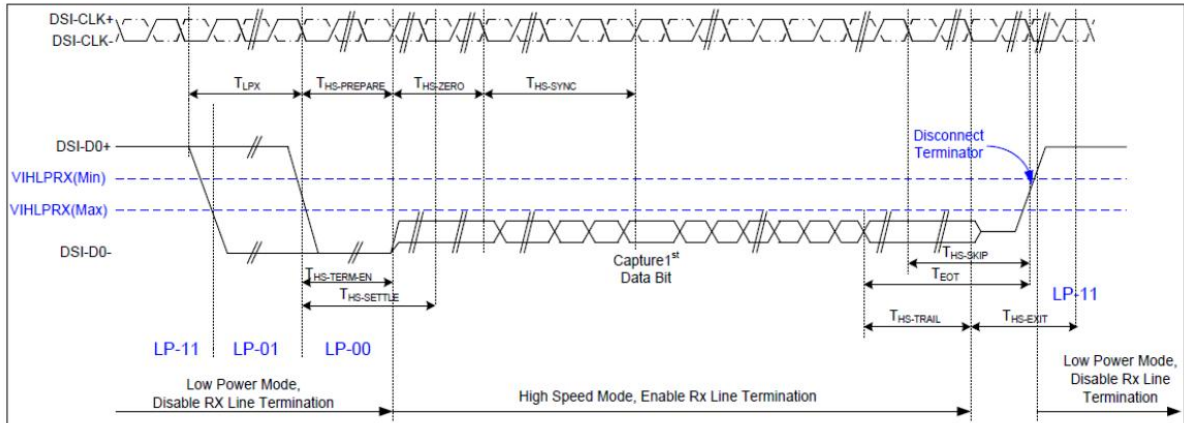


\*Bus Turnaround (BTA) from MPU to display module Timing

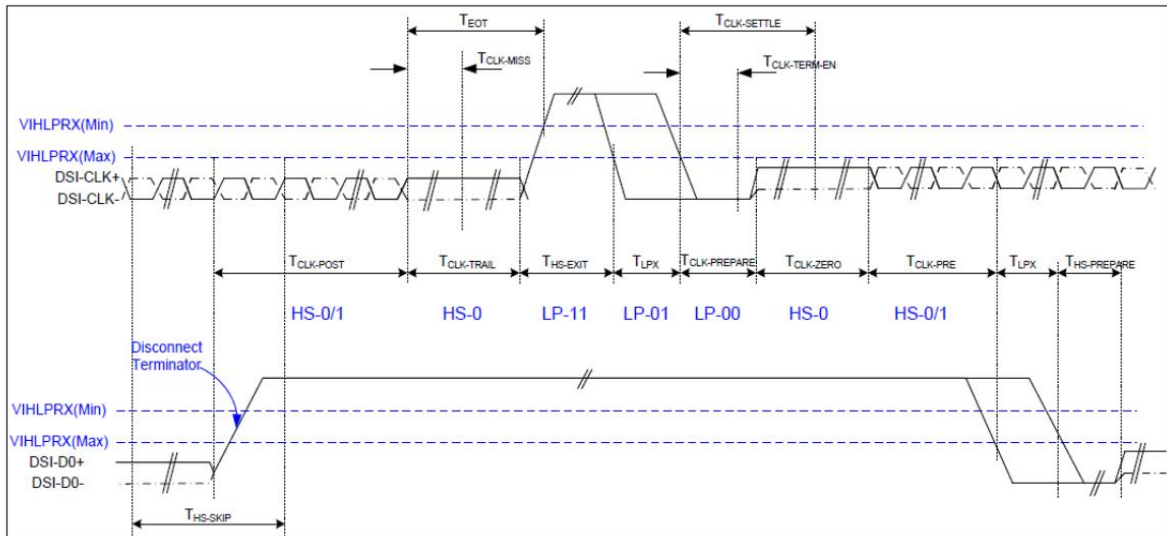
Signal	Symbol	Description	Min	Max	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01,LP-10 or LP-11 periods MPU → Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01,LP-10 or LP-11 periods MPU → Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	$T_{LPXD}$	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5 \times T_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4 \times T_{LPXD}$		ns	Output

\*Mipi Interface Low Power Mode Timing Characteristics

### 6.1.3 Bursts Mode



**\*Data lanes-Low Power Mode to/from High Speed Mode Timing**



**\*Clock lanes-High Speed Mode to/from Low Power Mode Timing**

Signal	Symbol	Description	Min	Max	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+10UI	-	ns	Input

High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Timing-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after lat payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Timing to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105ns +12UI	ns	Input

### 6.1.4 Reset timing:

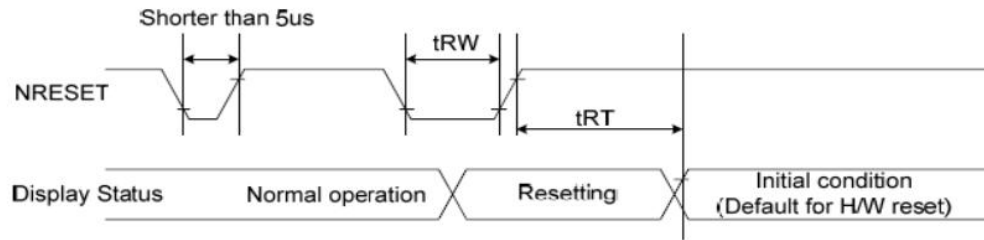


Figure 102 Reset Timing

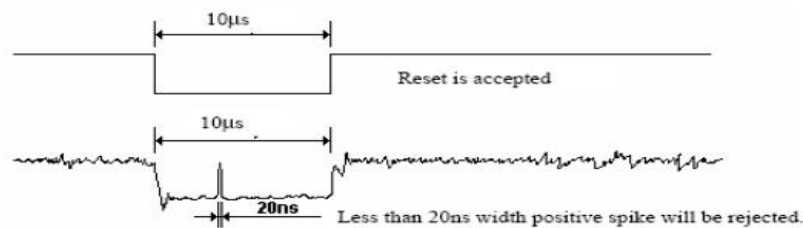
Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset Pulse Duration	10	-	$\mu$ s
	tRT	Reset Cancel	-	5(Note 1,5)	ms
			-	120(Note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than $5\mu$ s	Reset Rejected
Longer than $9\mu$ s	Reset
Between $5\mu$ s and $9\mu$ s	Reset Starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 7 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	90°C 96hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85°C 96hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30°C 96hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation.	-30°C/85°C 20 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55 Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	C=150pF, R=330,5points /panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

## 8 Warranty and Conditions

<http://www.displaymodule.com/pages/faq>