

DM-TFT24-383
2.4" 240x320 TRANSFLECTIVE
DISPLAY PANEL –SPI ,MCU,
RGB

Contents

- 1 Revision History
- 2 Main Features
- 3 Pin Description
- 4 Mechanical Drawing
- 5 Electrical Characteristics
- 6 Optical Characteristics
- 7 AC Characteristics
 - 7.1 Parallel 8/9/18bit interface Timing Characteristics(8080 system)
 - 7.2 Serial Interface (3-line SPI system) Timing Characteristics
 - 7.3 Serial interface (4-line SPI system) Timing Characteristics
 - 7.4 RGB Interface Timing Characteristics
 - 7.5 Reset Timing Characteristics
- 8 Reliability
- 9 Warranty and Conditions

1 Revision History

Date	Changes
2019-04-18	First release

2 Main Features

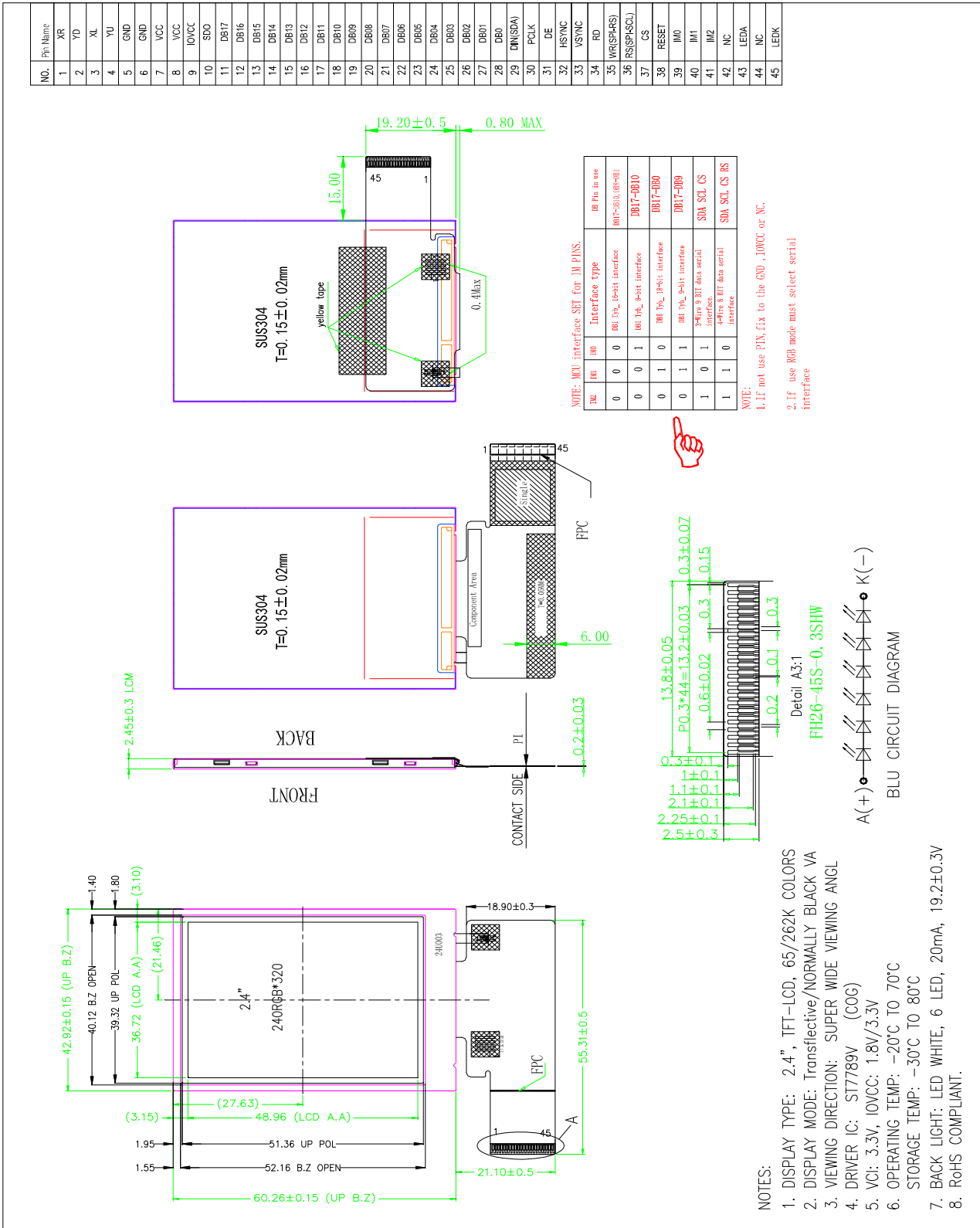
Item	Specification	Unit
Size	2.4	Inch
Resolution	240(RGB) x 320	pixel
Module Dimension	42.92 x 60.26 x 2.45	mm
Display area	36.72 x 48.96	mm
Pixel pitch	0.153 x 0.153	mm
TFT Controller IC	ST7789V	-
CTP Driver IC	None , can match RTP or CTP with FT6336G	-
Interface	8/9/16/18 Bit MCU 3/4SPI+16/18bit RGB 3-line/4-line Serial	-
Display Color	65K/262K	colors
View Direction	Super wide	O'clock
Display mode	Transflective / Normally Black VA	-
Weight	TBD	g

3 Pin Description

No.	Symbol	Description
1	XR	Touch panel Right Glass Terminal
2	YD	Touch panel Bottom Film Terminal
3	XL	Touch panel LEFT Glass Terminal
4	YU	Touch panel Top Film Terminal
5	GND	Ground
6	GND	Ground
7	VCC	Supply voltage(3.3V)
8	VCC	Supply voltage(3.3V)
9	IOVCC	Power Supply for I/O System
10	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.
11-28	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode. Fix to GND level when not in use
29	DIN(SDA)	Serial input signal. The data is latched on the rising edge of the SCL signal. fix this pin at IOVCC or GND when not in use.
30	PCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
31	DE	Data enable signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.
32	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.
33	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.
34	RD	Read enable in 8080 MCU parallel interface.

		-If not used, please fix this pin at IOVCC or DGND.
35	WR(SPI-RS)	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at IOVCC or DGND.
36	RS(SPI-SCL)	-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock. RS=' 1' : display data or parameter. RS=' 0' : command data. -If not used, please fix this pin at IOVCC or DGND.
37	CS	Chip select input pin ("Low" enable). fix this pin at IOVCC or GND when not in use.
38	RESET	This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active.
39	IM0	18-bit parallel bi-directional data bus for MCU system and RGB Interface mode. Fix to GND level when not in use
40	IM1	
41	IM2	
42	NC	-
43	LEDA	Anode pin of backlight
44	NC	-
45	LEDK	Cathode pin OF backlight

4 Mechanical Drawing



5 Electrical Characteristics

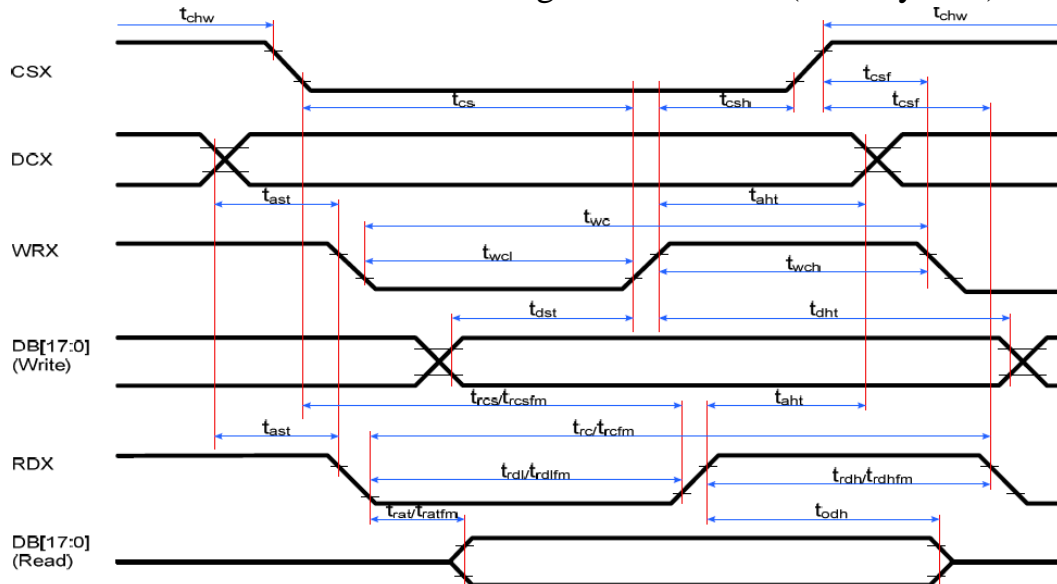
Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VCC		2.4	3.3	3.6	V
Supply Voltage Logic	IOVCC		1.65	1.8	3.3	V
Normal mode Current	IDD		-	7.3	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	°C
Storage Temperature	TST	Absolute Max	-30	-	+80	°C
LED Forward Current	If		15	20	-	mA
LED Forward Voltage	Vf		-	19.2	-	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	⊙U	-	80	-	deg
View Angles Bottom	⊙D	-	80	-	deg
View Angles Right	⊙R	-	80	-	deg
View Angles Left	⊙L	-	80	-	deg
Response Time	Tr +Tf		25	50	ms
Contrast Ratio	CR	-	300	-	--
LCM Luminance	Lv	310	360	-	cd/m ²

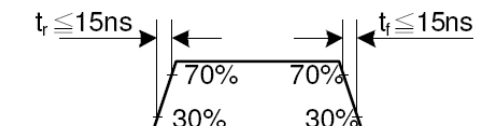
7 AC Characteristics

7.1 Parallel 8/9/18bit interface Timing Characteristics(8080 system)

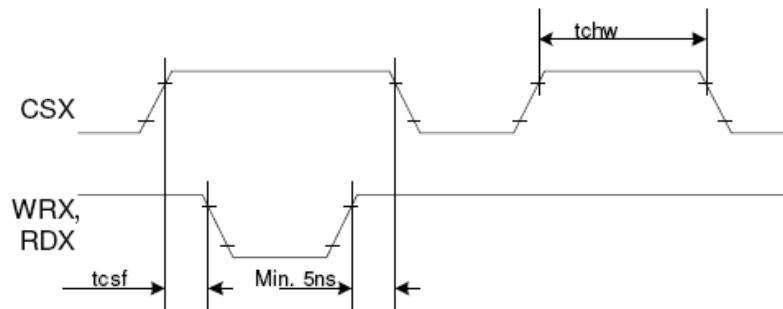


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
WRX	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
	twc	Write cycle	66	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	twrh	Write Control pulse H duration	15	-	ns	
	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
RDX (ID)	trdlfm	Read Control L duration (FM)	355	-	ns	
	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	trdl	Read Control pulse L duration	45	-	ns	
	tdst	Write data setup time	10	-	ns	
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	For maximum CL=30pF For minimum CL=8pF
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: $T_a = -30$ to 70 °C, $IOVCC=1.65V$ to $2.8V$, $VCI=2.6V$ to $3.3V$, $GND=0V$

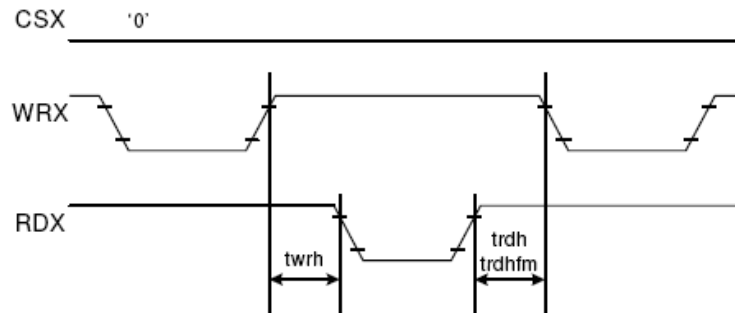


CSX timings :



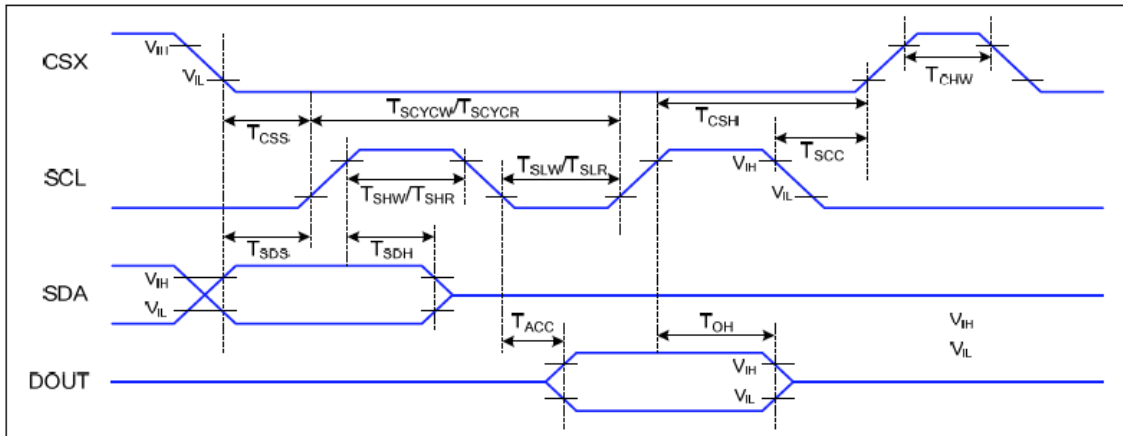
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

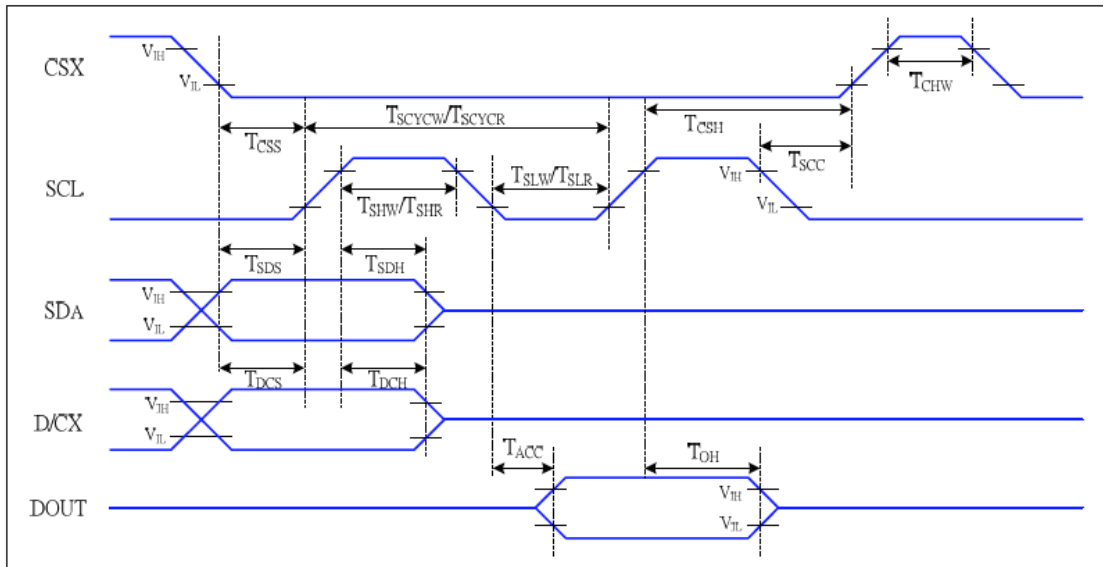
7.2 Serial Interface (3-line SPI system) Timing Characteristics



$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=-30$ to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $CL=8pF$

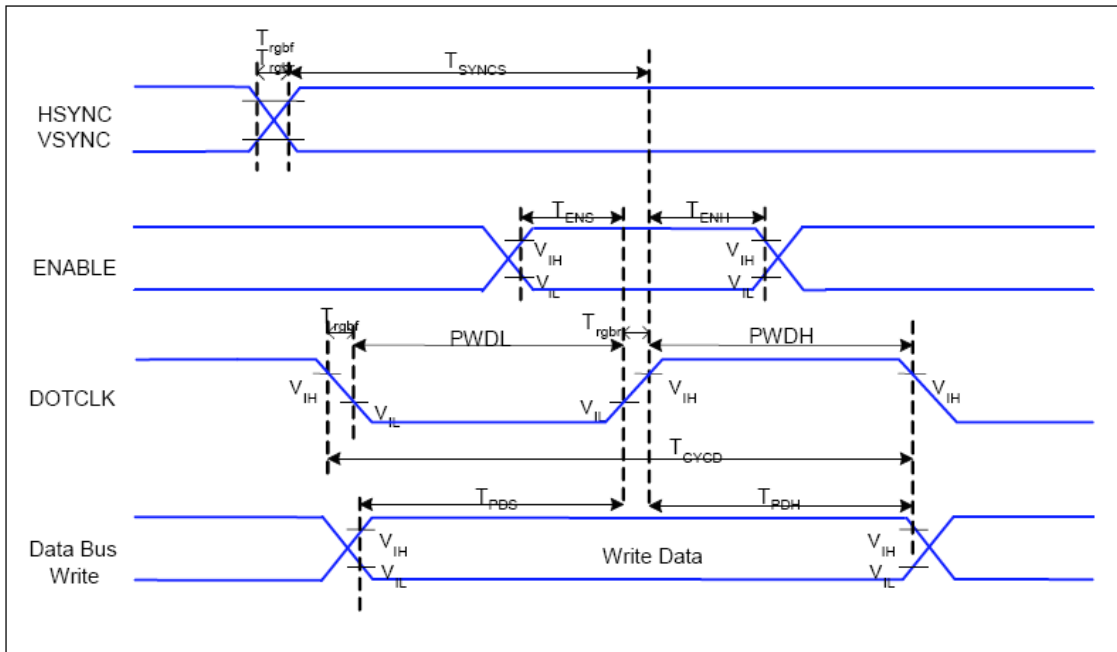
7.3 Serial interface (4-line SPI system) Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, T_a =-30 to 70 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

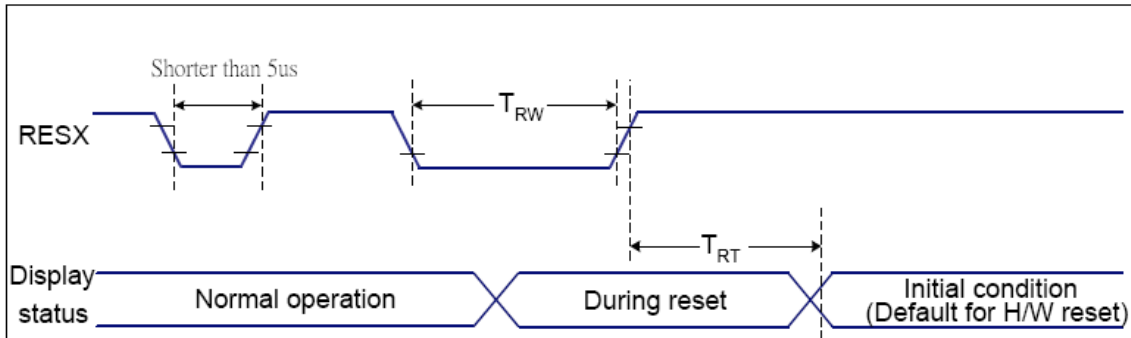
7.4 RGB Interface Timing Characteristics



$VDDI=1.65$ to $3.3V$, $VDD=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=-30 \sim 70 \text{ } ^\circ\text{C}$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	$PWDH$	DOTCLK High-level Pulse Width	60	-	ns	
	$PWDL$	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	T_{rghf}	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

7.5 Reset Timing Characteristics



$V_{DD1}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=-30 \sim 70$ °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			120 (Note 1, 6, 7)	ms	

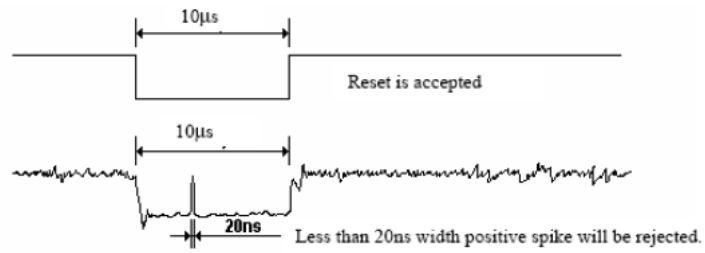
Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts


- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

- Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation.  <p style="text-align: center;">-20°C 25°C 70°C 30min 5min 30min 1 cycle</p>	-20°C/70°C 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

9 Warranty and Conditions

<http://www.displaymodule.com/pages/faq>