DisplayModule

DM-TFT24-311

2.4" TFT DISPLAY WITH 8/9/16/18 BIT MCU, 3/4 SPI AND 16/18 BIT RGB INTERFACE

Contents

1 Revision History

Date	Changes
2015-01-21	First release
2019-08-30	Second release

2 Main Features

Item	Specification	Unit
Screen Size	2.4	inch
Driver Mode	Transmissive	-
Display Colors	65K/262K	colors
Resolution	240 x 320	dots
Controller IC	ST7789V	-
Interface	8/16bit MCU, 3/4 SPI+16/18bit RGB	-
Power Supply	3.3	V
View Direction	12 o'clock	-
Background LED	4 LED Normally White	-
Weight	10.7	g

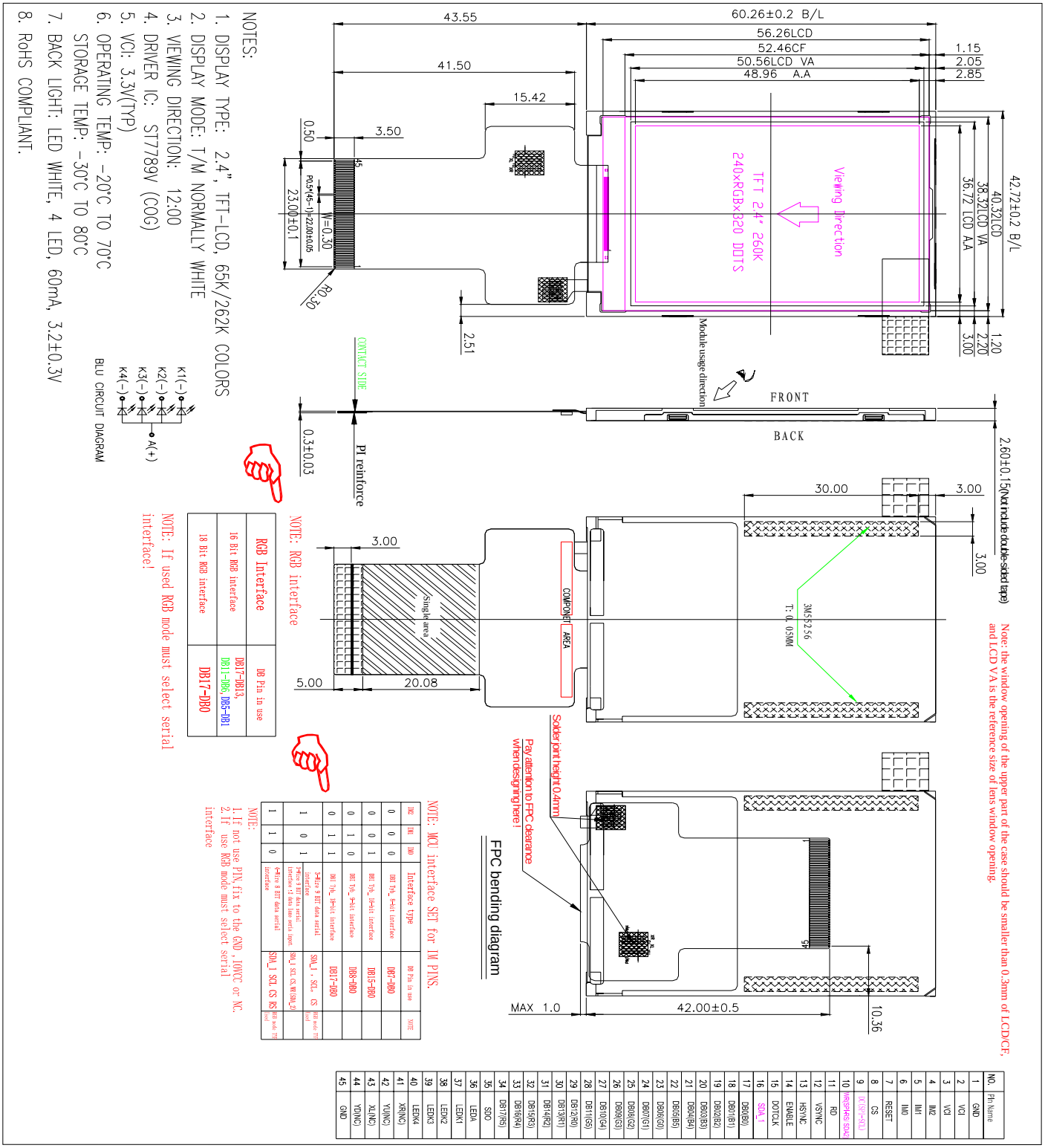
3 Pin Description

3.1 Panel Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1</td><td>GND</td><td>Ground</td></tr>
<tr><td>2</td><td>VCI</td><td>Supply voltage(3.3V)</td></tr>
<tr><td>3</td><td>VCI</td><td>Supply voltage(3.3V)</td></tr>
<tr><td>4</td><td>IM2</td><td>MCU Parallel interface bus and Serial interface select
IM2=’0’: Parallel Interface
IM2=’1’: Serial Interface</td></tr>
<tr><td>5</td><td>IM1</td><td rowspan="2"><table><tr><th>IM1</th><th>IM0</th><th>Parallel interface</th></tr><tr><td>0</td><td>0</td><td>MCU 8-bit Parallel</td></tr><tr><td>0</td><td>1</td><td>MCU 16-bit Parallel</td></tr><tr><td>1</td><td>0</td><td>MCU 9-bit Parallel</td></tr><tr><td>1</td><td>1</td><td>MCU 18-bit Parallel</td></tr></table></td></tr>
<tr><td>6</td><td>IM0</td></tr>
<tr><td>7</td><td>RESET</td><td>Active LOW Reset signal</td></tr>
<tr><td>8</td><td>CS</td><td>Chip select input pin (“LOW” enable). Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>9</td><td>DS(SCL)</td><td>This pin is used to select “Data or Command” in the parallel interface. When D/CX = ’1’, data is selected. When D/CX = ’0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4wire 8-bit serial data interface. Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>10</td><td>WR(SPI-RS,SDA2)</td><td>The data is applied on the rising edge of the SCL signal. If not used, second Data lane in 2 data lane serial interface. Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>11</td><td>RD</td><td>Serves as a read signal and MCU read data at the rising edge. Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>12</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation. Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>13</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation. Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>14</td><td>ENABLE</td><td>Data enable signal for RGB interface operation.</td></tr>
<tr><td>15</td><td>DOTCLK</td><td>Dot clock signal for RGB interface operation.
Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>16</td><td>SDA1</td><td>Dot clock signal for RGB interface operation.
Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>17-34</td><td>DB0-DB17</td><td>Dot clock signal for RGB interface operation.
Fix this pin at VCI or GND when not in use.</td></tr>
<tr><td>35</td><td>SDO</td><td>SPI interface output pin.
-The data is output on the falling edge of the SCL signal.
-If not used, let this pin open.</td></tr>
<tr><td>36</td><td>LEDA</td><td>Anode pin of backlight</td></tr>
<tr><td>37</td><td>LEDK1</td><td>Cathode pin OF backlight</td></tr>
<tr><td>38</td><td>LEDK2</td><td>Cathode pin OF backlight</td></tr>
<tr><td>39</td><td>LEDK3</td><td>Cathode pin OF backlight</td></tr>
<tr><td>40</td><td>LEDK4</td><td>Cathode pin OF backlight</td></tr>
<tr><td>41</td><td>XR(NC)</td><td></td></tr>
<tr><td>42</td><td>YD(NC)</td><td></td></tr>
<tr><td>43</td><td>XL(NC)</td><td></td></tr>
<tr><td>44</td><td>YU(NC)</td><td></td></tr>
<tr><td>45</td><td>GND</td><td>Ground</td></tr>
</table>

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles Top		-	45	-	°	
View Angles Bottom		-	20	-	°	
View Angles Left		-	45	-	°	
View Angles Right		-	45	-	°	
Response Time (25°C)	Tr + Tf	-	30	-	ms	
Uniformity		80	-	-	%	
Contrast Ratio	CR	-	500	-		
Luminance	L_V	250	-	-	cd/m²	

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Digital Supply Voltage	V_{DD}	-0.3	4.6	V
Digital interface supple Voltage	V_{DDIO}	-0.3	4.6	V
Operating Temperature	T_{OP}	-20	70	℃
Storage Temperature	T_{ST}	-30	80	℃

5.3 DC Characteristics

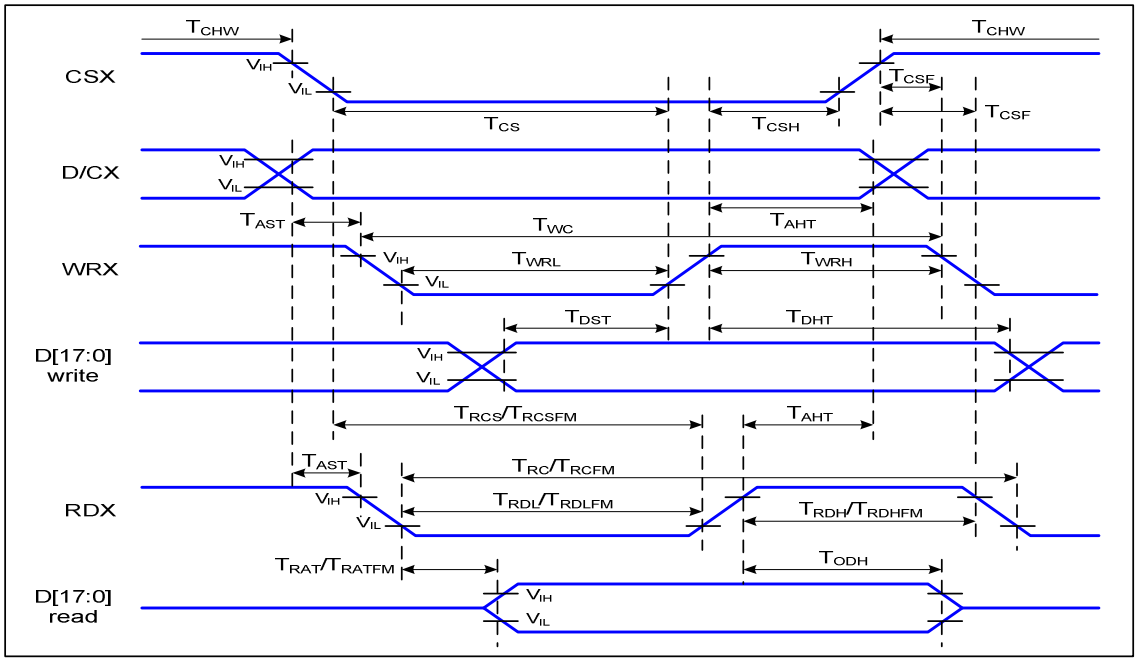
Item	Symbol	Min	Typ.	Max	Unit
Supply Voltage For Logic	VDD	2.4	3.3	4.2	V
Digital interface supple Voltage	VDDIO	1.65	3.3	4.2	V
Digital Operation Current	IDD	-	4	-	mA
Low Level Input Voltage	V_{IL}	GND	-	0.3VDDIO	V
High Level Input Voltage	V_{IH}	0.7VDDIO	-	VDDIO	V
Low Level Output Voltage	V_{OL}	GND		0.2VDDIO	V
High Level Output Voltage	V_{OH}	0.8VDDIO		VDDIO	V

5.4 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Backlight Forward Current	I_F	60	80	-	mA	
Backlight Forward Voltage	V_F	-	3.2	-	V	
LCM Luminance	L_V	250	-	-	cd/m²	I_F=80mA
Uniformity	AVg	80	-	-	%	

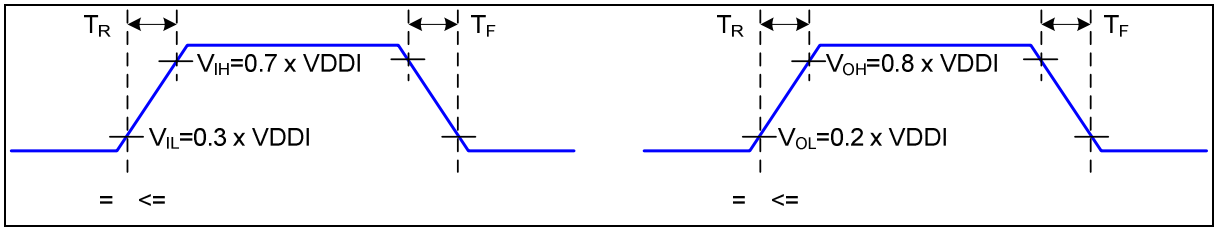
5.5 AC Characteristics

5.5.1 8080-Series MPU Parallel Interface Timing Characteristics

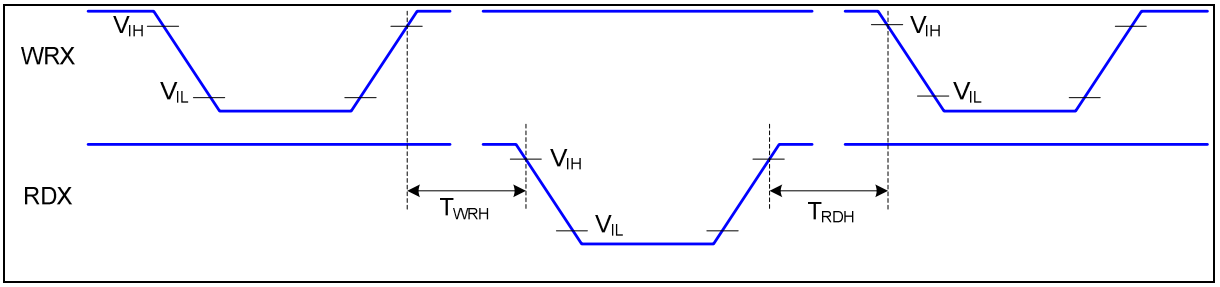


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 ℃

Signal	Symbol	Description	Min	Max	Unit	Note
D/CX	T_{AST}	Address setup time	0	-	ns	
	T_{AHT}	Address hold time(Write/Read)	10	-	ns	
CSX	T_{CHW}	CSH "H" Pulse Width	0	-	ns	
	T_{CS}	Chip select setup time(Write)	10	-	ns	
	T_{RCS}	Chip select setup time(Read ID)	45	-	ns	
	T_{RCSFM}	Chip select setup time(Read FM)	355	-	ns	
	T_{CSF}	Chip select wait time(Write/Read)	10	-	ns	
	T_{CSH}	Chip select hold time	10	-	ns	
WRX	T_{WC}	Write cycle	66	-	ns	
	T_{WRH}	Control pulse H duration	15	-	ns	
	T_{WRL}	Control pulse L duration	15	-	ns	
RDX	T_{RC}	Read cycle (ID)	160	-	ns	When read ID data
	T_{RDH}	Control pulse H duration(ID)	90	-	ns	
	T_{RDL}	Control pulse L duration(ID)	45	-	ns	
RDX	T_{RCFM}	Read cycle (FM)	450	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse H duration(FM)	90	-	ns	
	T_{RDLFM}	Control pules L duration(FM)	355	-	ns	
D[17…0]	T_{DST}	Data setup time	10	-	ns	ForCL=30pF
	T_{DHT}	Data hold time	10	-	ns	
	T_{RAT}	Read access time(ID)	-	40	ns	
	T_{RATFM}	Read access time(FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	



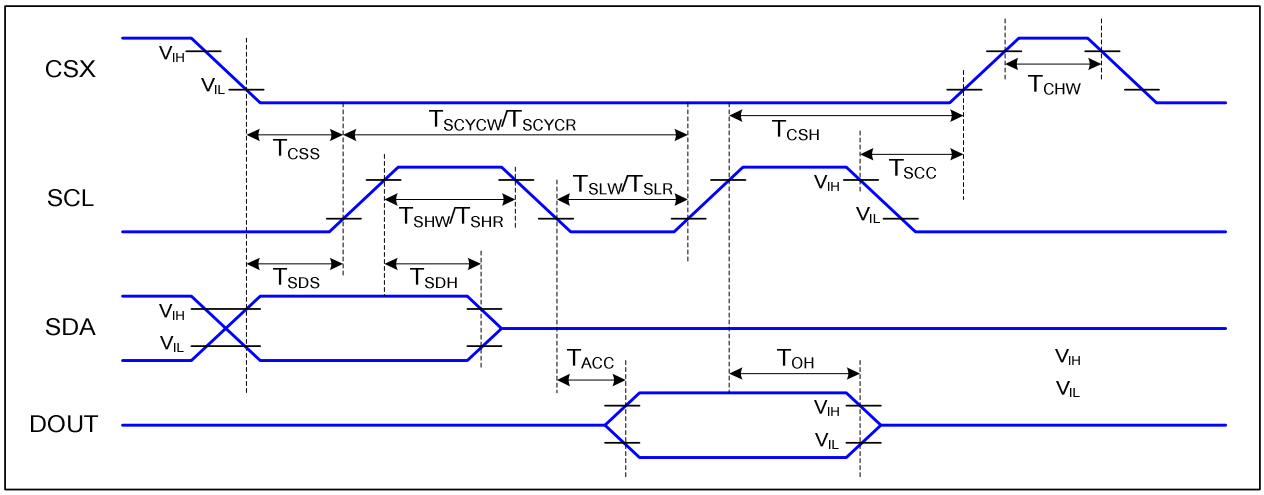
Rising and Falling Timing for I/O Signal



Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.5.2 3-wire Serial Interface Timing Characteristics:

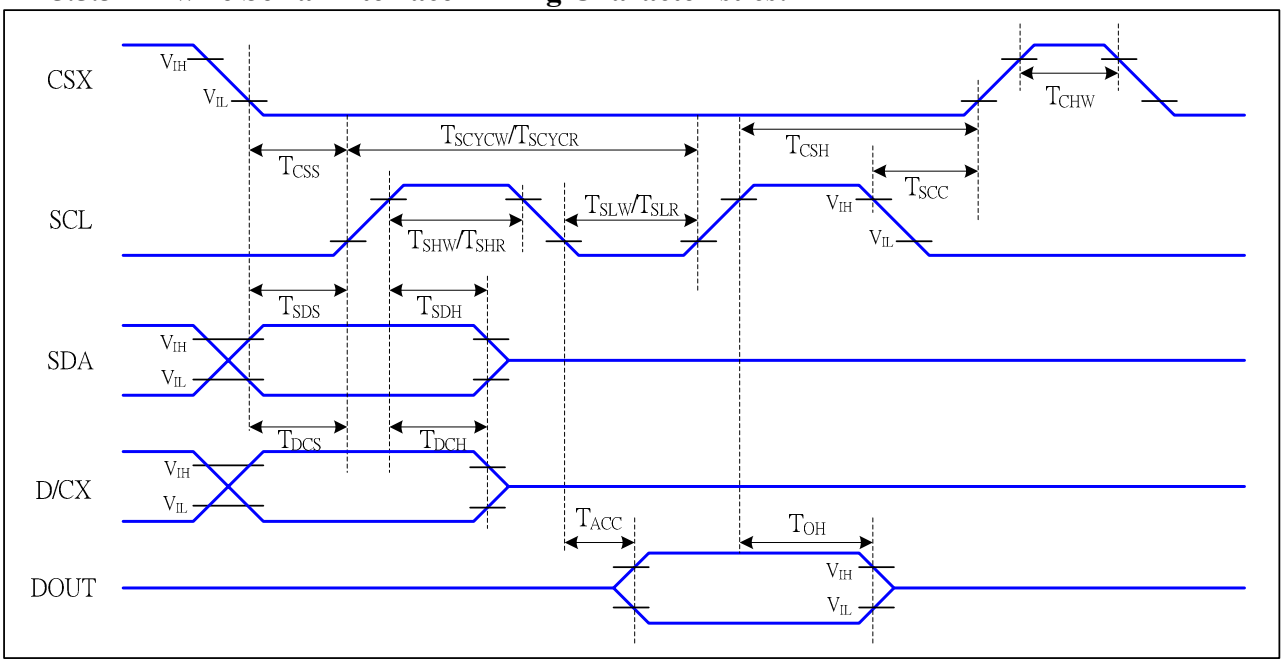


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Description	Min	Max	Unit	Remark
CSX	T_{CSS}	Chip Select Setup Time (Write)	15	-	ns	
	T_{CSH}	Chip Select Hold Time (Write)	15	-	ns	
	T_{CSS}	Chip Select Setup Time (Read)	60	-	ns	
	T_{SCC}	Chip Select Hold Time (Read)	65	-	ns	
	T_{CHW}	Chip Select "H" Pulse Width	40	-	ns	
SCL	T_{SCYCW}	Serial Clock Cycle (Write)	66	-	ns	
	T_{SHW}	SCL "H" Pulse Width (Write)	15	-	ns	
	T_{SLW}	SCL "L" Pulse Width (Write)	15	-	ns	
	T_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	
	T_{SHR}	SCL "H" Pulse Width (Read)	60	-	ns	
	T_{SLR}	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	T_{DCS}	D/CX Setup Time	10	-	ns	
	T_{DCH}	D/CX Hold Time	10	-	ns	
SDA (DIN)	T_{SDS}	Data Setup Time	10	-	ns	
	T_{SDH}	Data Hold Time	10	-	ns	
DOUT	T_{ACC}	Access Time	10	50	ns	For Maximum CL=30pF For Minimum CL=8pF
	T_{OH}	Output Disable Time	15	50	ns	

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.5.3 4-wire Serial Interface Timing Characteristics:

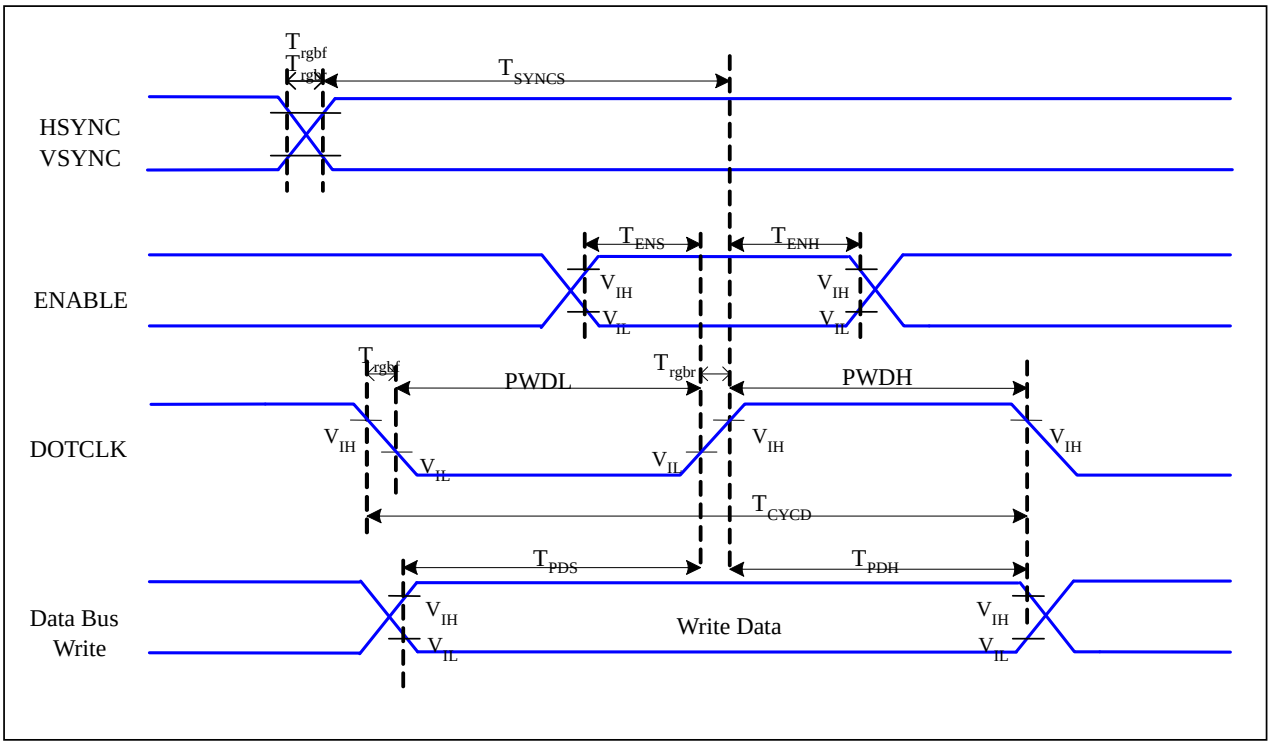


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Description	Min	Max	Unit	Remark
CSX	T_{CSS}	Chip Select Setup Time (Write)	15	-	ns	
	T_{CSH}	Chip Select Hold Time (Write)	15	-	ns	
	T_{CSS}	Chip Select Setup Time (Read)	60	-	ns	
	T_{SCC}	Chip Select Hold Time (Read)	65	-	ns	
	T_{CHW}	Chip Select "H" Pulse Width	40	-	ns	
SCL	T_{SCYCW}	Serial Clock Cycle (Write)	66	-	ns	-Write Command & Data Ram
	T_{SHW}	SCL "H" Pulse Width (Write)	15	-	ns	
	T_{SLW}	SCL "L" Pulse Width (Write)	15	-	ns	
	T_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	-Read Command & Data Ram
	T_{SHR}	SCL "H" Pulse Width (Read)	60	-	ns	
	T_{SLR}	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	T_{DCS}	D/CX Setup Time	10	-	ns	
	T_{DCH}	D/CX Hold Time	10	-	ns	
SDA (DIN)	T_{SDS}	Data Setup Time	10	-	ns	
	T_{SDH}	Data Hold Time	10	-	ns	
DOUT	T_{ACC}	Access Time	10	50	ns	For Maximum CL=30pF For Minimum CL=8pF
	T_{OH}	Output Disable Time	15	50	ns	

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

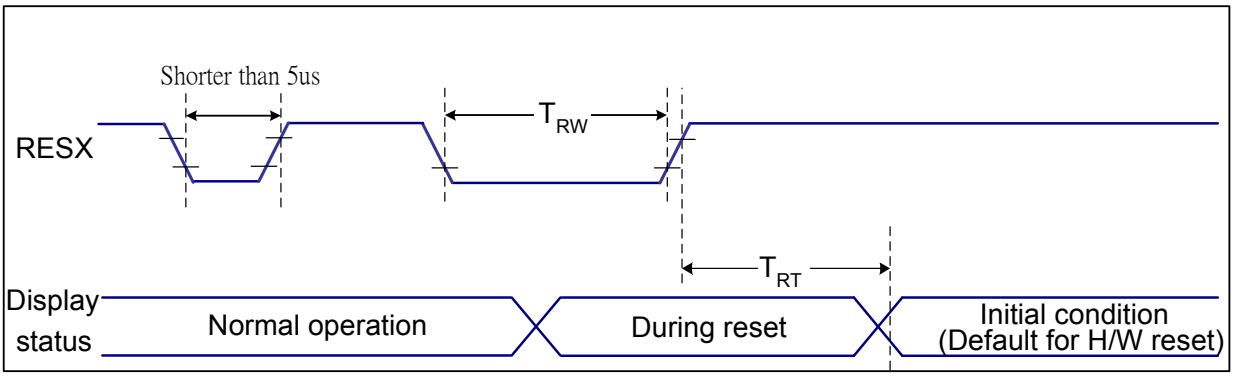
5.5.4 RGB Interface Characteristics:



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Signal	Symbol	Description	Min	Max	Unit	Remark
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{POH}	PDData Hold Time	50	-	ns	

5.5.5 Display RESET Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

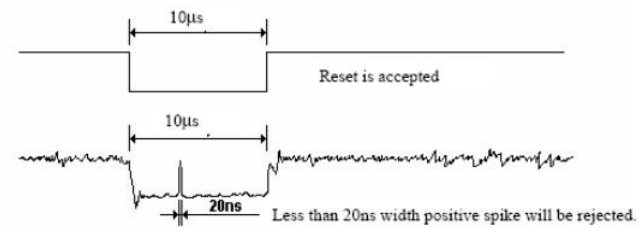
Related Pins	Symbol	Parameter	Min	Max	Unit
REXS	TRW	Reset pulse duration	10	-	µs
	TRT	Reset cancel	-	5(Note 1,5)	ms
			-	120(Note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

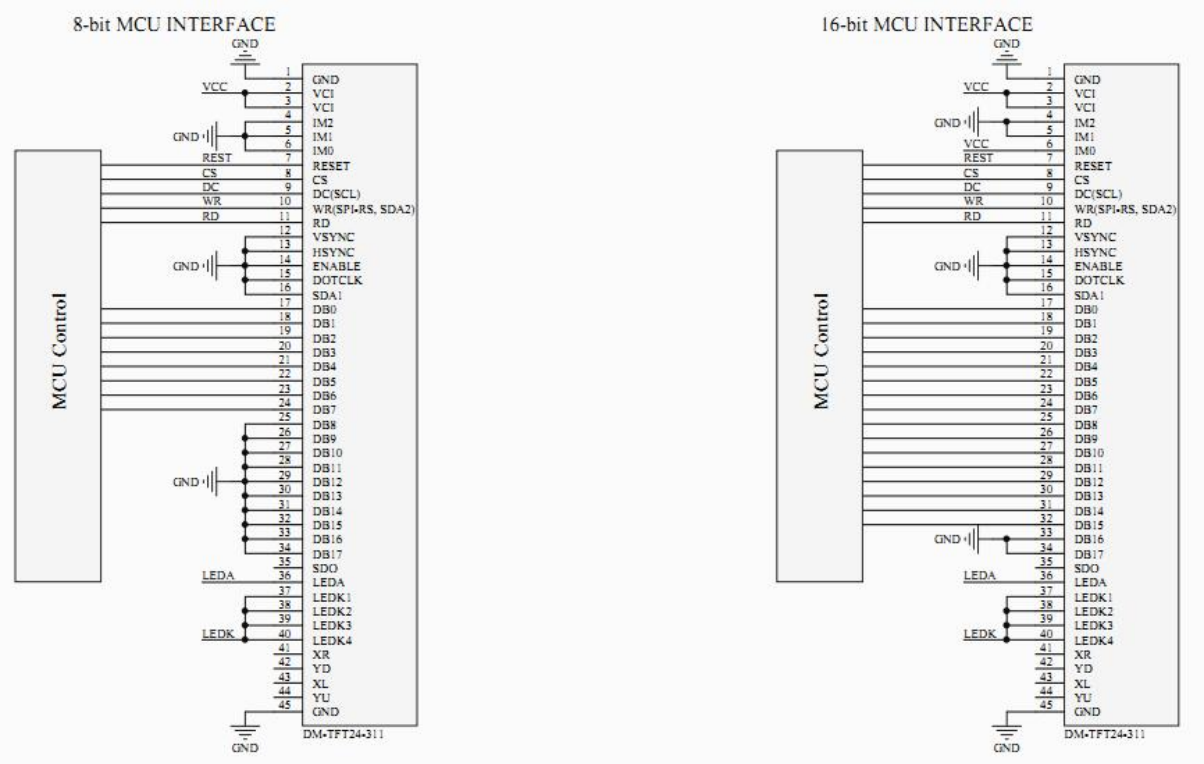
RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset Starts

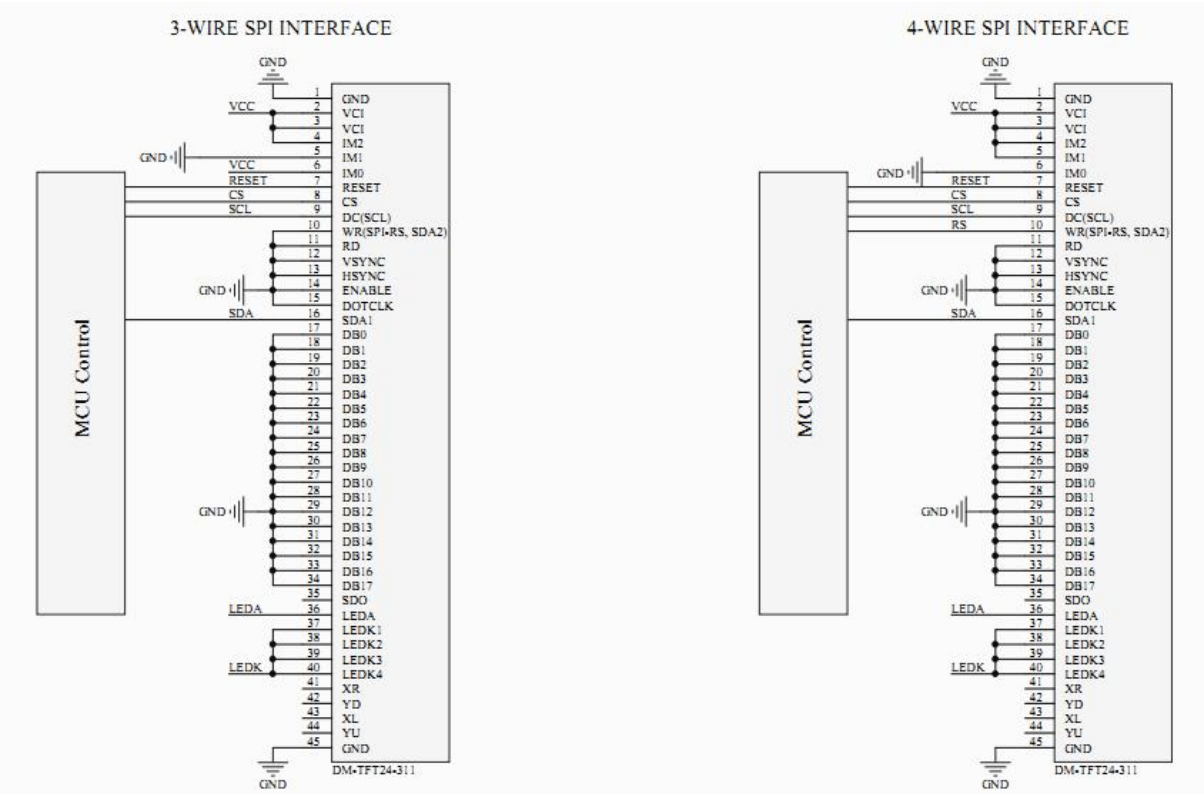
3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



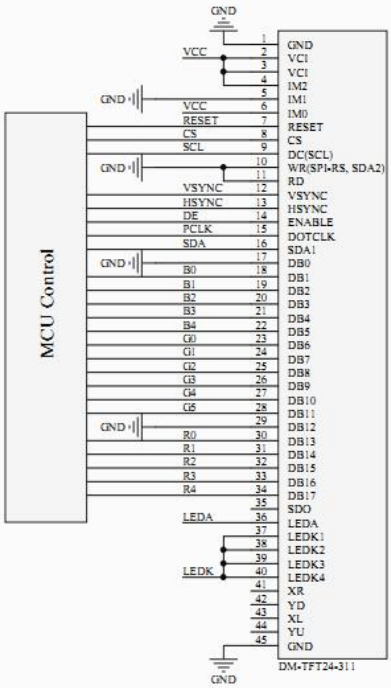
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6 Application Circuit Reference

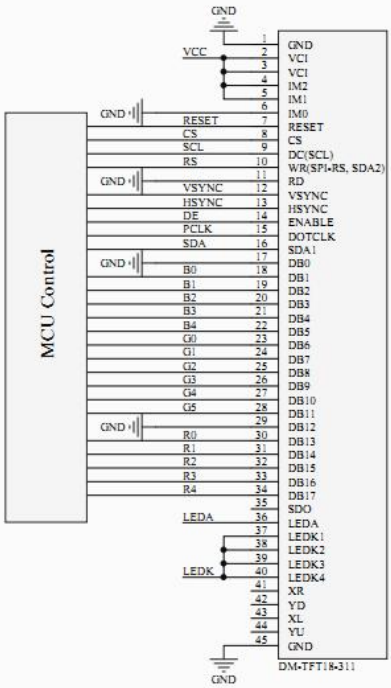




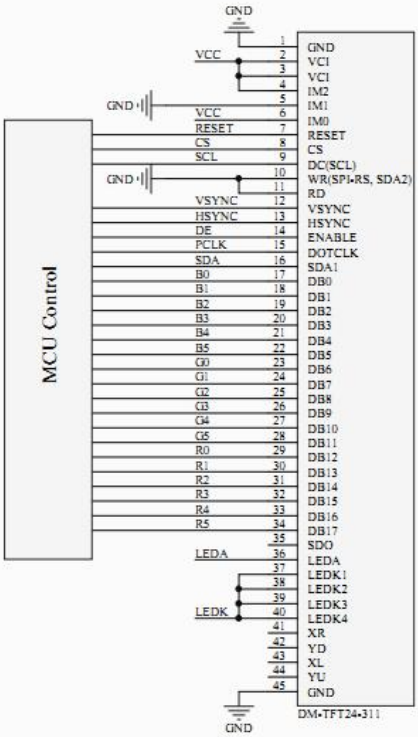
3-WIRE SPI AND 16-BIT RGB



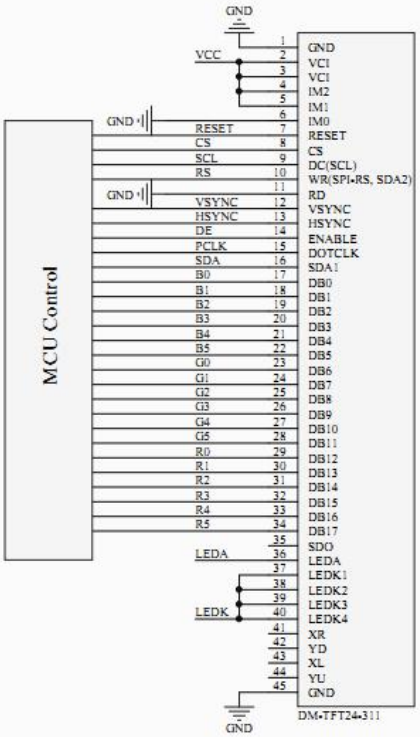
4-WIRE SPI AND 16-BIT RGB



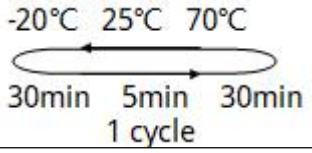
3-WIRE SPI AND 18-BIT RGB



4-WIRE SPI AND 18-BIT RGB



7 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-20°C/70°C 10 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

8 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"