

DM-TFT23-487

2.36"320x240TRANSMISSIVETFTLCD-RGB

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General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.36" TFT-LCD contains 320x240 pixels, and can display up to 262K colors.

* Features

-Low Input Voltage: 3.3V(TYP)

-Display Colors of TFT LCD: 65K/262K colors

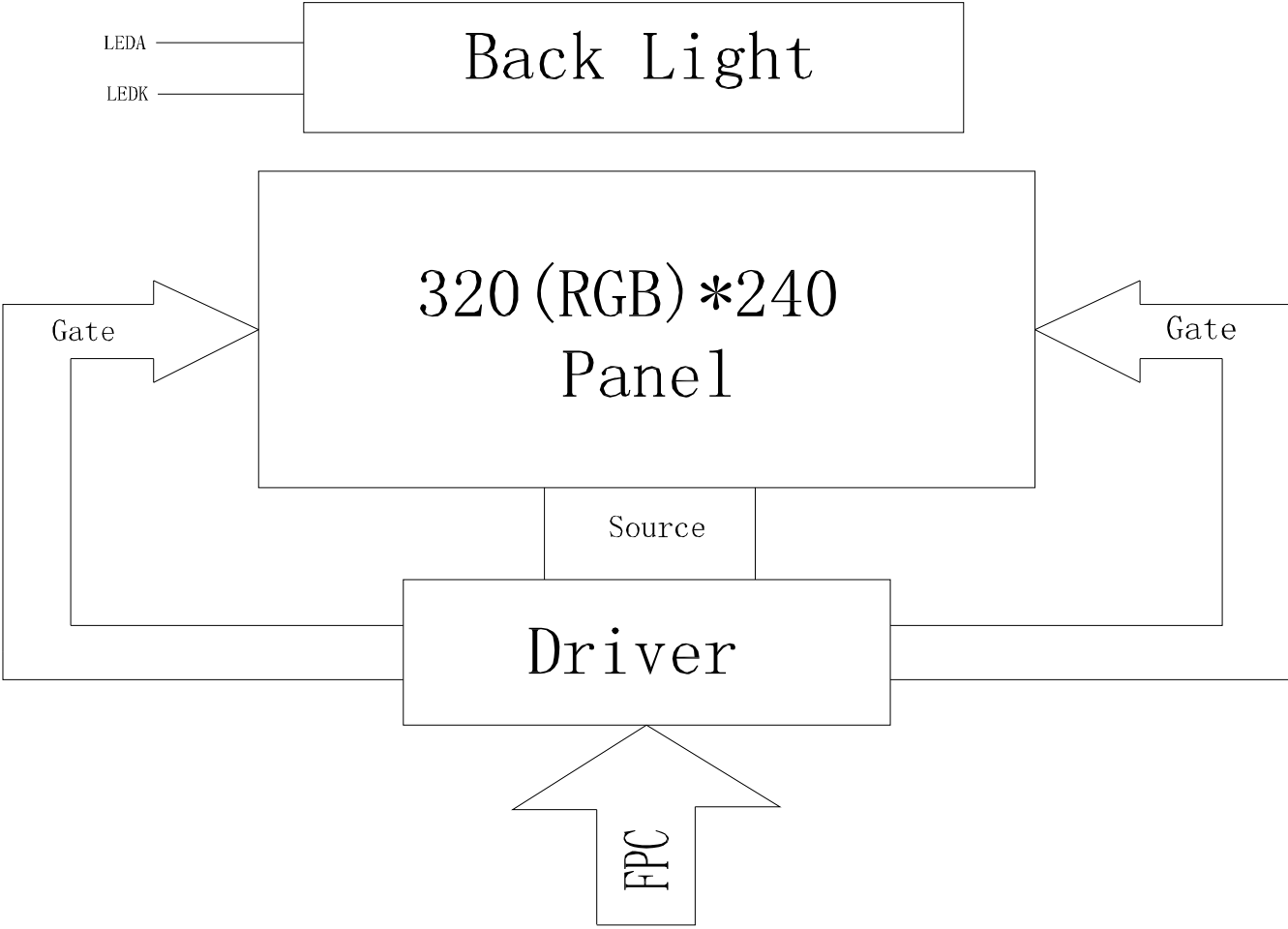
-RGB Interface: 8/9/16/18Bit MCU, 3/4SPI+16/18Bit RGB

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	46.75(H)*35.06(V) (2.36inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65/262K	colors	-
Number of pixels	320(RGB)*240	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1461(H)*0.1461(V)	mm	-
Viewing angle	12:00	o'clock	-
Controller IC	ILI9342C	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

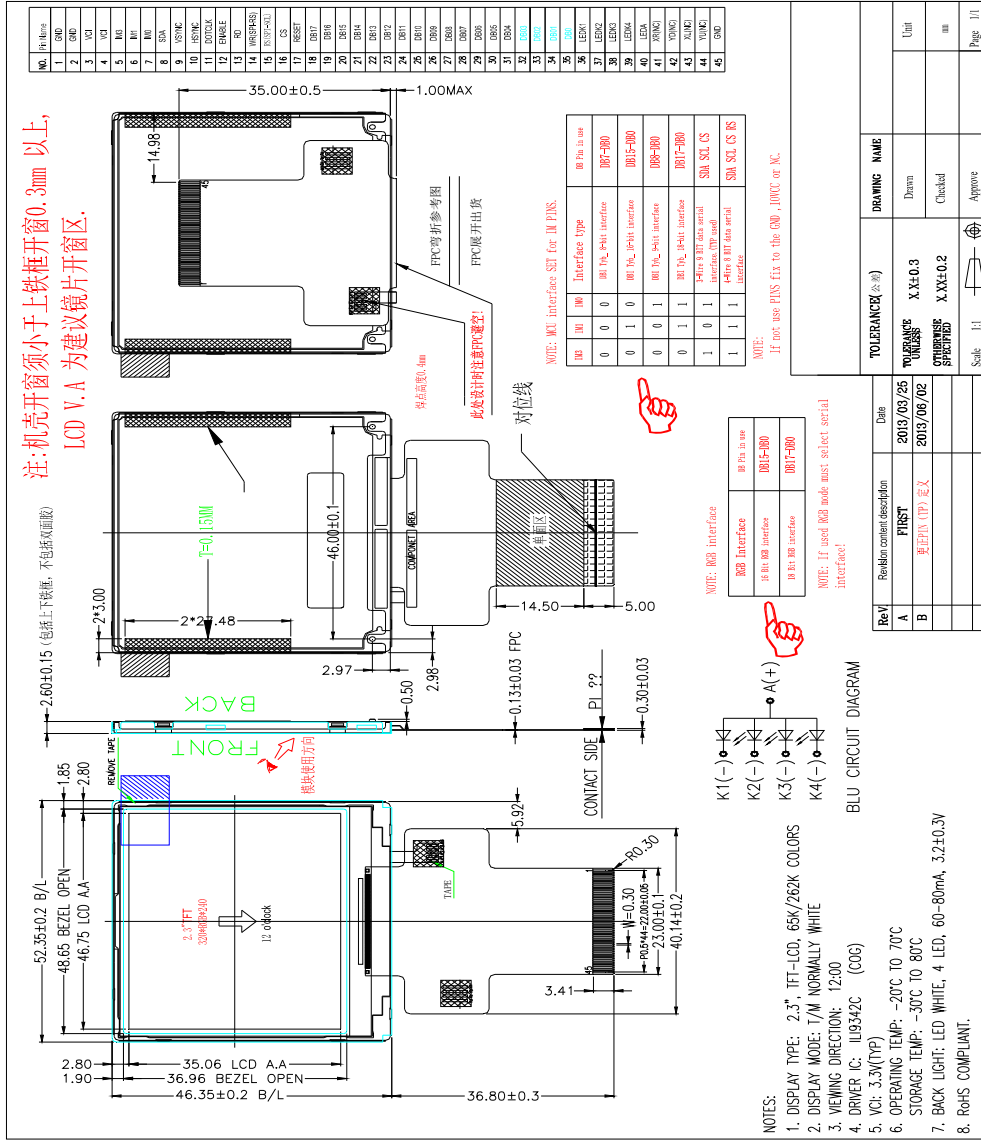
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		52.35		mm	-
	Vertical(V)		46.35		mm	-
	Depth(D)		2.60		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	GND	Ground.	P
3	VCI	Supply voltage(3.3V).	P
4	VCI	Supply voltage(3.3V).	P
5	IM3	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND.	I
6	IM1		I
7	IM0		I
8	SDA	The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND when not in use.	I
9	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
10	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
11	DOTCLK	Dot clock signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
12	ENABLE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
13	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.	I
14	WR(SPI_RS)	Serves as a write signal and writes data at the rising edge. 4-line system (D/CX): Serves as command or parameter select. fix this pin at VCI or GND when not in use.	I
15	RS(SPI_SCL)	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. fix this pin at VCI or GND when not in use.	I
16	CS	Chip select input pin ("Low" enable). fix this pin at VCI or GND when not in use.	I
17	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I

18-35	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
36	LEDK1	Cathode pin OF backlight	P
37	LEDK2	Cathode pin OF backlight	P
38	LEDK3	Cathode pin OF backlight	P
39	LEDK4	Cathode pin OF backlight	P
40	LEDA	Anode pin of backlight	P
41	XR(NC)	Touch panel Right Glass Terminal	A/D
42	YD(NC)	Touch panel Bottom Film Terminal	A/D
43	XL(NC)	Touch panel LIFT Glass Terminal	A/D
44	YU(NC)	Touch panel Top Film Terminal	A/D
45	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (without Polarizer)	T(%)	—	—	15.20%	—	—	
Contrast Ratio	CR	$\Theta=0$	400	500	—	—	(1)(2)
Response time	Rising	T_R	—	4	8	msec	(1)(3)
	Falling	T_F	—	12	20		
Color gamut	S(%)			50		%	
Color chromaticity (CIE1931)	White	W_x		0.283	0.303	0.323	(1)(4) CF glass
		W_y		0.304	0.324	0.344	
	Red	R_x		0.589	0.609	0.629	
		R_y		0.310	0.330	0.350	
	Green	G_x		0.267	0.287	0.307	
		G_y		0.507	0.527	0.547	
	Blue	B_x		0.127	0.147	0.167	
B_y			0.118	0.138	0.158		
Viewing angle	Hor.	Θ_L	CR>10	60	70	—	Viewing Angle base on using EWV Polarizer , Reference Only
		Θ_R		60	70	—	
	Ver.	Θ_U		60	70	—	
		Θ_D		50	60	—	
Optima View Direction	12 O'clock						(5)

4.2 Measuring Condition

■ Measuring surrounding : dark room

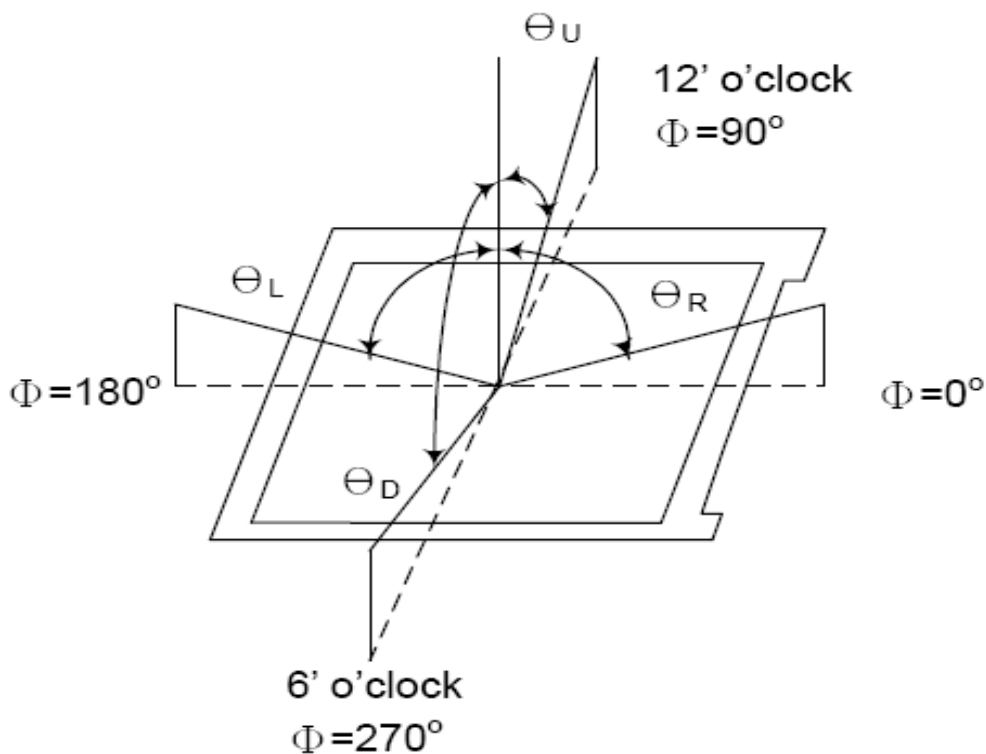
■ Ambient temperature : $25 \pm 2^\circ\text{C}$

■ 15min. warm-up time

4.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :

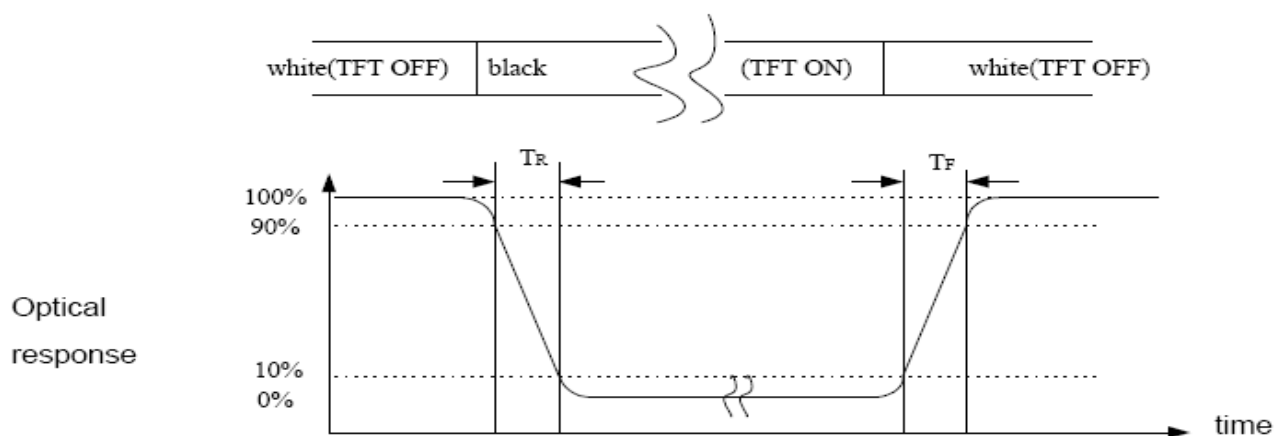
measured at the center point of panel

$$\text{CR} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

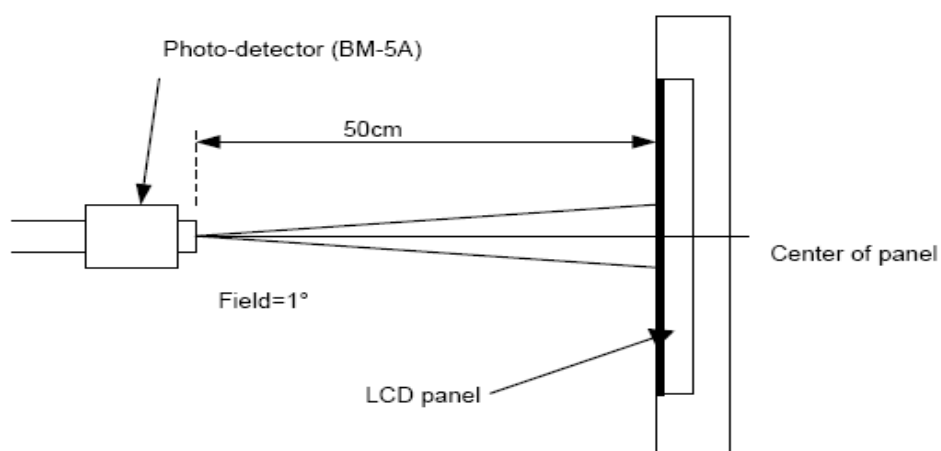
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.2	V
Digital interface supply Voltage	VDDIO	-0.3	VDD	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

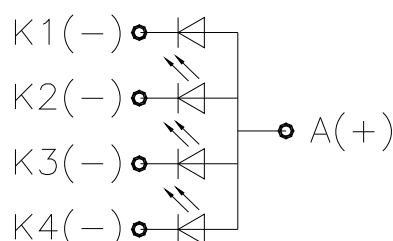
5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.6	3.3	4.2	V	
Digital interface supply Voltage	VDDIO	1.8	3.3	4.2	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V _{IH}	0.7V _{DDIO}		V _{DDIO}	V	
	V _{IL}	GND		0.3V _{DDIO}	V	
Level output voltage	V _{OH}	0.8V _{DDIO}		V _{DDIO}	V	
	V _{OL}	GND		0.2V _{DDIO}	V	

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4chips White LED

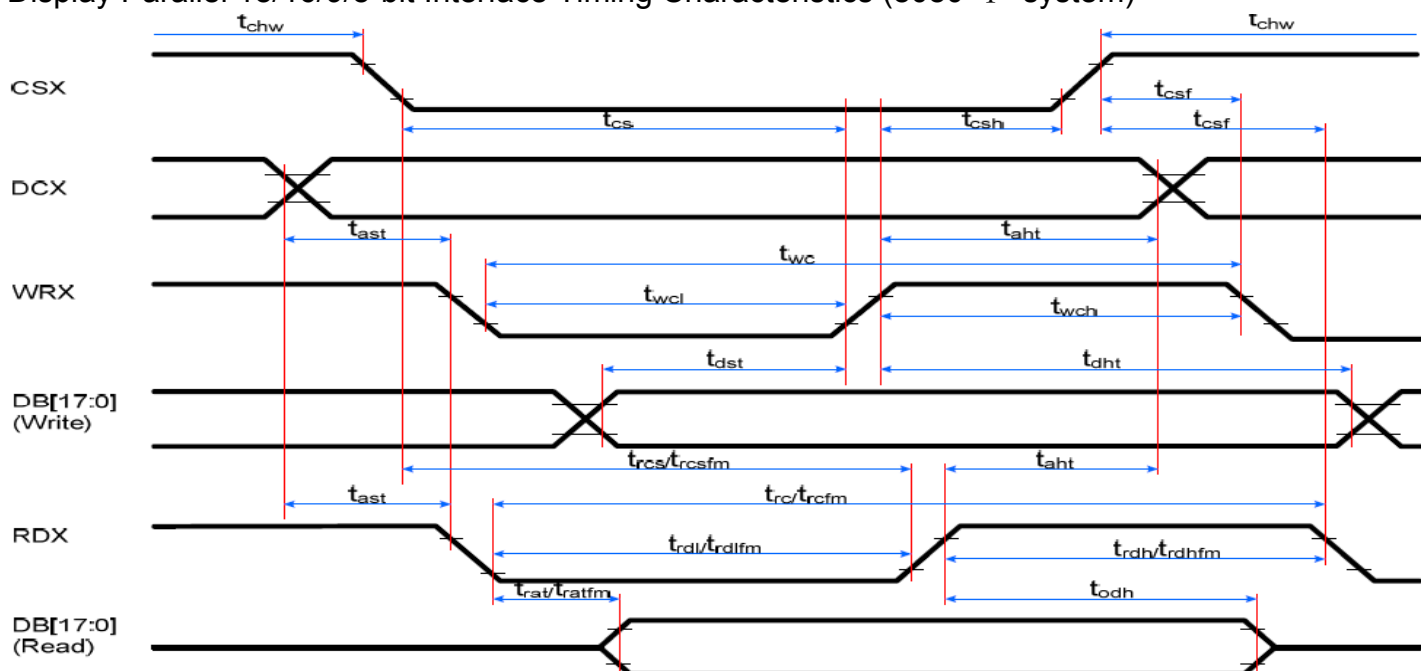
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	60	80	--	mA	
Forward Voltage	V _F	--	3.2	--	V	
LCM Luminance	L _V	300	--	--	cd/m ²	I _F =80mA
Uniformity	AV _g	80	--	--	%	



BLU CIRCUIT DIAGRAM

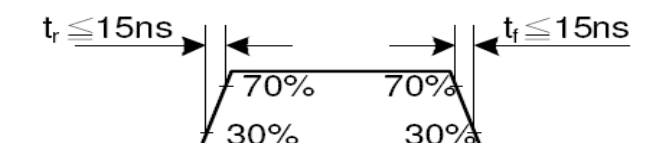
6. AC Characteristic

6.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)

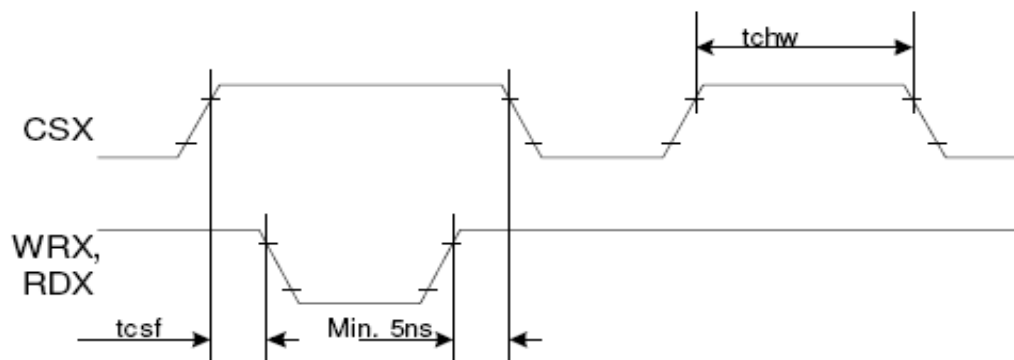


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ahh}	Address hold time (Write/Read)	10	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{r_{cs}}	Chip Select setup time (Read ID)	45	-	ns	
	t _{r_{csfm}}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{r_{cfm}}	Read Cycle (FM)	450	-	ns	
	t _{r_{dhfm}}	Read Control H duration (FM)	90	-	ns	
	t _{r_{dlfm}}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{r_{dh}}	Read Control pulse H duration	90	-	ns	
	t _{r_{dl}}	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

Note: $T_a = -30$ to 70 °C, $IOVCC=1.65V$ to $2.8V$, $V_{CI}=2.6V$ to $3.3V$, $GND=0V$

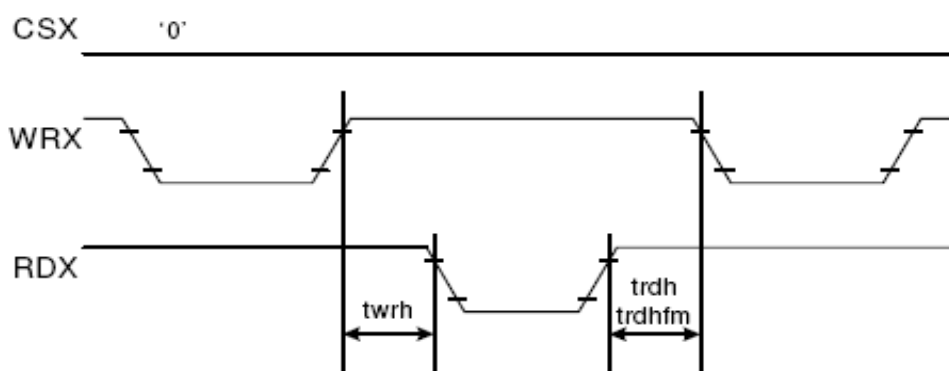


CSX timings :



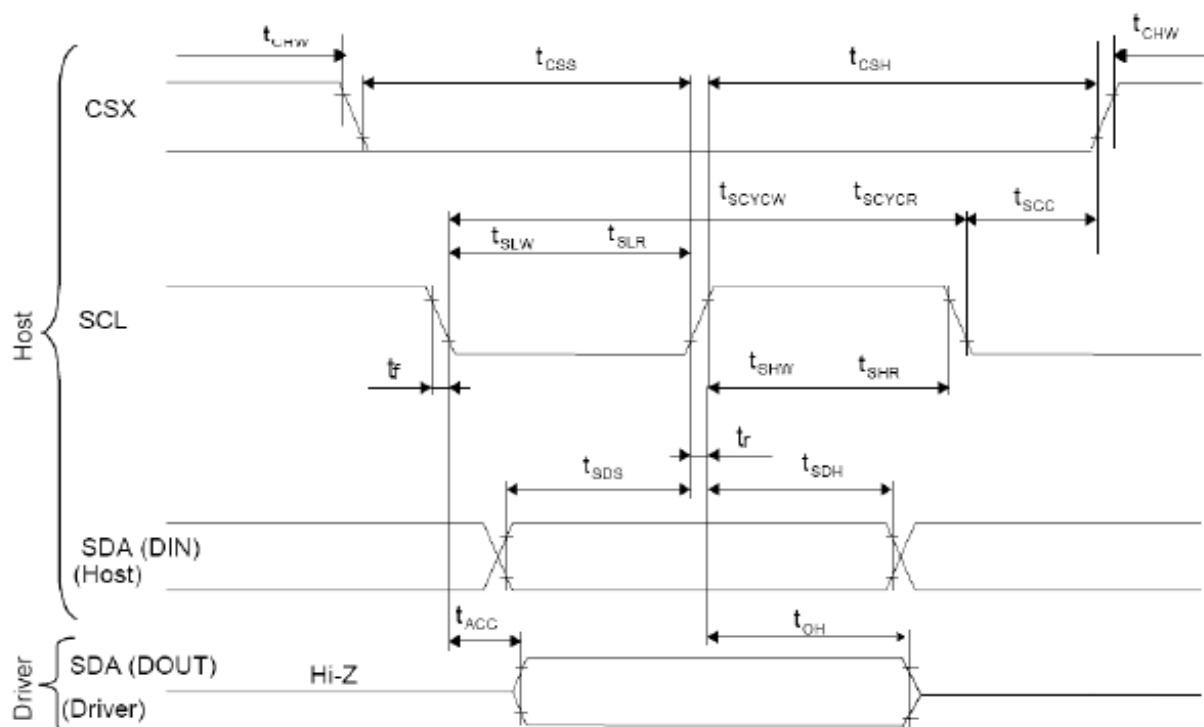
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



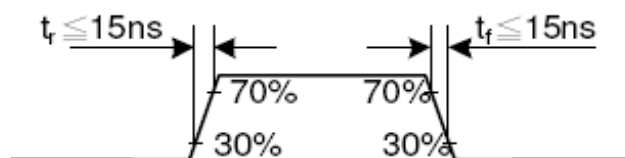
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

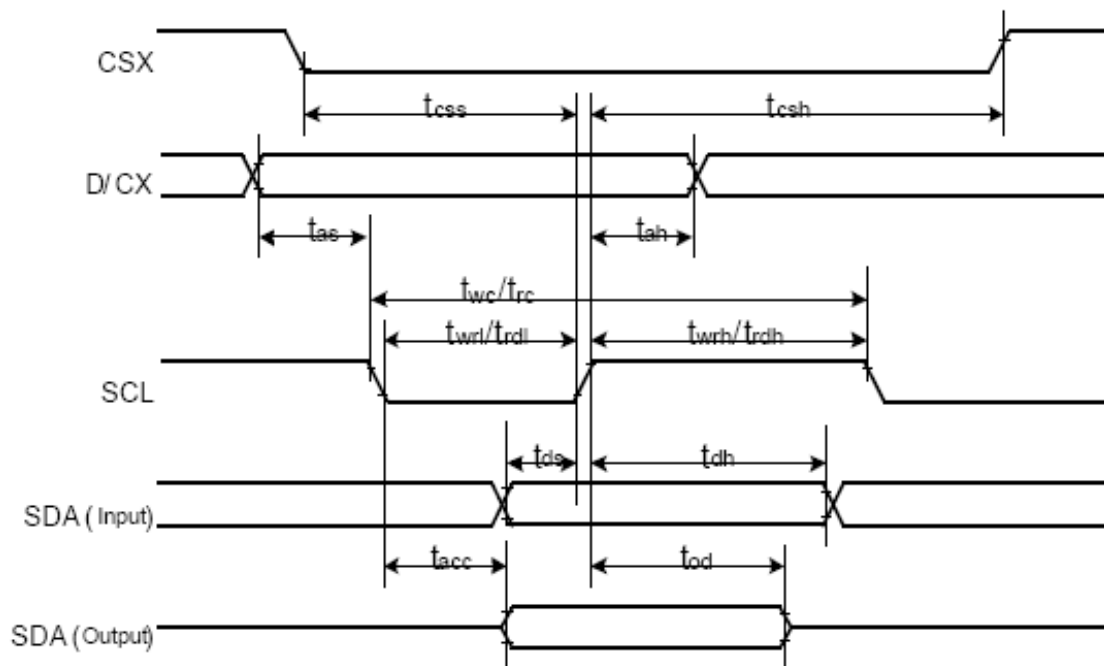


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	35	-	ns	
	tslw	SCL "L" Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tch	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time(write)	30	-	ns	
	tch		30	-	ns	

Note: $T_a = 25\text{ }^\circ\text{C}$, $IOVCC=1.65\text{V to }2.8\text{V}$, $VCI=2.6\text{V to }3.3\text{V}$, $AGND=GND=0\text{V}$

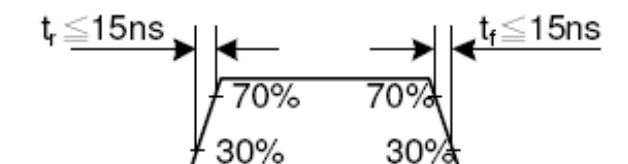


6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

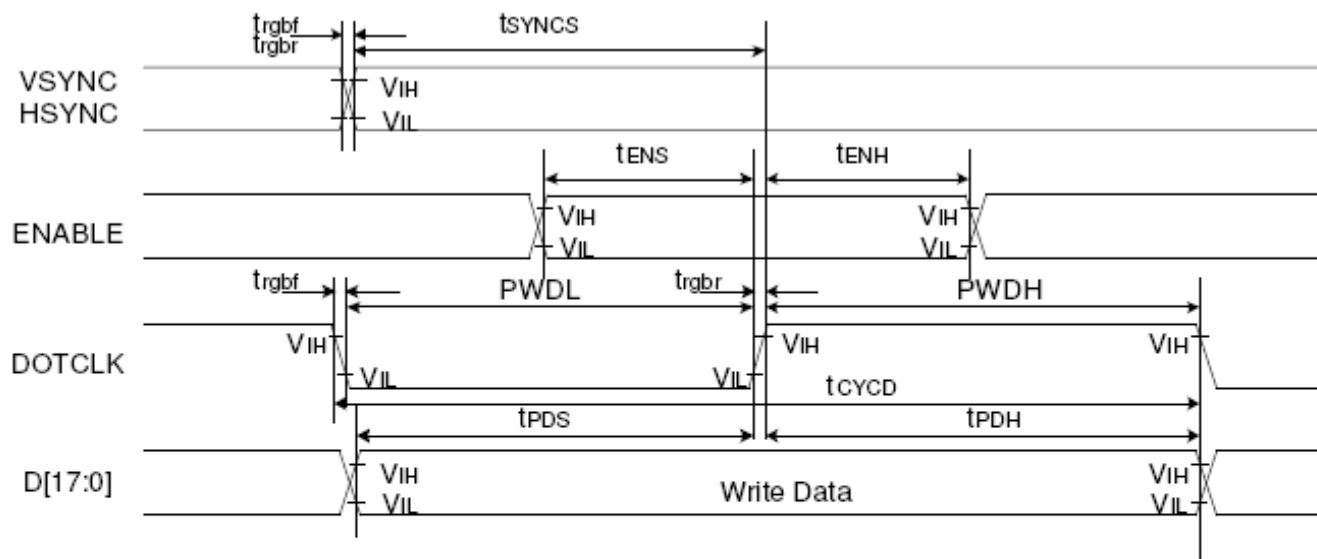


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	30	-	ns	
	tcsh	Chip select hold time (write)	30	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	twrh	SCL "H" pulse width (Write)	35	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	twrl	SCL "L" pulse width (Write)	35	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	-	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: $T_a = 25\text{ }^\circ\text{C}$, $IOVCC=1.65\text{V to }2.8\text{V}$, $VCI=2.6\text{V to }3.3\text{V}$, $AGND=GND=0\text{V}$

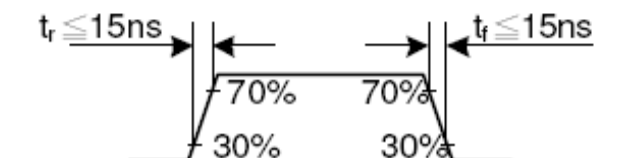


6.4 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	100	-	ns	
	t_{rgbv}, t_{rgbv}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbv}, t_{rgbv}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70 °C, $IOVCC=1.65V$ to $2.8V$, $VCI=2.6V$ to $3.3V$, $AGND=GND=0V$



7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

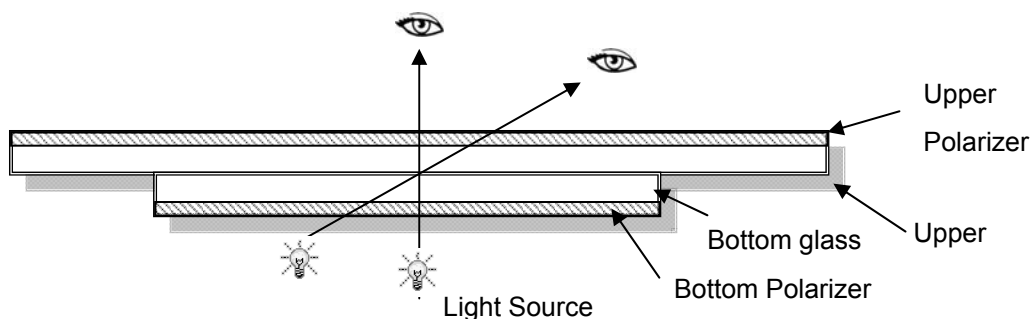
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

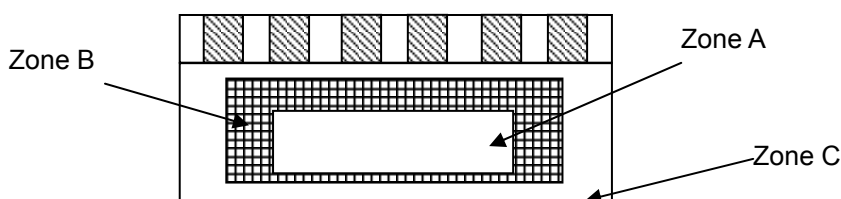
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

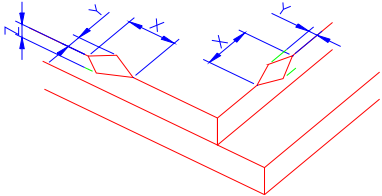
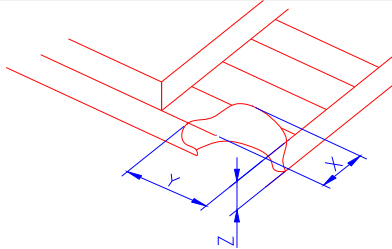
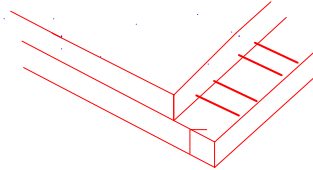
AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

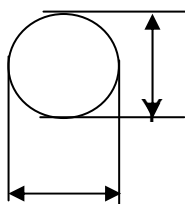
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="868 640 1441 792"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>≤3.0mm</td> <td><Inner border line of the seal</td> <td>≤T</td> </tr> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table border="1" data-bbox="932 1128 1377 1229"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 <p style="text-align: center;">Crack Not allowed</p>							

2.0

Spot defect



X

$$\Phi = (X+Y)/2$$

① light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.10$	Ignore		
$0.10 < \Phi \leq 0.20$	3(distance $\geq 10\text{mm}$)		
$0.20 < \Phi \leq 0.25$	2		
$\Phi > 0.25$	0		

② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)

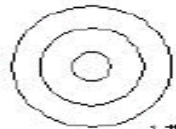


Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore		
$0.10 < \Phi \leq 0.20$	3(distance $\geq 10\text{mm}$)		
$0.20 < \Phi \leq 0.30$	2		
$\Phi > 0.30$	0		

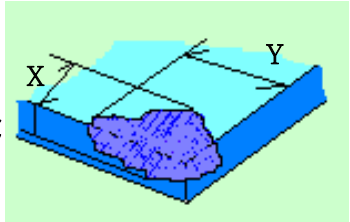
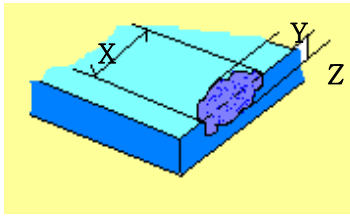
③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		
$0.3 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.5$	0		

Line defect
(LCD/TP
/Polarizer
black/white
line, scratch,
stain)

Width(mm)	Length(mm)	Acceptable Qty		
		A	B	C
$\Phi \leq 0.03$	Ignore	Ignore		
$0.03 < W \leq 0.05$	$L \leq 3.0$	$N \leq 2$		
$0.05 < W \leq 0.08$	$L \leq 2.0$	$N \leq 2$		
$0.08 < W$	Define as spot defect			

3.0	Polarizer Bubble	<table border="1"> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> <tr> <td>$\Phi \leq 0.2$</td> <td colspan="2">Ignore</td> <td rowspan="4">Ignore</td> </tr> <tr> <td>$0.2 < \Phi \leq 0.4$</td> <td colspan="2">3 (distance ≥ 10 m)</td> </tr> <tr> <td>$0.4 < \Phi \leq 0.6$</td> <td colspan="2">2</td> </tr> <tr> <td>$0.6 < \Phi$</td> <td colspan="2">0</td> </tr> </table>			Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore		Ignore	$0.2 < \Phi \leq 0.4$	3 (distance ≥ 10 m)		$0.4 < \Phi \leq 0.6$	2		$0.6 < \Phi$	0		
		Zone Size (mm)	Acceptable Qty																						
			A	B	C																				
		$\Phi \leq 0.2$	Ignore		Ignore																				
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$0.4 < \Phi \leq 0.6$	2																								
$0.6 < \Phi$	0																								
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.																							
5.0	TP Related	TP bubble/ accidented spot	<table border="1"> <tr> <th rowspan="2">Size Φ(mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> <tr> <td>$\Phi \leq 0.1$</td> <td colspan="2">Ignore</td> <td rowspan="4">Ignore</td> </tr> <tr> <td>$0.1 < \Phi \leq 0.25$</td> <td colspan="2">3 (distance \geq</td> </tr> <tr> <td>$0.25 < \Phi \leq 0.3$</td> <td colspan="2">2</td> </tr> <tr> <td>$0.3 < \Phi$</td> <td colspan="2">0</td> </tr> </table>			Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore		Ignore	$0.1 < \Phi \leq 0.25$	3 (distance \geq		$0.25 < \Phi \leq 0.3$	2		$0.3 < \Phi$	0	
			Size Φ (mm)	Acceptable Qty																					
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			$0.1 < \Phi \leq 0.25$	3 (distance \geq																					
$0.25 < \Phi \leq 0.3$	2																								
$0.3 < \Phi$	0																								
Assembly deflection	beyond the edge of backlight ≤ 0.15 mm																								
Newton Ring	<p>Newton Ring area $> 1/3$ TP area NG</p> <p>Newton Ring area $\leq 1/3$ TP area OK</p>	 1 规律性  2 非规律性  似牛顿环																							

		TP corner broken X : length Y : width Z : height	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>$X \leq 3.0\text{mm}$</td> <td>$Y \leq 3.0\text{mm}$</td> <td>$Z < \text{LCD thickness}$</td> </tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	$X \leq 3.0\text{mm}$	$Y \leq 3.0\text{mm}$	$Z < \text{LCD thickness}$	
X	Y	Z								
$X \leq 3.0\text{mm}$	$Y \leq 3.0\text{mm}$	$Z < \text{LCD thickness}$								
		TP edge broken X : length Y : width Z : height	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>$X \leq 6.0\text{mm}$</td> <td>$Y \leq 2.0\text{mm}$</td> <td>$Z < \text{LCD thickness}$</td> </tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	$X \leq 6.0\text{mm}$	$Y \leq 2.0\text{mm}$	$Z < \text{LCD thickness}$	
X	Y	Z								
$X \leq 6.0\text{mm}$	$Y \leq 2.0\text{mm}$	$Z < \text{LCD thickness}$								

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20°C, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	60°C, 90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20°C ↔ 70°C, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80°C, 96HR	3ea	pass	-
Low Temperature Storage test	- 30°C, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66 _{cm} (MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

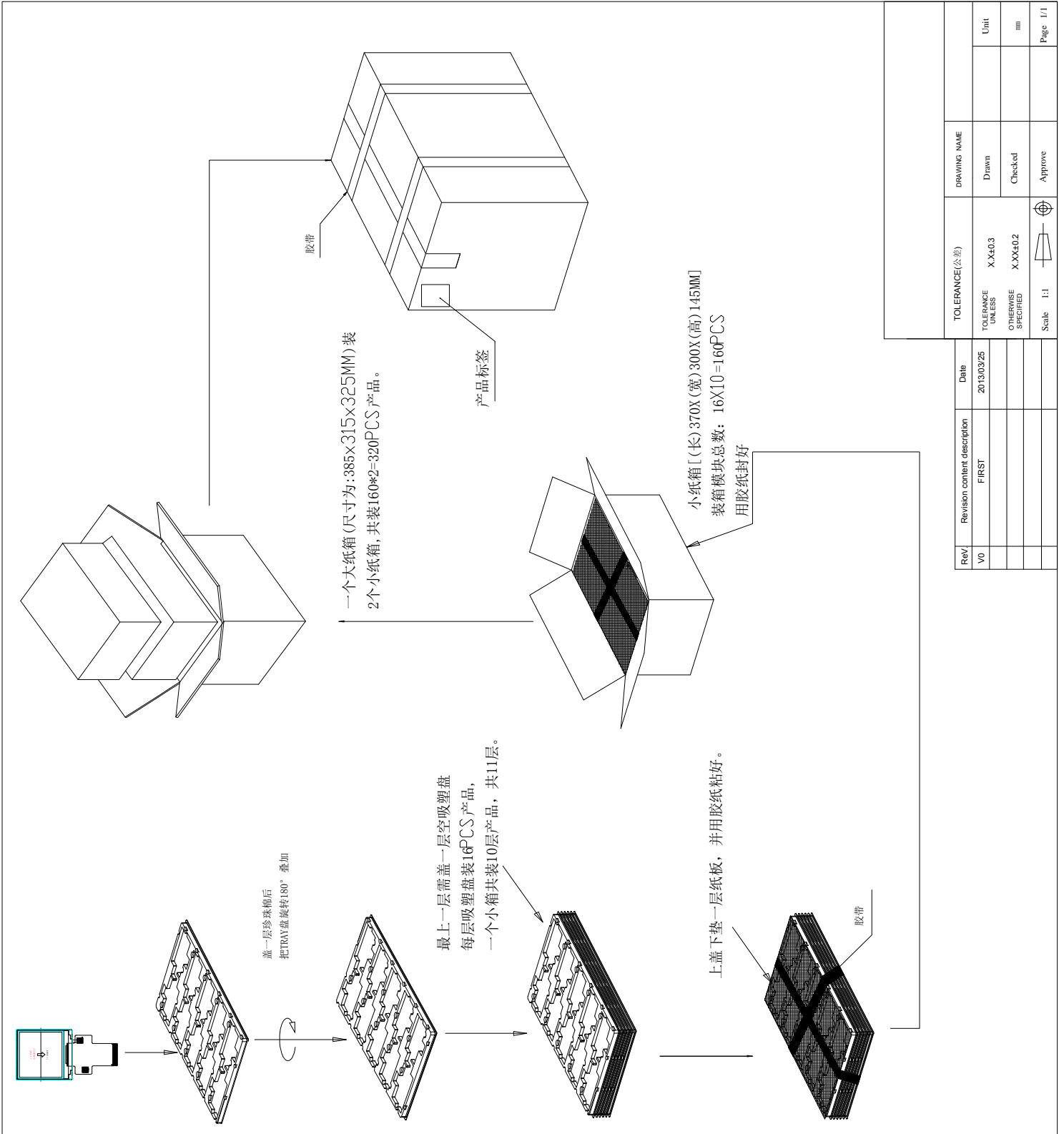
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

10.Packing



Rev	Revision content description	Date	TOLERANCE(公差)	DRAWING NAME	Unit	Page
V0	FIRST	2019/09/25	TOLERANCE UNLESS OTHERWISE SPECIFIED	Drawn	mm	1/1
				Checked		
				Approve		