DisplayModule

DM-TFT18-309

1.8” TFT LCD DISPLAY PANEL WITH 8/9/16/18 BIT MCU, 3/4 SPI AND 16/18 BIT RGB INTERFACE

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1 Revision History

Date	Changes
2015-01-21	First release

2 Main Features

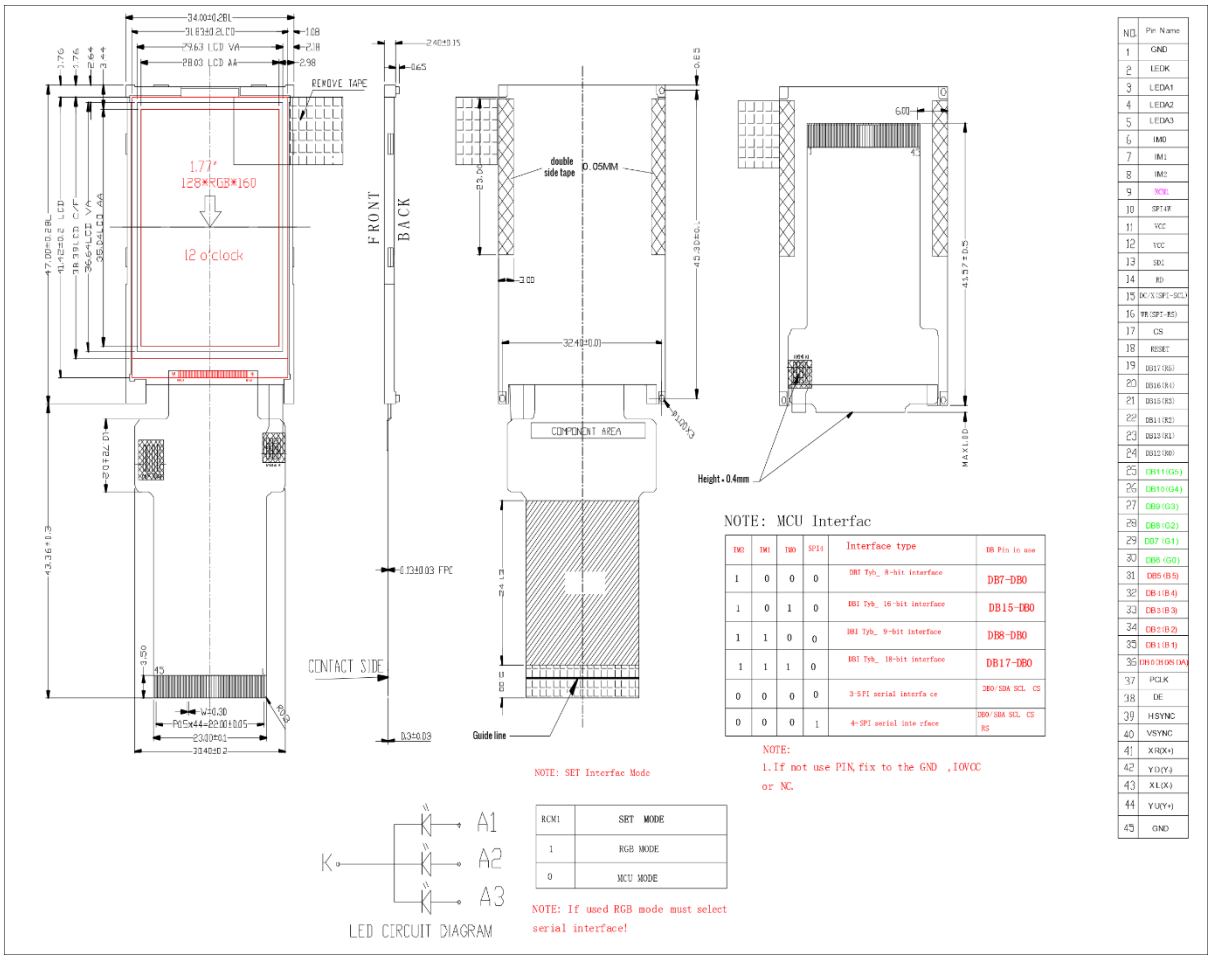
Item	Specification	Unit
Screen Size	1.77	inch
Driver Mode	Transmissive	-
Display Colors	65K	colors
Resolution	128 x 160	dots
Controller IC	Ilitek ILI9163	-
Interface	8/16bit MCU, 3/4 SPI+16/18bit RGB	-
Power Supply	3.3	V
View Direction	12 o'clock	-
Background LED	3 LED Normally White	-
Weight	5.9	g

3 Pin Description

Pin No.	Symbol	Function Description
1	GND	Ground
2	LEDK	Cathode pin of backlight
3	LEDA1	Anode pin of backlight
4	LEDA2	Anode pin of backlight
5	LEDA3	Anode pin of backlight
6	IM0	IM1 / IM0 / Parallel interface 0 / 0 / MCU 8-bit Parallel 0 / 1 / MCU 16-bit Parallel 1 / 0 / MCU 9-bit Parallel 1 / 1 / MCU 18-bit Parallel
7	IM1	
8	IM2	MCU Parallel interface bus and Serial interface select IM2='1': Parallel Interface IM2='0': Serial Interface
9	RCM1	RGB and MCU interface mode selection pin RCM1='1': RGB Interface RCM1='0': MCU Interface
10	SPI4W	SPI interface selection pin SPI4W='1': 3-wire SPI SPI4W='0': 4-wire SPI. This pin is internal pull low.
11	VCC	Supply voltage(3.3V)
12	VCC	Supply voltage(3.3V)
13	SDI	When RCM1='1': The data is input on the rising edge of the SCL signal. The data is output on the falling edge of the SCL signal. When RCM1='0': This pin is not used and fix at VDDI or GND level.
14	SD	Read enable. If not used, please connect this pin to VDD
15	DC/SCL	Display data / Command selection pin in parallel and SCL in SPI interface. DC/SCL='1': Display data DC/SCL='0': Command data. If not used, please connect to this pin to GND.
16	WR/SPI_RS	Write enable in parallel interface. WR: for 8080 MCU SPI_RS: for SPI Interface
17	CS	Chip select input pin (LOW enable).
18	RESET	Active LOW Reset signal
19-36	DB17-DB0(SDA)	When RCM1='0' (MCU I/F), D [17:0] are used to MCU parallel interface data bus, and D 0 is also the serial input/ output signal in SPI interface mode. In serial interface, D [17: 1] are not used and should be connected to ground. When RCM1='1' (RGB I/F), D [17:0] are used to RGB interface data bus.
37	PCLK	Pixel clock signal in RGB I/F mode. If not used, please fix this pin at GND level

38	DE	Data enable signal in RGB I/F mode. If not used, please fix this pin at GND level
39	HSYNC	Horizontal sync signal in RGB I/F mode. If not used, please fix this pin at GND level
40	VSUNC	Vertical sync signal in RGB I/F mode. If not used, please fix this pin at GND level
41	XR(NC)	No connection
42	YD(NC)	No connection
43	XL(NC)	No connection
44	YU(NC)	No connection
45	GND	Ground

4 Mechanical Drawing



5 Electrical Characteristics

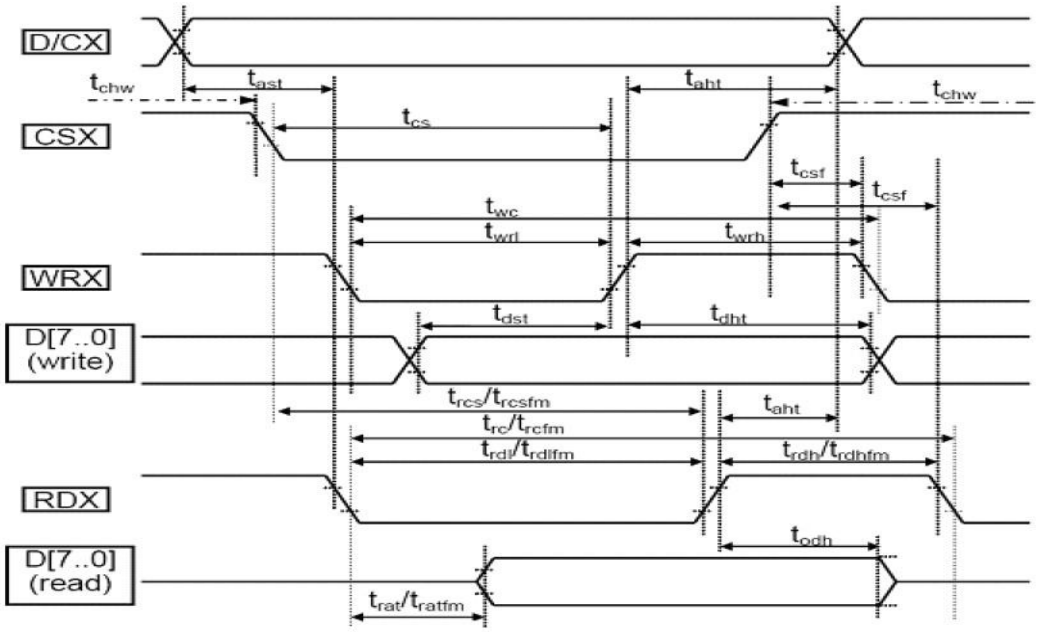
Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage For Logic	VDD		2.5	3.3	4.2	V
Digital Operation Current	IDD	VDD=3.3V	-	1.5	-	mA
Low Level Input Voltage	V_{IL}		GND	-	0.3VDD	V
High Level Input Voltage	V_{IH}		0.7VDD	-	VDD	V
Low Level Output Voltage	V_{OL}		GND		0.2VDD	V
High Level Output Voltage	V_{OH}		0.8VDD		VDD	V
Backlight Forward Voltage	V_{LED}		-	3.2	-	V
Backlight Forward Current	I_{LED}	V_{LED}=3.2V	45	60	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Note
View Angles Top		35	45		°	
View Angles Bottom		10	20		°	
View Angles Left		35	45		°	
View Angles Right		35	45		°	
Response Time (25°C)	Tr + Tf		8	16	ms	
Uniformity		80			%	
Contrast Ratio	CR	400	500			
Luminance	L_V	300	360		cd/m²	

7 Timing Characteristics

7.1 8-bit Parallel MCU Interface Timing Characteristics (8080-system)



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Signal	Symbol	Parameter	min	max	Unit	Note
D/CX	tast	Address setup time	0		ns	
	taht	Address hold time(Write/Read)	10		ns	
CSX	tchw	CSH “H” Pulse Width	0		ns	
	tcs	Chip select setup time(Write)	10		ns	
	trcs	Chip select setup time(Read ID)	45		ns	
	trcsfm	Chip select setup time(Read FM)	355		ns	
	tcsf	Chip select wait time(Write/Read)	10		ns	
WRX	twc	Write cycle	66		ns	
	twrh	Control pulse H duration	15.		ns	
	twrl	Control pulse L duration	15		ns	
RDX	trc	Read cycle (ID)	160		ns	When read ID data
	trdh	Control pulse H duration(ID)	90		ns	
	trdl	Control pulse L duration(ID)	45		ns	
RDX	trcfm	Read cycle (FM)	450		ns	When read from frame memory
	trdhfm	Control pulse H duration(FM)	90		ns	
	trdlfm	Control pules L duration(FM)	355		ns	
D[17 …0]	tdst	Data setup time	10		ns	For maximum CL=30pF for minimum CL=8pF
	tdht	Data hold time	10		ns	
	trat	Read access time(ID)		40	ns	
	tratfm	Read access time(FM)		340	ns	
	todh	Output disable time	20	80	ns	

Note 1: VDDI 1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V, Ta=-30 to 70℃ (to +85℃ no change).

Note 2: This input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

7.2 3-Wire Serial Interface Timing Characteristics

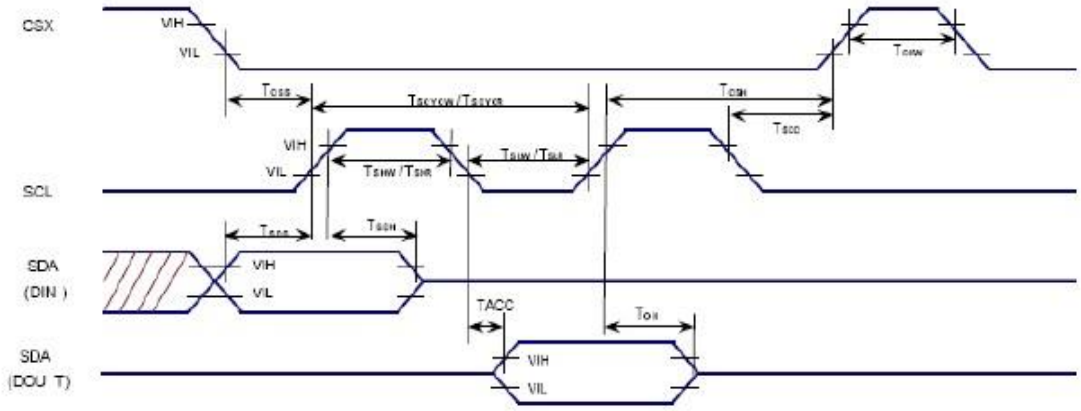


Table 17.3.2.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	10		ns	
	TCSH	Chip select hold time	30		ns	
	TCHW	Chip select "H" pulse width	30		ns	
SCL	TSCYCW	Serial clock cycle(Write)	66		ns	
	TSHW	S"L""H" pulse width(Write)	15		ns	
	TSLW	S"L""L" pulse width(Write)	15		ns	
	TSCYCR	Serial clock cycle(Read)	150		ns	
	TSHR	S"L""H" pulse width(Read)	60		ns	
	TSLR	S"L""L" pulse width(Read)	60		ns	
SDA(DIN) (DOUT)	TSDS	Data setup time	5		ns	
	TSDH	Data hold time	5		ns	
	TACC	Access time	5	50	ns	For maximum CL = 30pF
	TOH	Output disable time	10		ns	For minimum CL = 8pF

Note 1: VDDI=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70℃ (to +85℃ no damage)

Note 2 : The input signal rise time and fall time(tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

7.3 4-Wire Serial Interface Timing Characteristics

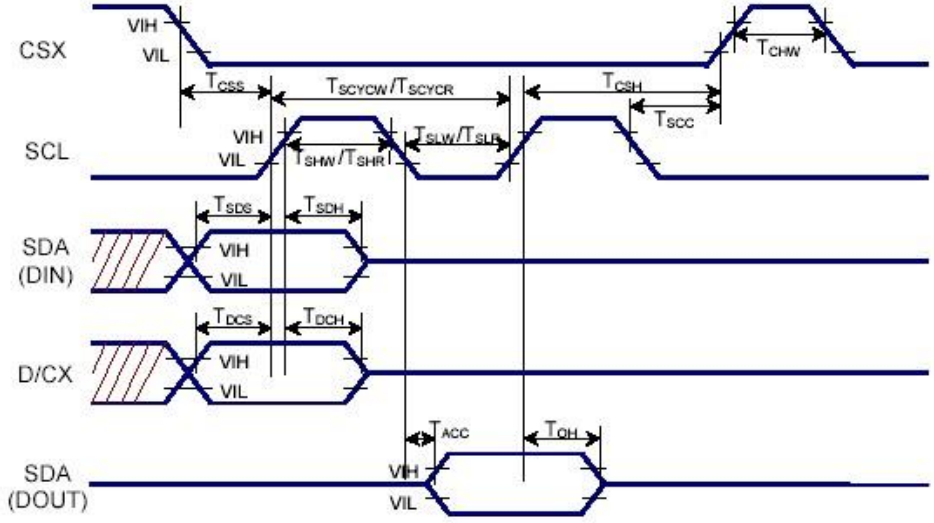


Table 17.3.2.2: 4 pin Serial Interface Characteristics

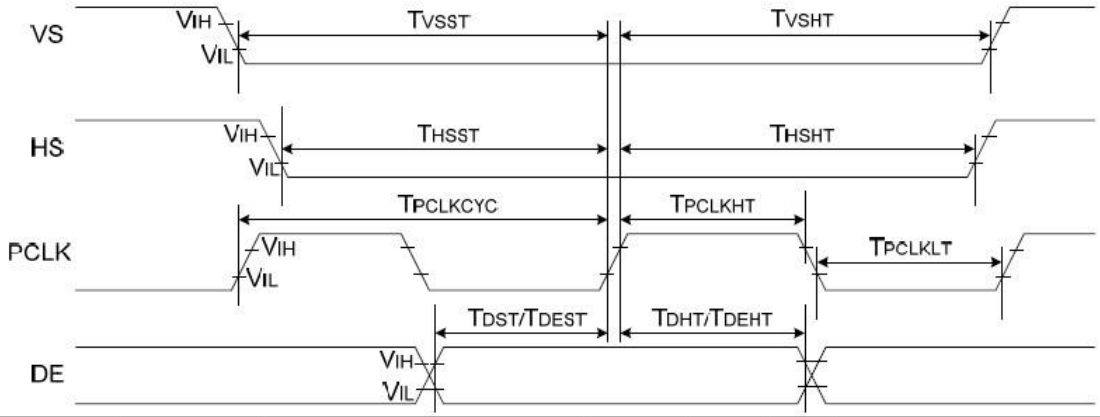
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	10		ns	
	TCSH	Chip select hold time	30		ns	
	TCHW	Chip select "H" pulse width	30		ns	
SCL	TSCYCW	Serial clock cycle(Write)	66		ns	
	TSHW	S"L""H" pulse width(Write)	15		ns	
	TSLW	S"L""L" pulse width(Write)	15		ns	
	TSCYCR	Serial clock cycle(Read)	150		ns	
	TSHR	S"L""H" pulse width(Read)	60		ns	
	TSLR	S"L""L" pulse width(Read)	60		ns	
D/CX	TDCS	D/CX setup time	5		ns	
	TDCH	D/CX hold time	5		ns	
SDA(DIN) (DOUT)	TSDS	Data setup time	5		ns	
	TSDH	Data hold time	5		ns	
	TACC	Access time	5	50	ns	For maximum CL = 30pF
	TOH	Output disable time	10		ns	For minimum CL = 8pF

Note 1: VDDI=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70℃ (to +85℃ no damage)

Note 2 : The input signal rise time and fall time(tr, tf) is specified at 15 ns or less.

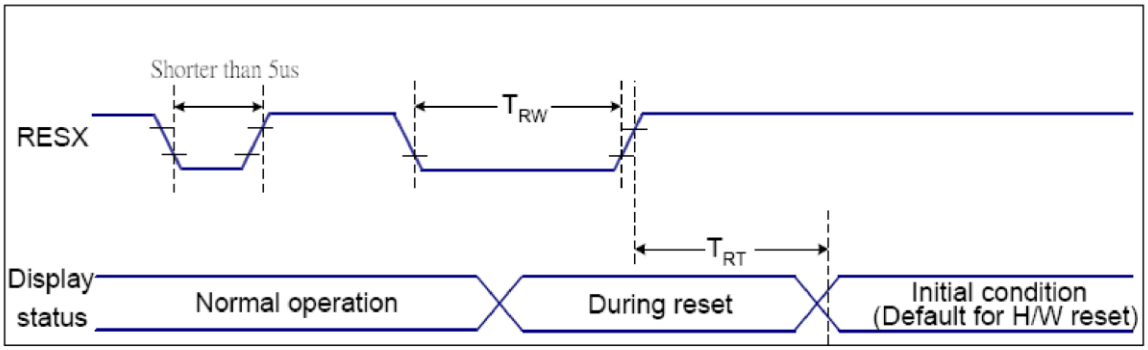
Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

7.4 Parallel RGB Interface Timing Characteristics



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
PCLK	TPCLKCYC	TPCLK Cycle time	66		ns	
	TPCLKLT	Pixel low pulse width	15	-	ns	
	TPCLKHT	Pixel high pulse width	15	-	ns	
VS	TVSST	Vertical Sync. setup time	15	-	ns	
	TVSHT	Vertical Sync. hold time	15	-	ns	
HS	THSST	Horizontal Sync. setup time	15	-	ns	
	THSHT	Horizontal Sync. hold time	15	-	ns	
DE	TDEST	Data Enable setup time	15	-	ns	
	TDEHT	Data Enable hold time	15	-	ns	
D[17:0]	TDST	Data setup time	15	-	ns	
	TDHT	Data hold time	15	-	ns	

7.5 Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

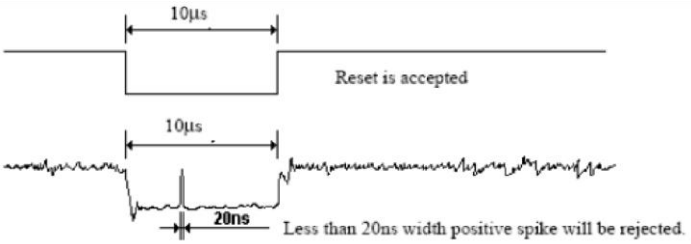
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



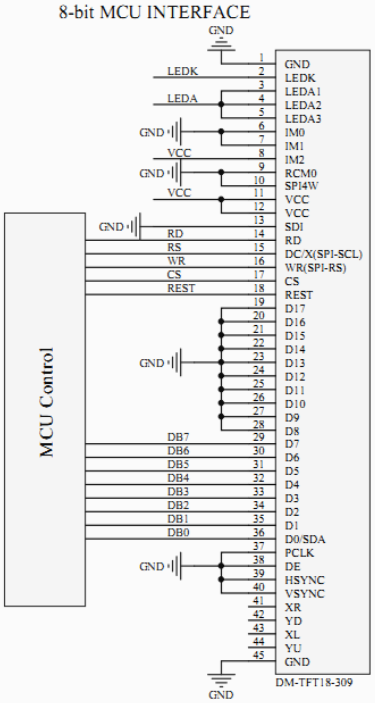
5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

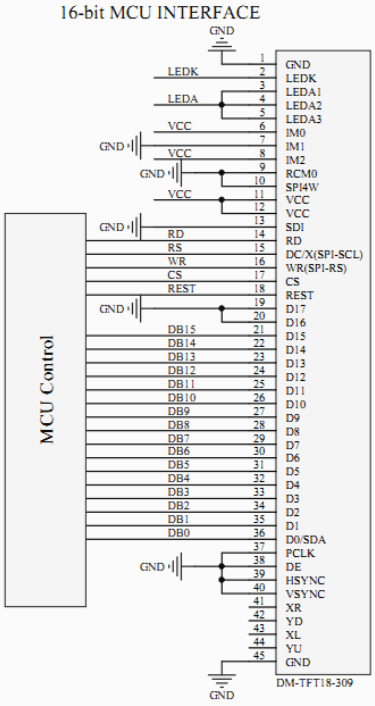
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 Application Reference

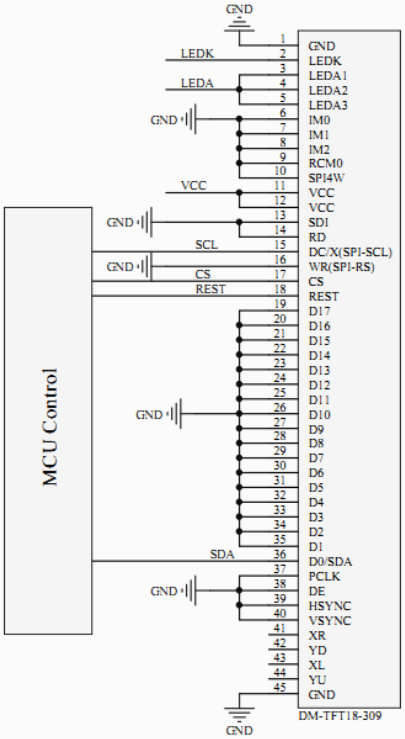
8-bit MCU INTERFACE



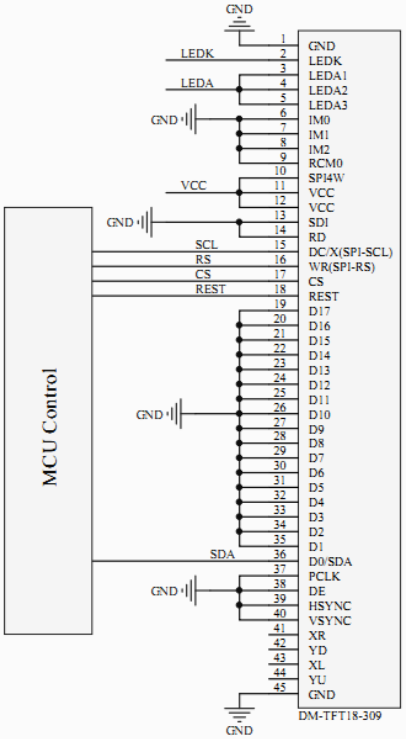
16-bit MCU INTERFACE



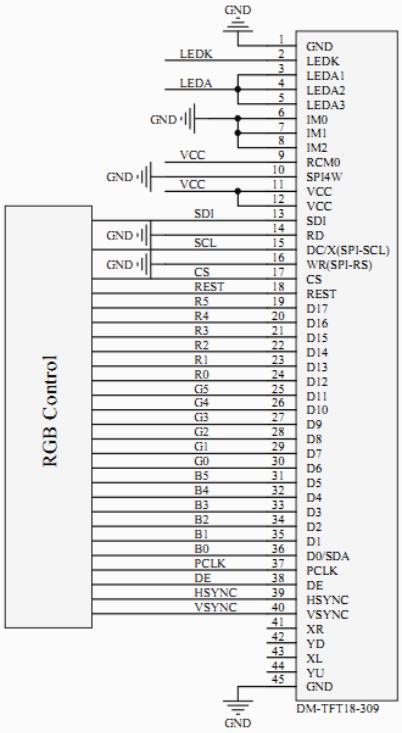
3-WIRE SPI INTERFACE



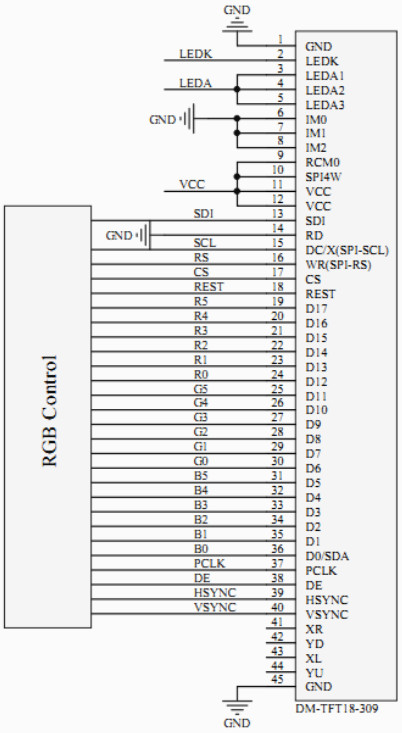
4-WIRE SPI INTERFACE



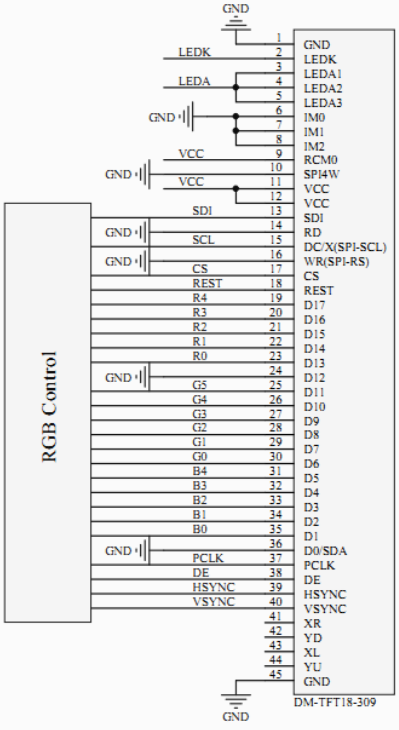
3-WIRE SPI AND 18-BIT RGB



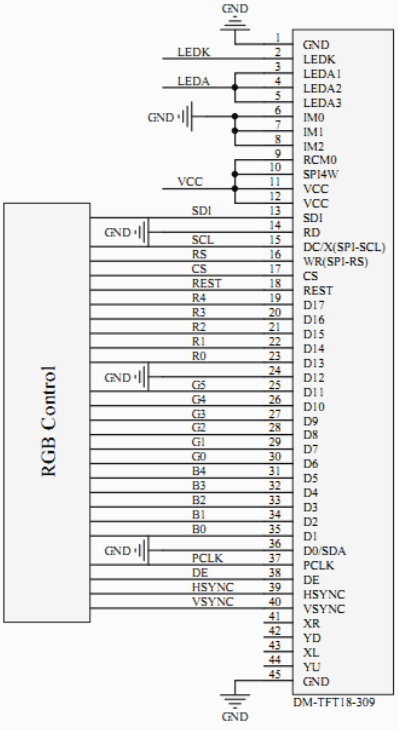
4-WIRE SPI AND 18-BIT RGB



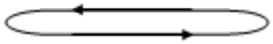
3-WIRE SPI AND 16-BIT RGB



4-WIRE SPI AND 16-BIT RGB



9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 ℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃  30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: The packing have to including into the vibration testing.

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq