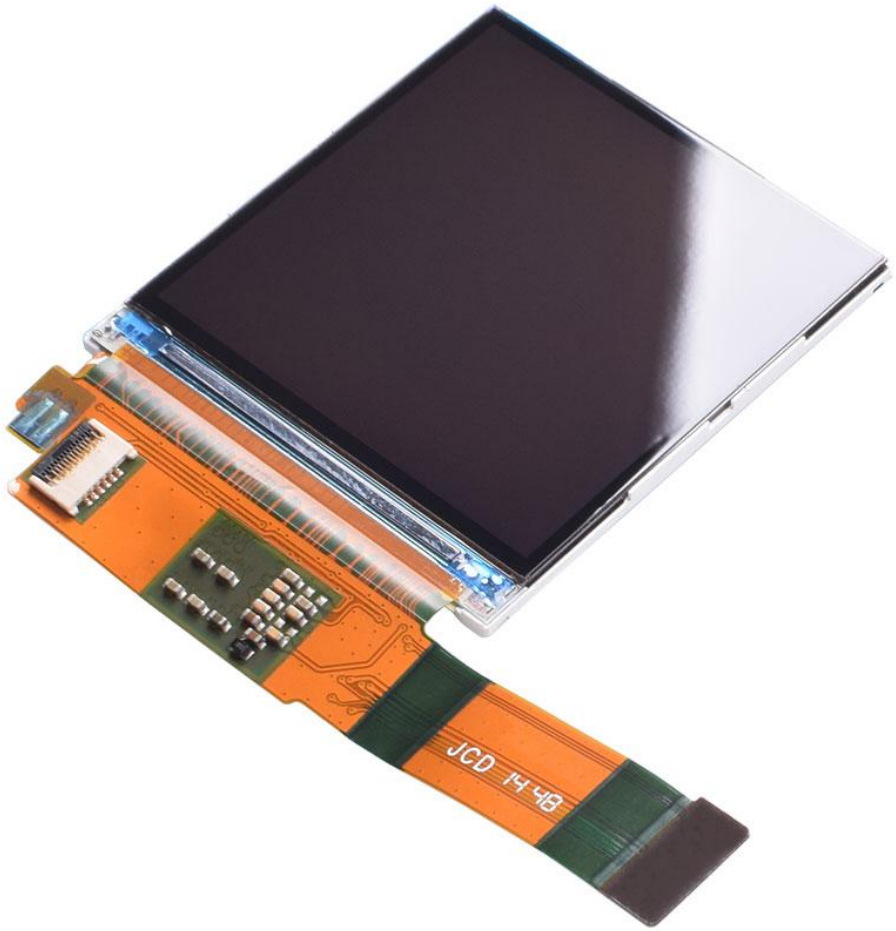
DisplayModule




# DM-TFT16-393

## 1.6" 320 × 320 TRANSFLECTIVE DISPLAY PANEL - MIPI

# Contents

# 1 Revision History

| Date | Changes |
|---|---|
| 2019-08-02 | First release |

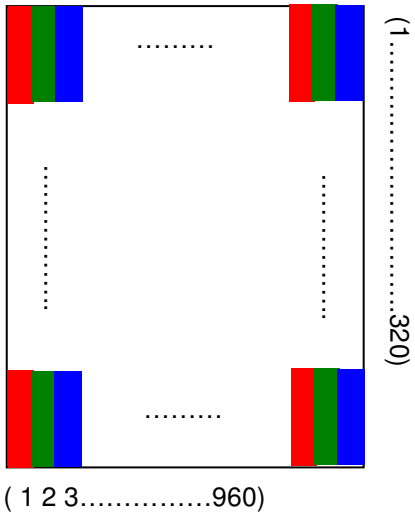
# 2 Main Features

| Item | Specification | Unit | Remark |
|---|---|---|---|
| Diagonal Size | 1.6 | inch | |
| Display Mode | a-Si | - | |
| LCM Type | Transflective | - | |
| Liquid Crystal Mode | TR-MVA | - | |
| Resolution | 320 x 3 RGB x 320 | pixel | |
| Controller IC | Novatek 35310 | - | |
| Interface | MIPI | - | |
| Active Area | 28.80 x 28.80 | mm | |
| Panel Dimension | 31.0 x 34.36 x 0.4 | mm | Note 1 |
| Pixel Pitch | 0.03 x RGB x 0.09 | mm | |
| Color Configuration | R. G. B. Stripe | - | Note 2 |
| Display Colors | 262K Colors | Colors | Note 3 |
| Weight | TBD | g | |

Note 1: 0.2mm TFT + 0.2mm CF glass.

Note 2: Below figure shows dot stripe arrangement.

Note 3: Color depth depend on Driver IC output.



# 3 Pin Description

## 3.1 LCD Pin Description

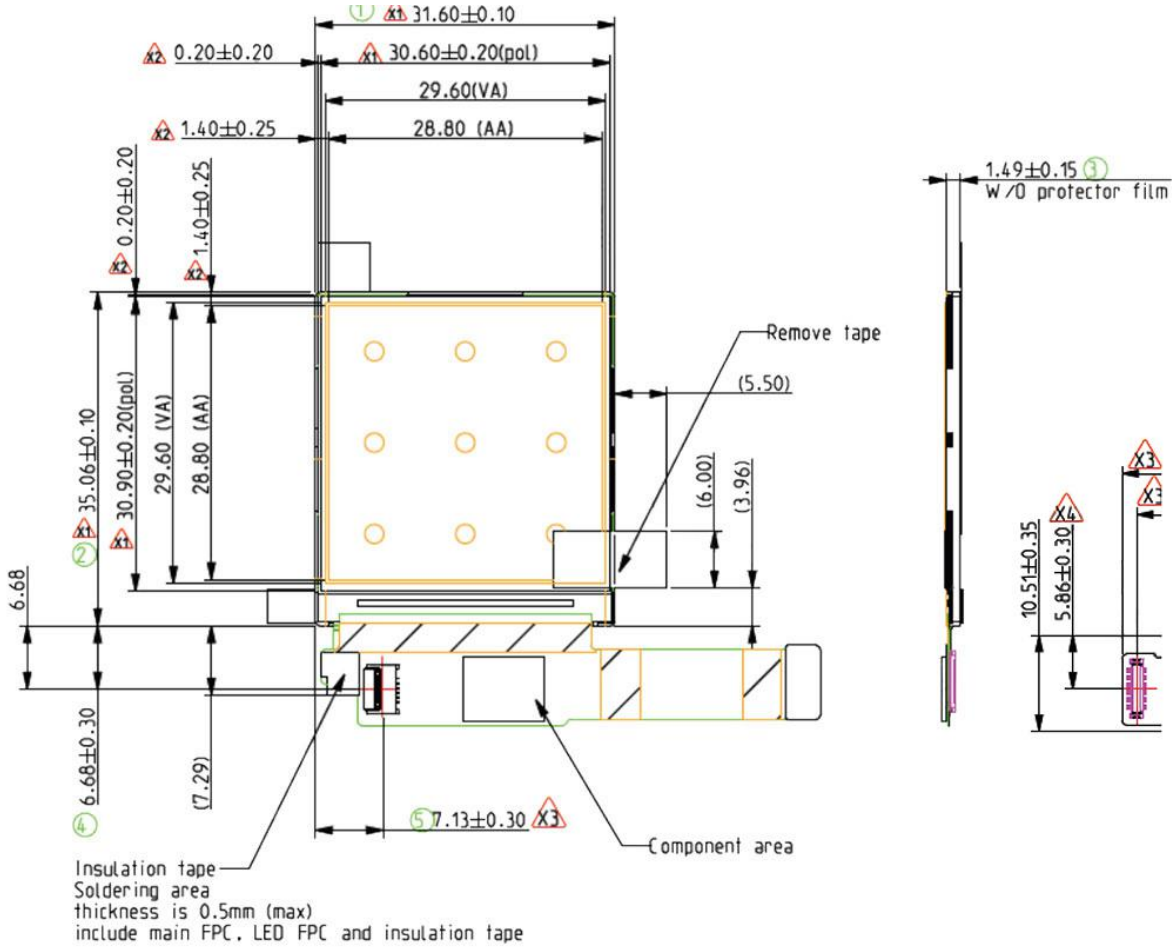
| Pin No. | Symbol | Function Description |
|---|---|---|
| A1 | GND | Ground |
| A2 | MIPI_D0N | Data Pair - |
| A3 | MIPI_D0P | Data Pair + |
| A4 | GND | Ground |
| A5 | MIPI_CKN | Clock pair - |
| A6 | MIPI_CKP | Clock pair + |
| A7 | GND | Ground |
| A8 | TOUCH_RESET | Reset Signal TOUCH |
| A9 | I2C_TOUCH_SCL | TOCUH I2C Clock |
| A10 | I2C_TOUCH_SDA | TOCUH I2C Data |
| A11 | LCD_ANODE | LED Anode |
| A12 | GND | Ground |
| B1 | GND | Ground |
| B2 | MTP_PWR | Free to use for OTP (NC on PCB) |
| B3 | BMU_PWM | Output PWM Signal |
| B4 | DISP_3V0 | Analog Power Supply 3v |
| B5 | GND | Ground |
| B6 | LCD_1V8 | Digital power supply 1.8V |
| B7 | GND | Ground |
| B8 | LCD_RESET | RESET SIGNAL LCD |
| B9 | TEARING | Tearing Signal |
| B10 | TOUCH_WKUP_INT | Touch Interrupt |
| B11 | LCD_CATHODE | LED Cathode |
| B12 | GND | Ground |

## 3.2 Touch Connector Pin Description

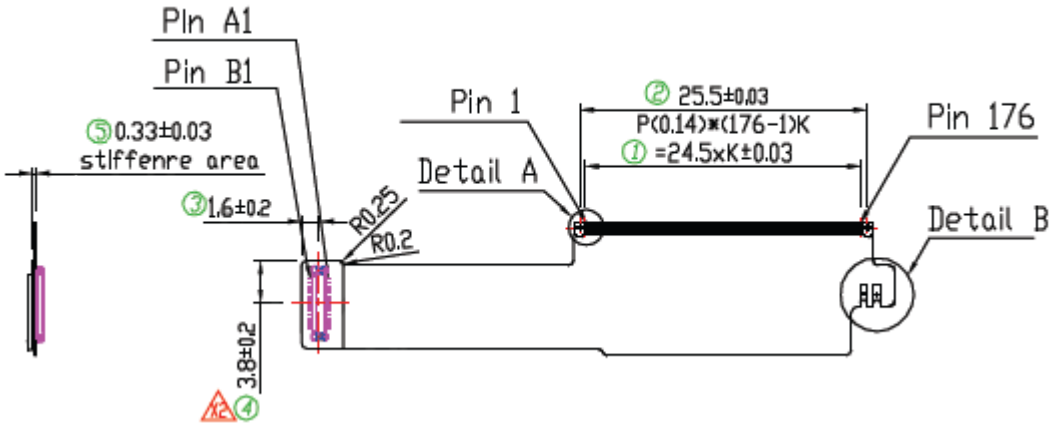
| Pin No. | Symbol | Function Description |
|---|---|---|
| 1 | VDDI | Digital power supply 1.8V |
| 2 | VCI | Analog Power Supply 3 V |
| 3 | TOUCH_WKUP_INT | Touch Interrupt |
| 4 | GND | Ground |
| 5 | I2C_SDA | TOUCH I2C Data |
| 6 | GND | Ground |
| 7 | I2C_SCL | TOUCH I2C Clock |
| 8 | GND | Ground |
| 9 | TOUCH_RESET | Reset Signal TOUCH |
| 10 | GND | Ground |
| 11 | NC | ISSP SDA |
| 12 | NC | ISSP SCL |

# 4 Mechanical Drawing

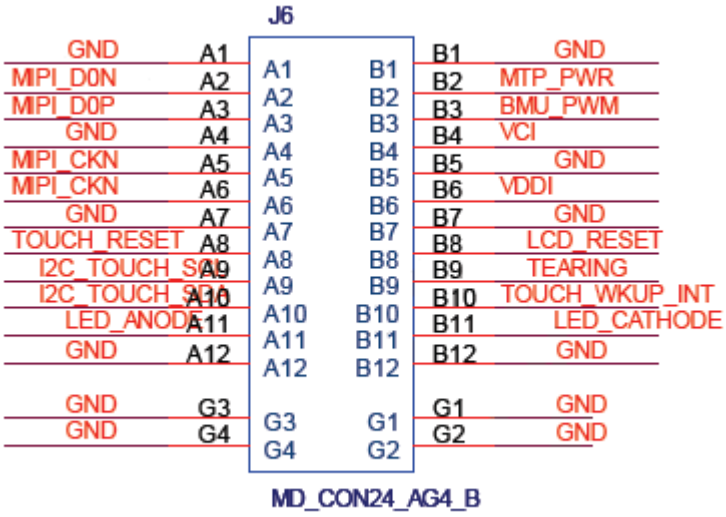
## 4.1 Panel Mechanical Drawing



## 4.2 Touch Connector




## 4.3 LCD Connector



# 5 Optics & Electrical Characteristics

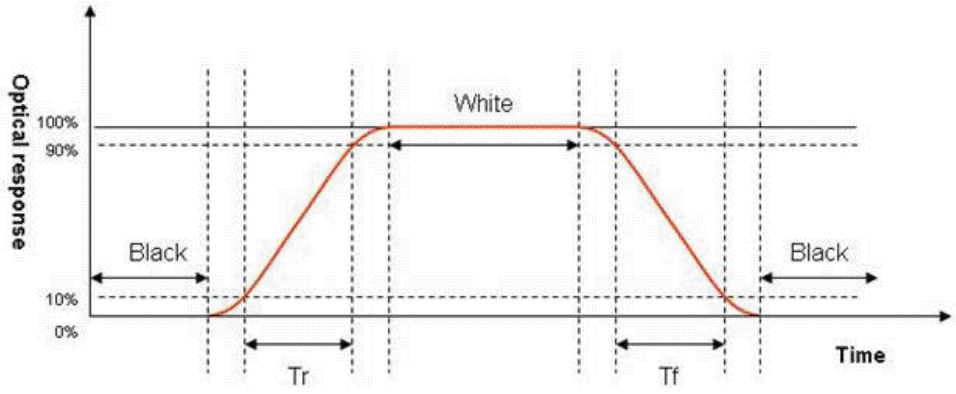
## 5.1 Optical Characteristics

| Item | Symbol | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| View Angles TOP | Θ U | - | 50 | - | ° | CR≧10; θ=0 ,90,180,270; |
| View Angles Bottom | Θ D | - | 45 | - | ° | |
| View Angles Right | Θ R | - | 50 | - | ° | |
| View Angles Left | Θ L | - | 45 | - | ° | |
| C.I.E. (White) | u'<br>v' | - | 0.189<br>0.477 | - | - | θ=0° |
| C.I.E(Red) | u'<br>v' | - | 0.451<br>0.528 | - | - | |
| C.I.E(Green) | u'<br>v' | - | 0.129<br>0.558 | - | - | |
| C.I.E(Blue) | u'<br>v' | - | 0.180<br>0.160 | - | - | |
| NTSC | - | - | 80 | - | % | θ=0°; NTSC1976 |
| Pixel Luminance | $L_{br}$ | 270 | 340 | - | cd/m² | - |
| Response Time Rise + Fall | Tr + Tf | - | 30 | 40 | ms | θ=0°; Note 1 |
| Contrast Ratio | CR | 450 | 600 | - | - | θ=0°; Note 2 |
| Reflection | - | - | 5.3 | - | % | Panel with APCF (GVDD = 4.9V); BLU Off, C-light on DMS-803 |

Note 1: Definition of response time

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (rising time) and from “white” to “black” (falling time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.




Note 2.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

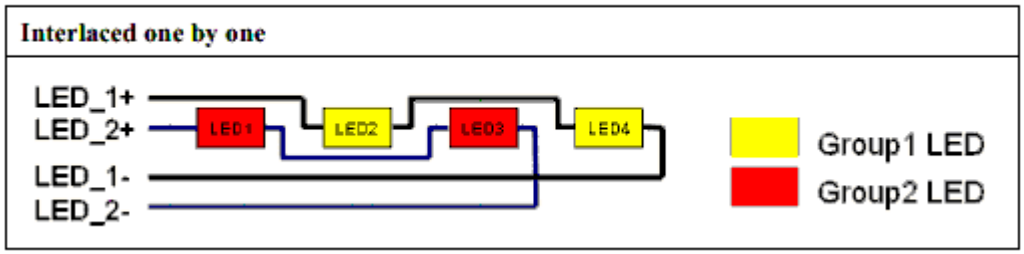
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

**Backlight Driving Conditions**

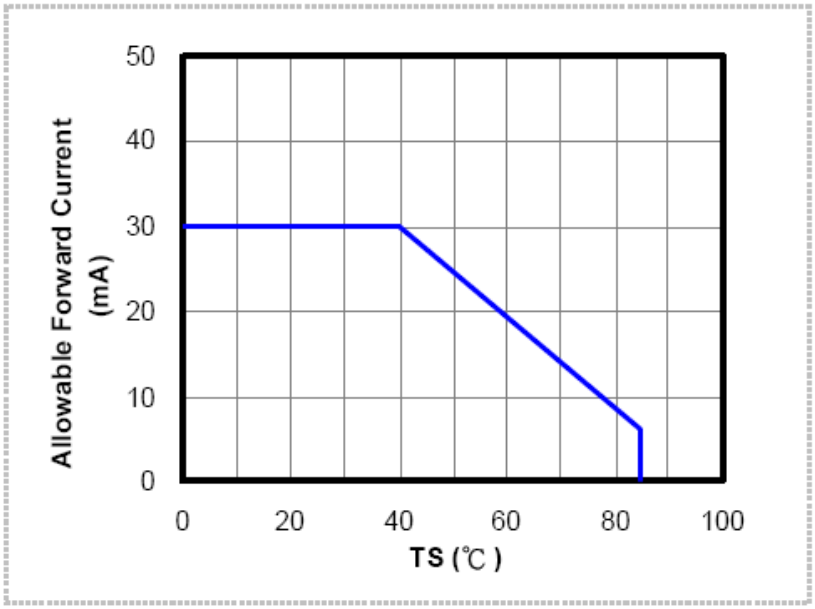
| Item | Symbol | Min | Typ. | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| LED Supply | IL | -- | 15 | | mA | Single Serial |
| LED Supply | VL | -- | 12 | | V | Single Serial |
| LED Supply | IR | -- | -- | | uA | Single Serial |

Note 1: LED backlight is 4 LEDs 4 serial 1 parallel type.
Note 2: Nichia 206C

**LED interlacing**




**LED Forward Current VS. Temperature**



## 5.2 Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Logic Input Voltage | VIN | 1.65 | 3.3 | V |
| Logic Input Voltage | VO | 1.65 | 3.3 | V |
| Supply Voltage | VDDI | 1.65 | 3.3 | V |
| Supply Voltage | VCI-AVSS | 2.3 | 3.3 | V |
| Driver Supply Voltage | AVDD-AVSS | -0.3 | 6.4 | V |
| Supply voltage (MTP) | MTP_PWR - AVSS | 7.5 | | V |
| Max Voltage of VGH-VGL | | <32 | | V |
| Humidity | | 5 | 95 | % |
| Operating Temperature | TOP | -40 | 70 | ℃ |
| Storage Temperature | TSTG | -40 | 85 | ℃ |

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

## 5.3 DC Characteristics

| Item | Symbol | Min | Typ. | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| Analog Operating Voltage<br>MDDI/MIPI Operating Voltage<br>Digital Operating Voltage | VCI | 2.3 | 2.8 | 3.3 | V | Operating Voltage<br>MDDI/MIPI<br>Supply voltage;<br>Note 1,5 |
| I/O Operating Voltage | VDDI | 1.65 | 1.8 | 3.3 | V | I/O supply<br>voltage;<br>Note 1,5 |
| Low Level Input Voltage | VIL | VSS | - | 0.3 x VDDI | V | - |
| High Level Input Voltage | VIH | 0.7 x VDDI | - | VDDI | V | - |
| Low Level Output Voltage | VOL | VSS | - | 0.2 x VDDI | V | - |
| High Level Output Voltage | VOH | 0.8 x VDDI | - | VDDI | V | - |
| Logic Low level leakage<br>(Except MDDI / MIPI) | ILIL1 | -1 | - | - | µA | Vin = 0 to VDDI;<br>Note 2,3,4 |
| Logic High level leakage<br>(Except MDDI / MIPI) | ILIH1 | - | - | 1 | µA | Vin = 0 to VDDI;<br>Note 2,3,4 |
| Logic Low level leakage<br>(MDDI / MIPI) | ILIL2<br>(MDDI) | -10 | - | - | µA | Vin = 0 to 1.3V;<br>Note 2,5 |
| | ILIL2<br>(MIPI) | | | | | |
| Logic High level leakage<br>(MDDI / MIPI) | ILIH2<br>(MDDI) | - | - | 10 | µA | Vin = 0 to VDDI;<br>Note 2,5 |
| | ILIH2<br>(MIPI) | | | | | |

Note 1: VDDI=1.65 to 3.3V, VCI=2.3 to 3.3V, AVSS=VSS=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage).

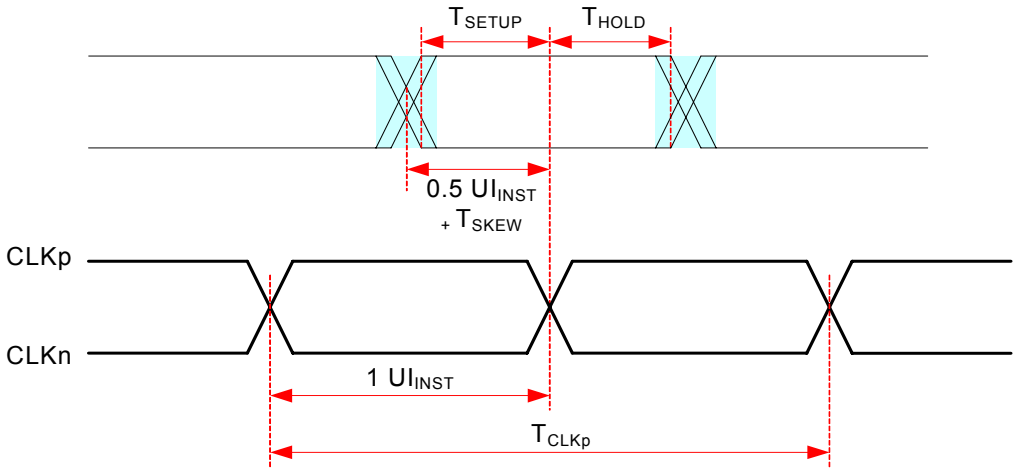
Note 2,3,4: When the measurements are performed with LCD module, Measurement Points are like below.

Note 5: VCI=2.3V to 3.3 V, VDDI=1.65 to 3.3V, AVSS=VSS=0V, Ta=-30 to 70 ℃ (to +85 ℃ no damage).

## 5.4 AC Characteristics

### 5.4.1 MIPI Interface Timing Characteristics

**High Speed Data transmission: Data-Clock Timing**




| Parameter | Symbol | Min | Typ. | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | TBD | - | 12.5 | ns | Note 1,2 |
| Data to Clock Skew [measured at tansmitter] | $T_{SKEW[TX]}$ | -0.15 | - | 0.15 | $UI_{INST}$ | Note 3 |
| Data to Clock Setup Time [measured at receiver] | $T_{SETUP[RX]}$ | 0.15 | - | - | $UI_{INST}$ | Note 4 |
| Data to Clock Hold Time [measured at reciever] | $T_{HOLD[RX]}$ | 0.15 | - | - | $UI_{INST}$ | Note 4 |
| 20% - 80% rise time and fall time | $t_R$ / $t_F$ | 150 | - | - | ps | - |
| | | | - | 0.3 | $UI_{INST}$ | - |

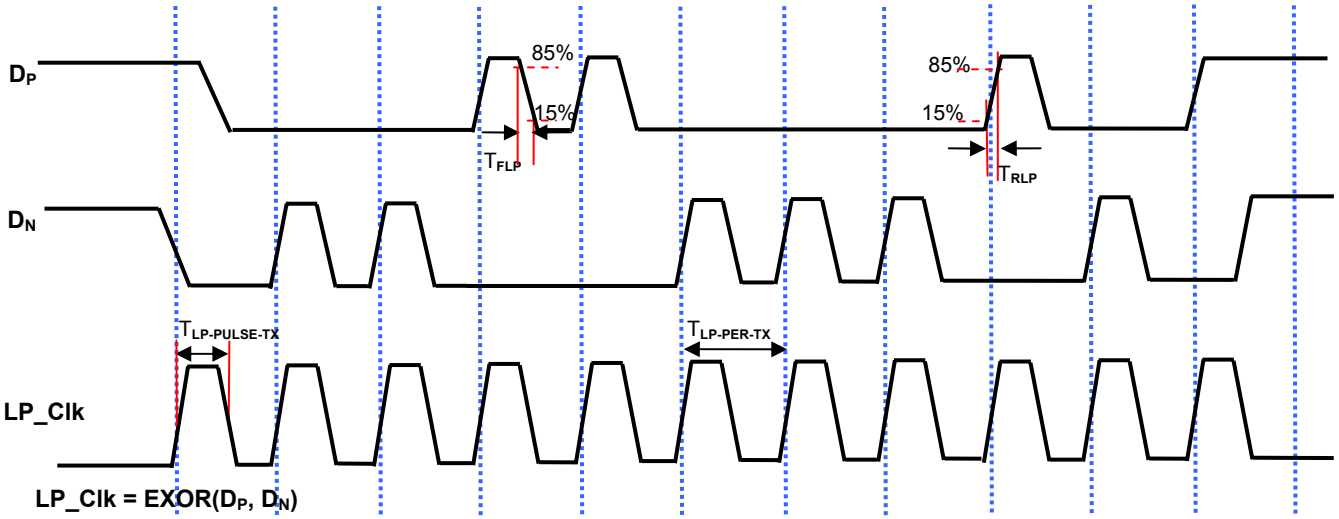
Note 1: This value corresponds to a minimum 80 MHz data rate.

Note 2: The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.

Note 3: Total silicon and package delay budget of 0.3* $UI_{INST}$.

Note 4: Total setup and hole window for receiver of 0.3* $UI_{INST}$.

## LP Transmission AC Specification




| Parameter | | Symbol | Min | Typ. | Max | Unit | Remark |
|---|---|---|---|---|---|---|---|
| 15%-85% rise time and fall time | | $T_{RLP}$ / $T_{FLP}$ | - | - | 25 | ns | Note 1 |
| 30%-85% rise time and fall time | | $T_{REOT}$ | - | - | 35 | ns | Note 1,5,6 |
| Pulse width of the LP exclusive-OR clock | First LP exclusive-OR clock pulse after STOP state or last pulse before stop state | $T_{LP\ PULSE\ TX}$ | 40 | - | - | ns | Note 4 |
| | All other pulses | | 20 | - | - | ns | Note 4 |
| Period of the LP exclusive-OR clock | | $T_{LP\text{-}PER\text{-}TX}$ | 90 | - | - | mV/ns | Note 1,2,3,7 |
| Slew Rate@ $C_{LOAD}$ = 0pF | | $\delta V/\delta t_{SR}$ | 30 | - | 500 | mV/ns | Note 1,2,3,7 |
| Slew Rate@ $C_{LOAD}$ = 5pF | | | 30 | - | 200 | mV/ns | Note 1,2,3,7 |
| Slew Rate@ $C_{LOAD}$ = 20pF | | | 30 | - | 150 | mV/ns | Note 1,2,3,7 |
| Slew Rate@ $C_{LOAD}$ = 70pF | | | 30 | - | 100 | mV/ns | Note 1,2,3,7 |
| Load Capacitance | | $C_{LOAD}$ | - | - | 70 | pF | Note 1 |

Note 1: $C_{LOAD}$ includes the low-frequency equivalent transmission line capacitance. The apacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

Note 2: When the output voltage is between 15% and below 85% of the fully settled LP signal levels.

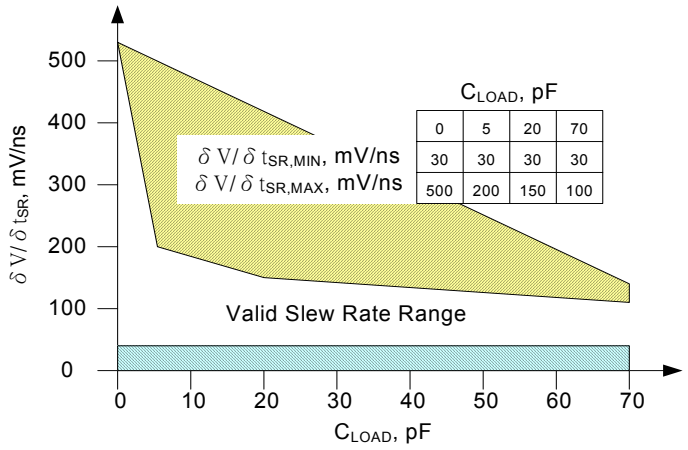
Note 3: Measured as average across any 50 mV segment of the output signal transition.

Note 4: This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.

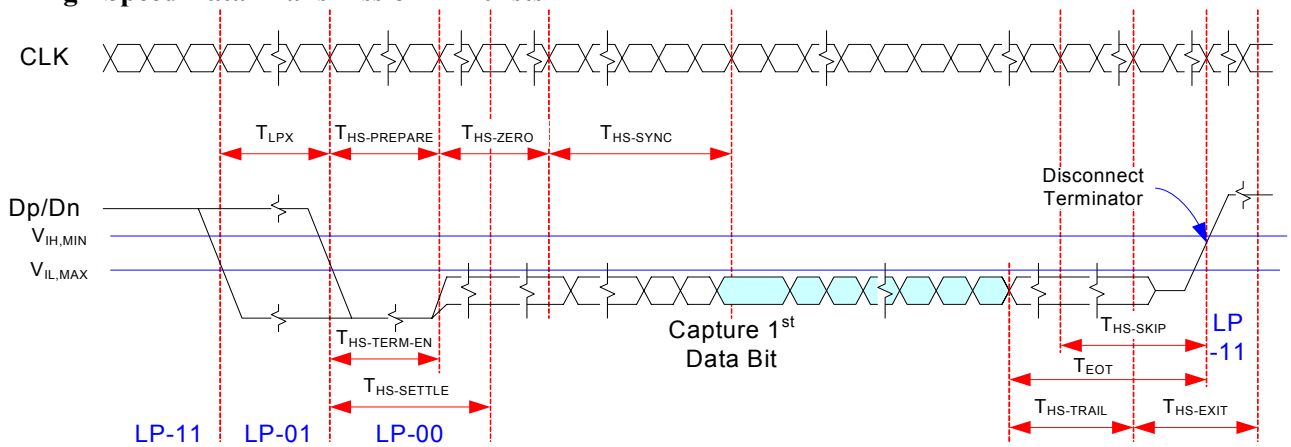
Note 5: The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

Note 6: With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.

Note 7: This value represents a corner point in a piecewise linear curve as bellowed.




**High-Speed Data Transmission in Bursts**



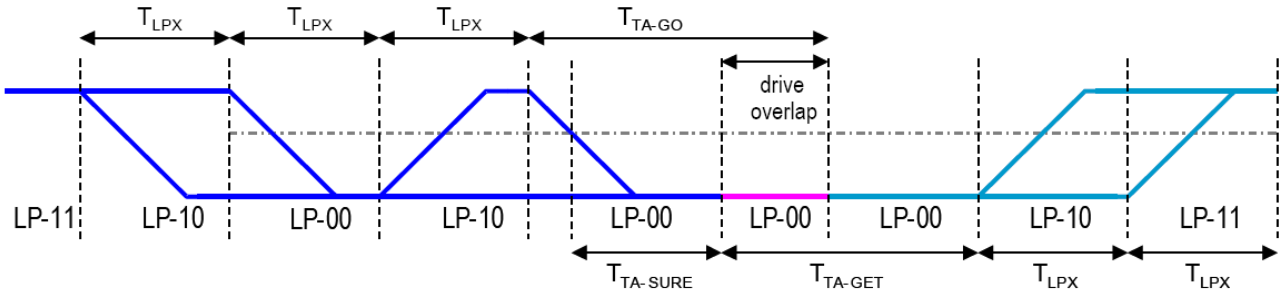

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Time to drive LP-00 to prepare for HS transmission | $T_{HS-PREPARE}$ | 40+4UI | | 85+6UI | ns |
| Time from start of $t_{HS-TRAIL}$ or $t_{CLK-TRAIL}$ period to start of LP-11 state | $T_{EOT}$ | | | 105+12 UI | ns |
| Time to enable Data Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$ | $T_{HS-TERM-EN}$ | | | 35+4UI | ns |
| Time to drive flipped differential state after last payload data bit of a HS transmission burst | $T_{HS-TRAIL}$ | 60+4UI | | | ns |
| Time-out at RX to ignore transition period of EoT | $T_{HS-SKIP}$ | 40 | | 55+4UI | ns |
| Time to drive LP-11 after HS burst | $T_{HS-EXIT}$ | 100 | | | ns |
| Length of any Low-Power state period | $T_{LPX}$ | 50 | | | ns |
| Sync sequence period | $T_{HS-SYNC}$ | | 8UI | | ns |
| Minimum lead HS-0 drive period before the Sync sequence | $T_{HS-ZERO}$ | 105+6UI | | | ns |

Note 1:The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

Note 2:UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.

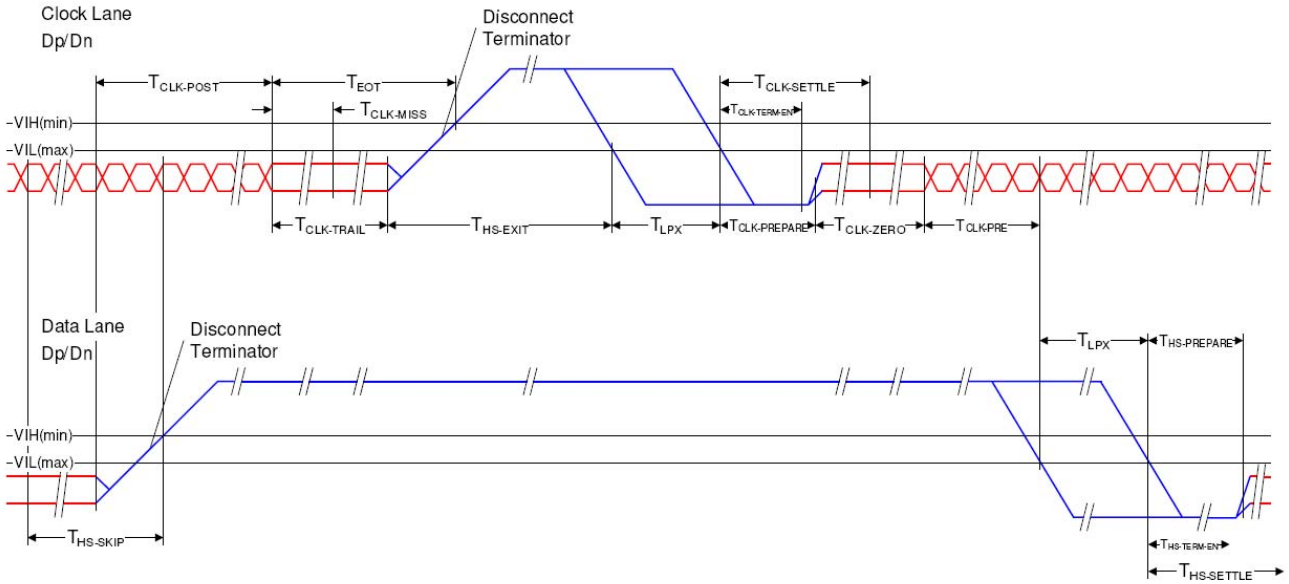
Note 3:TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

**Turnaround Procedure**




| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Length of any Low-Power state period : Master side | $T_{LPX}$ | 50 | | 75 | ns |
| Length of any Low-Power state period : Slave side | $T_{LPX}$ | 47.5 | 50 | 52.5 | ns |
| Ratio of $T_{LPX}$(MASTER)/$T_{LPX}$(SLAVE) between Master and Slave side | Ratio $T_{LPX}$ | 2/3 | | 3/2 | |
| Time-out before new TX side start driving | $T_{TA-SURE}$ | $T_{LPX}$ | | $2T_{LPX}$ | ns |
| Time to drive LP-00 by new TX | $T_{TA-GET}$ | | $5T_{LPX}$ | | ns |
| Time to drive LP-00 after Turnaround Request | $T_{TA-GO}$ | | $4T_{LPX}$ | | ns |

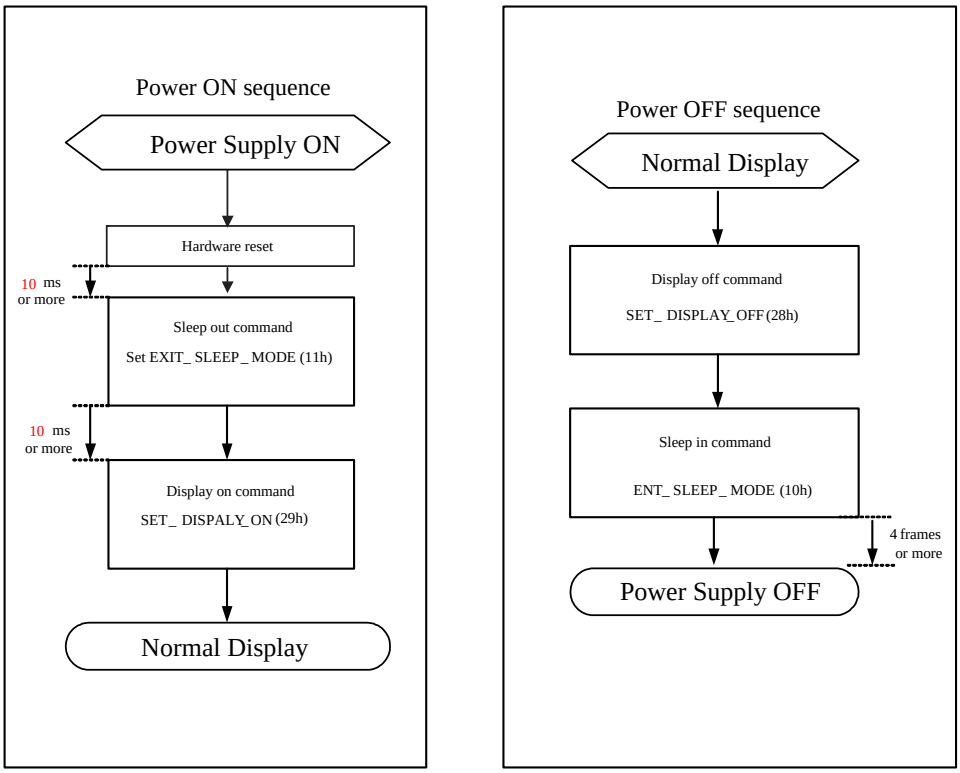
**Switching the Clock Lane between Clock Transmission and Low-Power Mode**



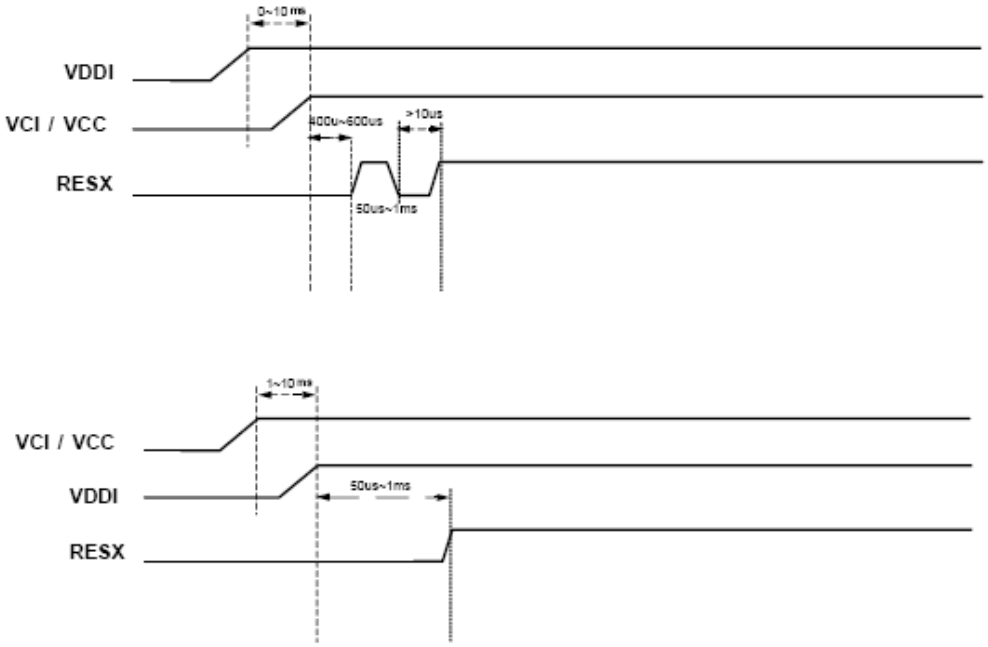

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | $T_{CLK-POST}$ | 60+52 UI | | | ns |
| Detection time that the clock has stopped toggling | $T_{CLK-MISS}$ | | | 60 | ns |
| Time to drive LP-00 to prepare for HS clock transmission | $T_{CLK-PREPARE}$ | 38 | | 95 | ns |
| Minimum lead HS-0 drive period before starting Clock | $T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$ | 300 | | | ns |
| Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX | $T_{HS-TERM-EN}$ | | | 38 | ns |
| Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode | $T_{CLK-PRE}$ | 8 | | | UI |
| Time to drive HS differential state after last payload clock bit of a HS transmission burst | $T_{CLK-TRAIL}$ | 60 | | | ns |

# 6 Power ON/OFF Timing Sequence

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.

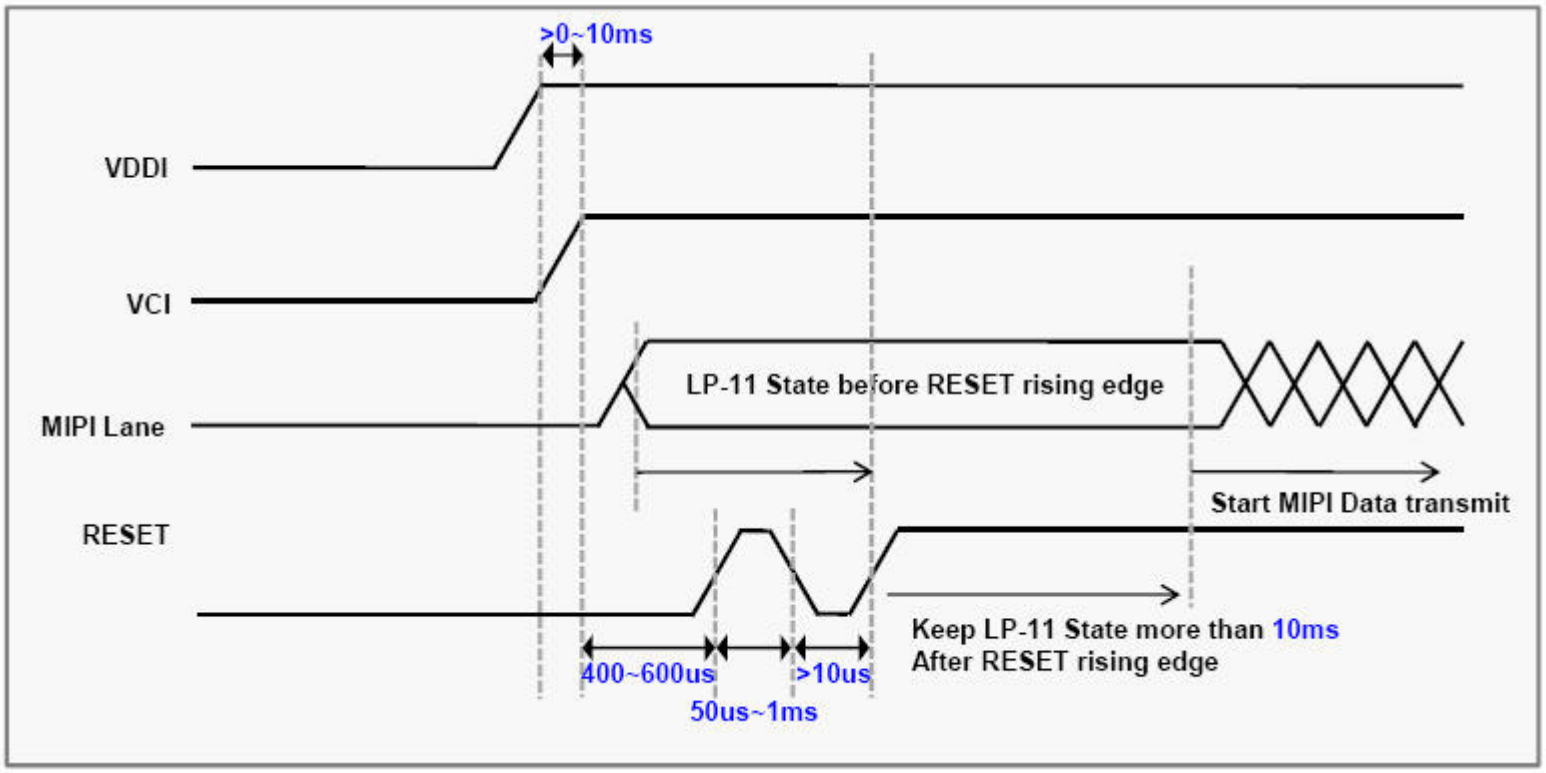



NT35310 support 2 kinds of power on sequence as below.

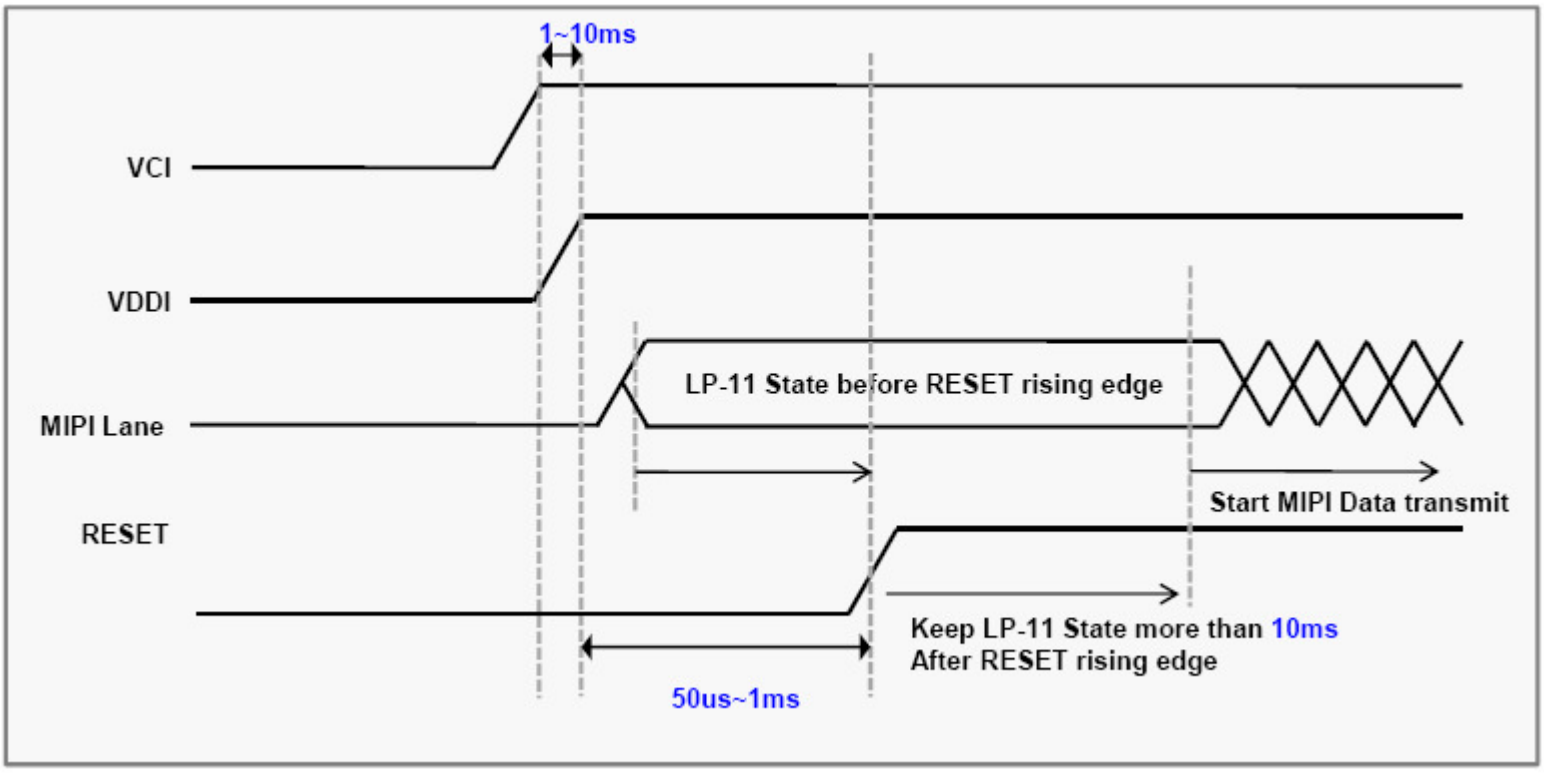


<Power On start condition>

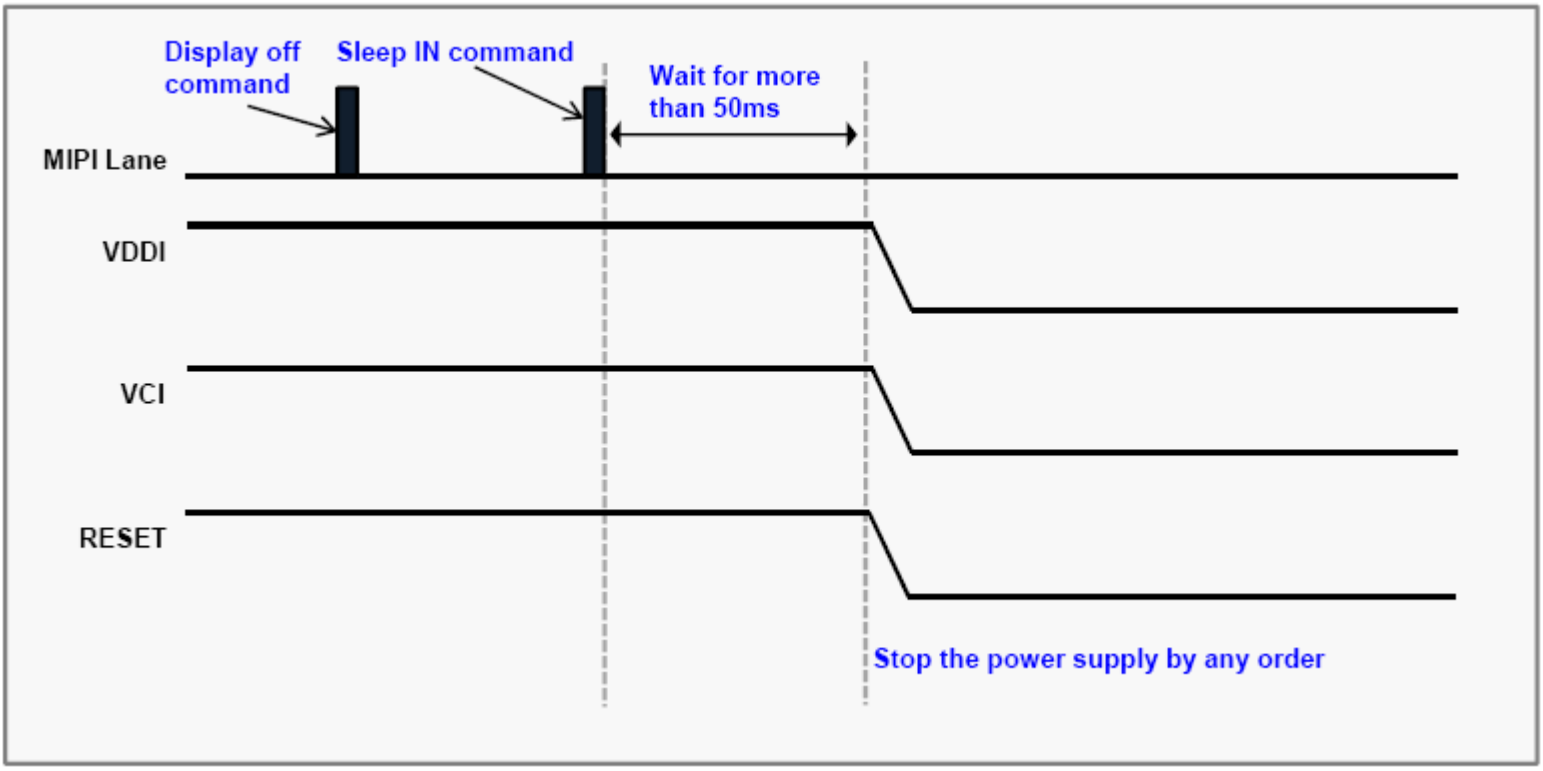
Power on-1



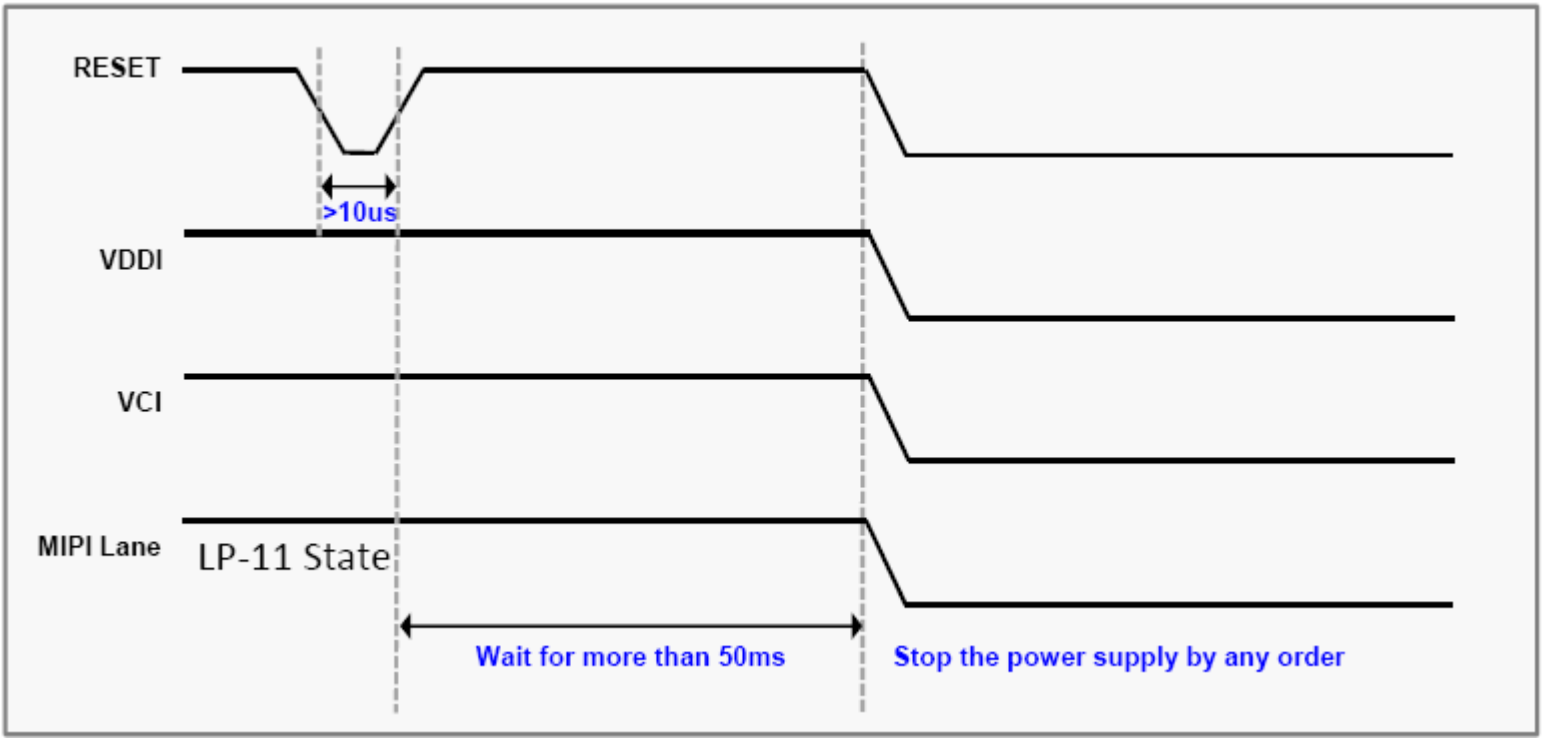

Power on-2



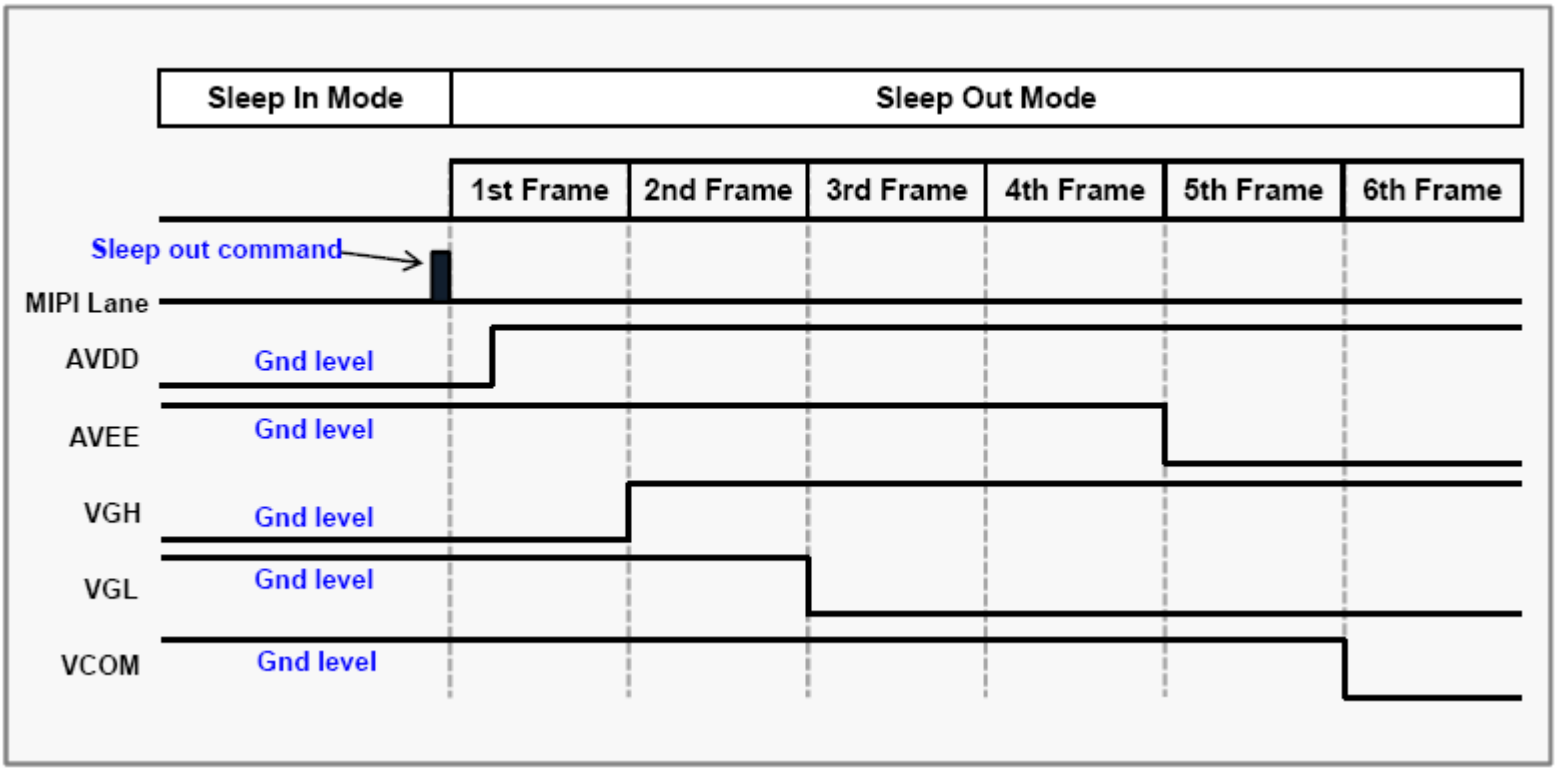
Power off without H/w reset




Power off with H/w reset



Sleep out




**Current & Power Consumption**

| | Max. |
|---|---|
| Power consumption in Normal Mode (white pattern) | 20mW |
| Power consumption in Idle Mode (white pattern) | 6 mW |

**Backlight Power consumption**

| Parameter | Symbol | Min | Typ. | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| Current | IB | - | 15 | - | mA | Note 1 |
| Power Consumption | PFL | - | 180 | - | mW | Note 2 |

Note1: 4 LEDs are connected in serial; each LED’ s forward current is 15mA.

Note2: Where IB=15mA, PBL = IB x VBL, VBL is backlight forward voltage.

**Other electrical characteristics**

| Parameter | Min | Typ. | Max | Unit |
|---|---|---|---|---|
| Frame frequency | - | 60 | - | Hz |

At the condition of power supply voltage is in a range of operation range, ambient temperature is 25℃.

# 7 Reliability

| Test Item | Content of Test | Test Condition | Note |
|---|---|---|---|
| High Temperature Storage | Endurance test applying the high storage temperature for a long time. | 70℃<br>240hrs | 2 |
| Low Temperature Storage | Endurance test applying the high storage temperature for a long time. | -30℃<br>240hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time. | 60℃<br>240hrs | - |
| Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time. | -20 ℃<br>240hrs | 1 |
| High Temperature/<br>Humidity Operation | The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature. | 60℃,90%RH<br>16hrs | 1,2 |
| Thermal Shock Resistance | The sample should be allowed stand the following 10 cycles of operation | -30℃/70℃<br>50 cycles | - |

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

# 8 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"