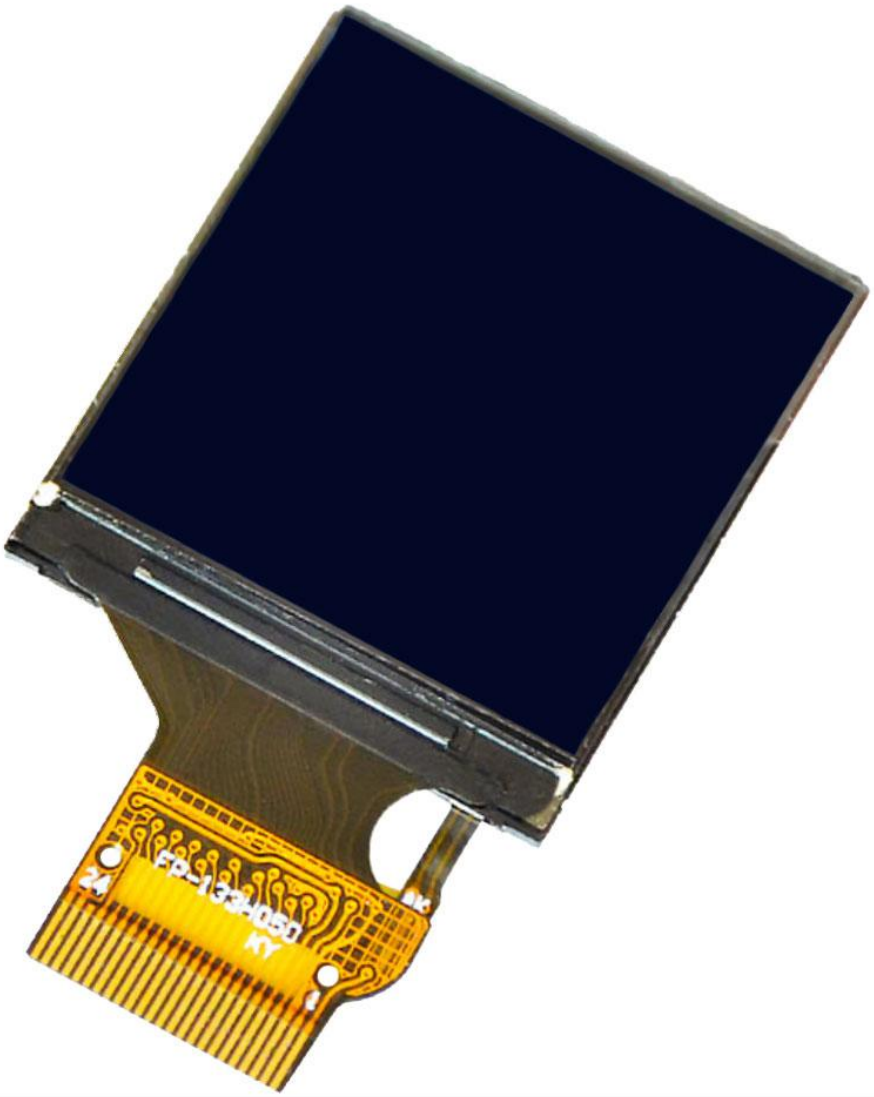
DisplayModule



DM-TFT13-377PANEL

1.3" 240 × 240 IPS TFT LCD DISPLAY PANEL-SPI

Contents

1 Revision History

Date	Changes
2020-04-03	First release

2 Main Features

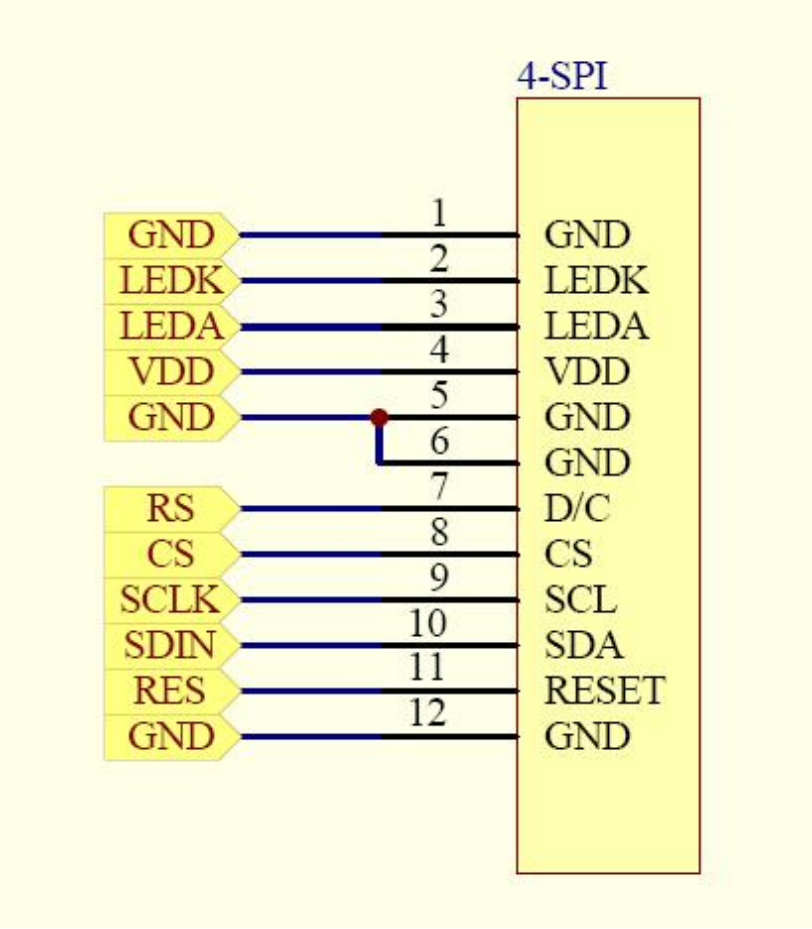
Item	Specification	Unit
Diagonal Size	1.3	inch
Display Mode	Normally black	-
Color arrangement	RGB Vtertical stripe	-
Viewing Direction	All View	-
Resolution	240(RGB) x 240	pixel
Controller IC	ST7789VW	-
Interface	4 Line SPI	-
Active Area	23.4 x 23.4	mm
Panel Dimension	26.16 x 29.22 x 1.5	mm
Pixel Pitch	0.0975 x 0.0975	mm
Backlight	2 White LED	-
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

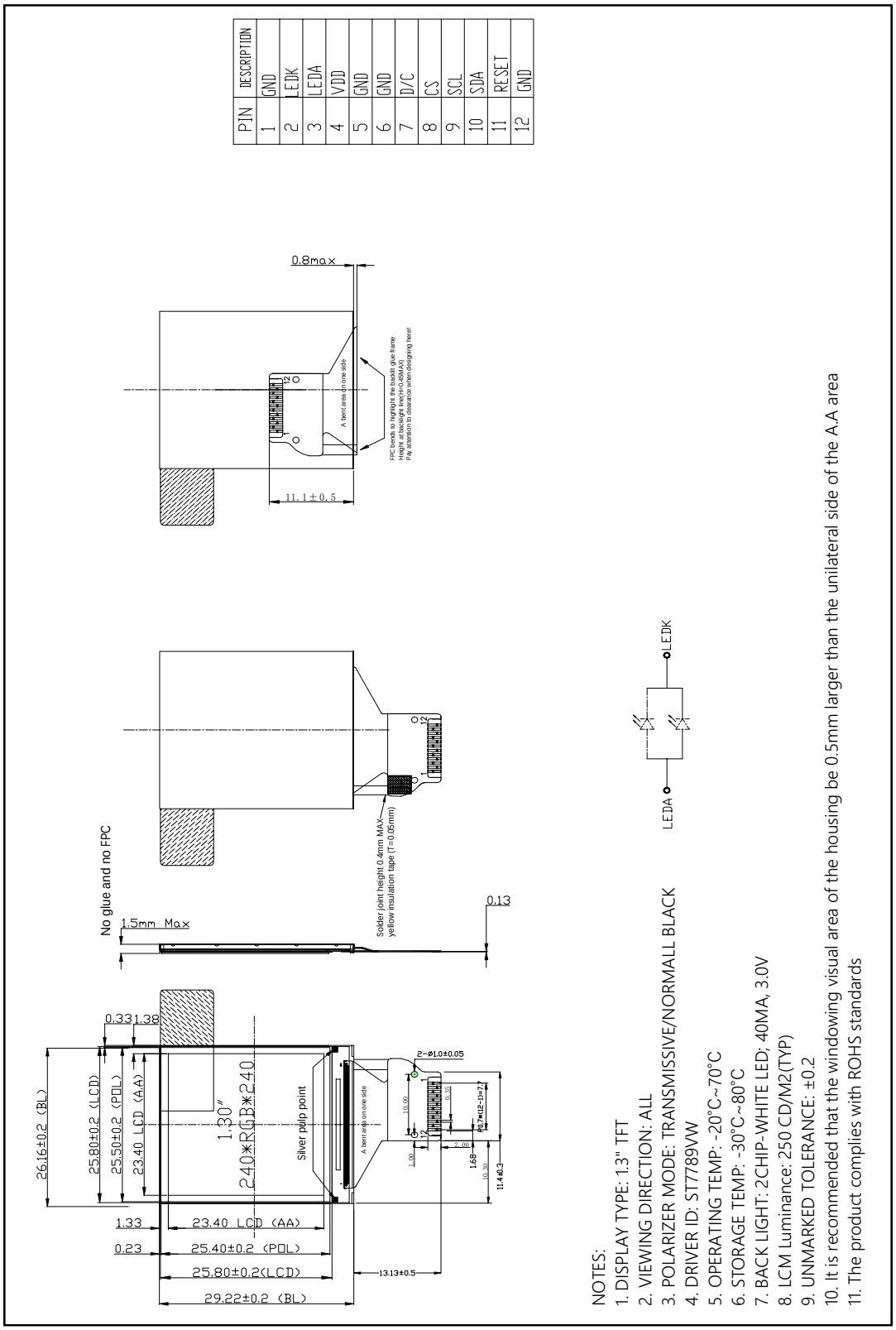
Pin No.	Symbol	Function Description
1	GND	Power Ground
2	LEDK	LED Cathode
3	LEDA	LED Anode
4	VDD	Power Supply for Analog
5	GND	Power Ground
6	GND	Power Ground
7	D/C	Display data/command selection pin in 4-line serial interface.
8	CS	Chip selection pin;Low enable,high disable.
9	SCL	This pin is used to be serial interface clock
10	SDA	SPI interface input/output pin.the data is latched on the rising edge of the SCL signal.
11	RESET	This signal will reset the device and it must be applied to properly initialize the chip.Signal is active low.
12	GND	Power Ground

Note:



4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles		-	80	-	°	-
C.I.E. (White)	(x) (y)	0.300 0.323	0.302 0.325	0.304 0.327	-	-
C.I.E(Red)	(x) (y)	0.622 0.327	0.624 0.329	0.626 0.331	-	-
C.I.E(Green)	(x) (y)	0.286 0.520	0.288 0.522	0.290 0.524	-	-
C.I.E(Blue)	(x) (y)	0.134 0.135	0.136 0.137	0.138 0.139	-	-
Response Time	Tr+Tf	-	30	35	ms	-
Contrast Ratio	CR	640	800	-	-	-
Transmittance (with polarizer)		4.18	4.65	-	%	-

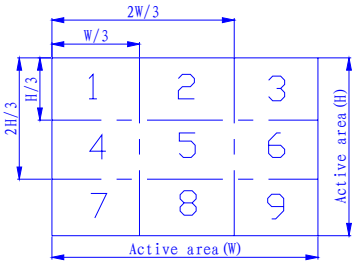
5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
I/O Supply Voltage for panel	V_{DD}	-0.3	4.6	V	-
Analog Supply Voltage for panel	V_{DDIO}	-0.3	4.6	V	-
Logic Input Voltage for panel	V_{IN}	-0.3	V_{DD}+0.3	V	-
Operating Temperature	T_{OP}	-20	70	℃	-
Storage Temperature	T_{STG}	-30	80	℃	-

5.3 DC Characteristics

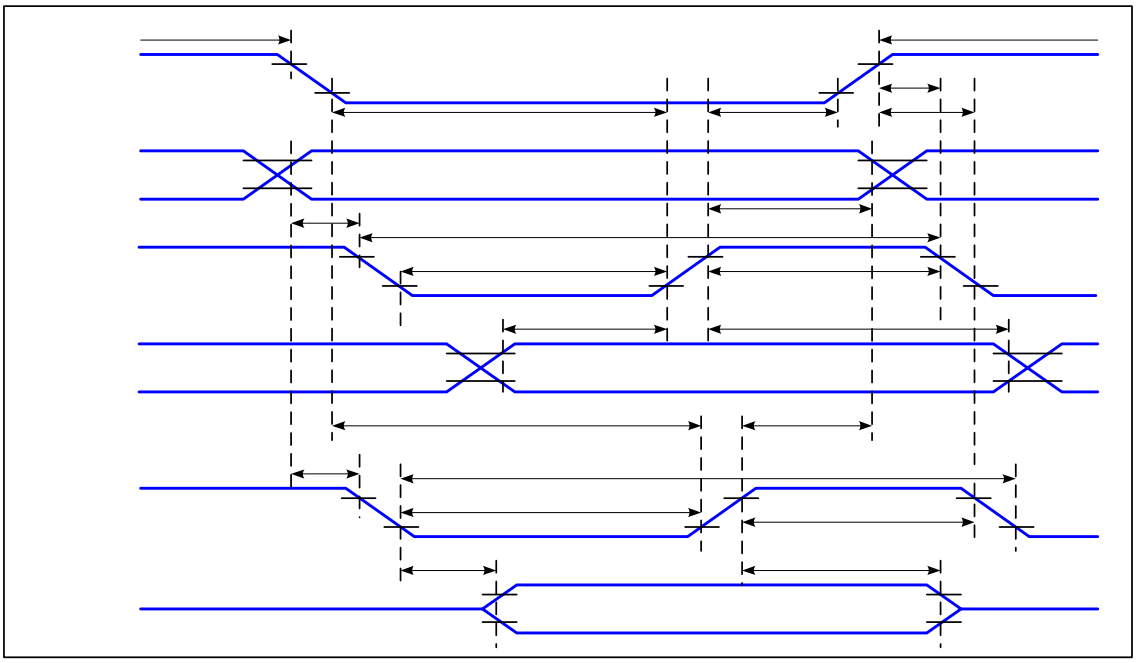
Item	Symbol	Min	Typ.	Max	Unit	Notes
Voltage for LED backlight	V_{LED}	2.8	-	3.0	V	
System Voltage	V_{DD}	2.4	2.8	3.3	V	
Interface Operation Voltage	V_{DDIO}	1.65	1.8	3.3	V	
Gate Driver High Voltage	V_{GH}	12.2	-	14.97	V	
Gate Driver Low Voltage	V_{GL}	-12.5	-	-7.16	V	
Operating Current for V_{DD}	I_{DD}	-	8	10	mA	
Current for LED backlight	I_{LED}	30	-	40	mA	2 LED
Brightness	L_{br}	200	250	-	cd/m^2	
Sleep_In Mode VDD	I_{dd}	-	15	30	μA	
Sleep_In Mode VDDIO	I_{ddio}	-	5	10	μA	

1. Test condition is:
   a：Center point on active area
   b：Best Contrast
2. Uniform measure condition:
   a：Measure 9 point,Measure location is show below:
   b：Uniform=(Min brightness/Max.brightness)x100%
   c：Best Contrast.



5.4 AC Characteristics

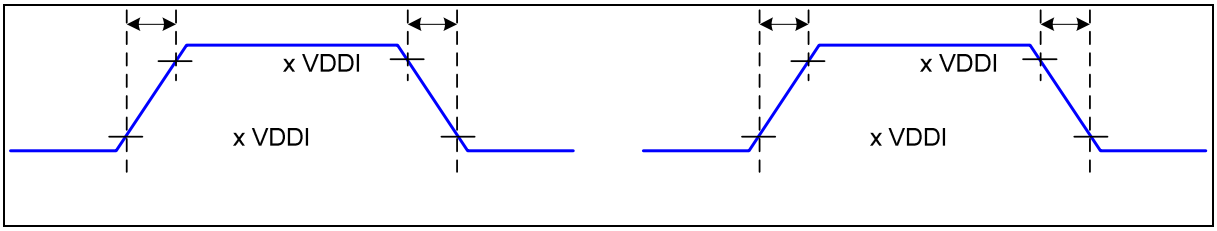
5.4.1 8080-Series MCU Parallel Interface Timing Characteristics:18/16/9/8-bit Bus



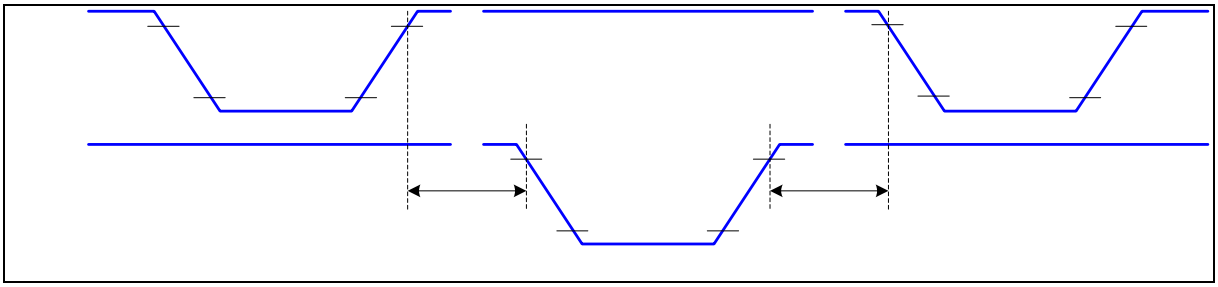
VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Description	Min	Max	Unit	Remark
D/CX	TAST	Address setup time	0	-	ns	-
	TAHT	Address hold time (Write/Read)	10	-	ns	
CSX	T_{CHW}	Chip select “H” pulse width	0	-	ns	-
	T_{CS}	Chip select setup time (Write)	15	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	45	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
	T_{CSH}	Chip select hold time	10	-	ns	
WRX	TWC	Write cycle	66	-	ns	-
	TWRH	Control pulse “H” duration	15	-	ns	
	TWRL	Control pulse “L” duration	15	-	ns	
RDX (ID)	TRC	Read cycle (ID)	160	-	ns	When read ID data
	TRDH	Control pulse “H” duration (ID)	90	-	ns	
	TRDL	Control pulse “L” duration (ID)	45	-	ns	
RDX (FM)	TRCFM	Read cycle (FM)	450	-	ns	When read from frame memory
	TRDHFM	Control pulse “H” duration (FM)	90	-	ns	
	TRDLFM	Control pulse “L” duration (FM)	355	-	ns	
D[17:0]	TDST	Data setup time	10	-	ns	For CL=30pF
	TDHT	Data hold time	10	-	ns	
	TRAT	Read access time (ID)	-	40	ns	
	TRATFM	Read access time (FM)	-	340	ns	
	TODH	Output disable time	20	80	ns	

Rising and Falling Timing for I/O Signal

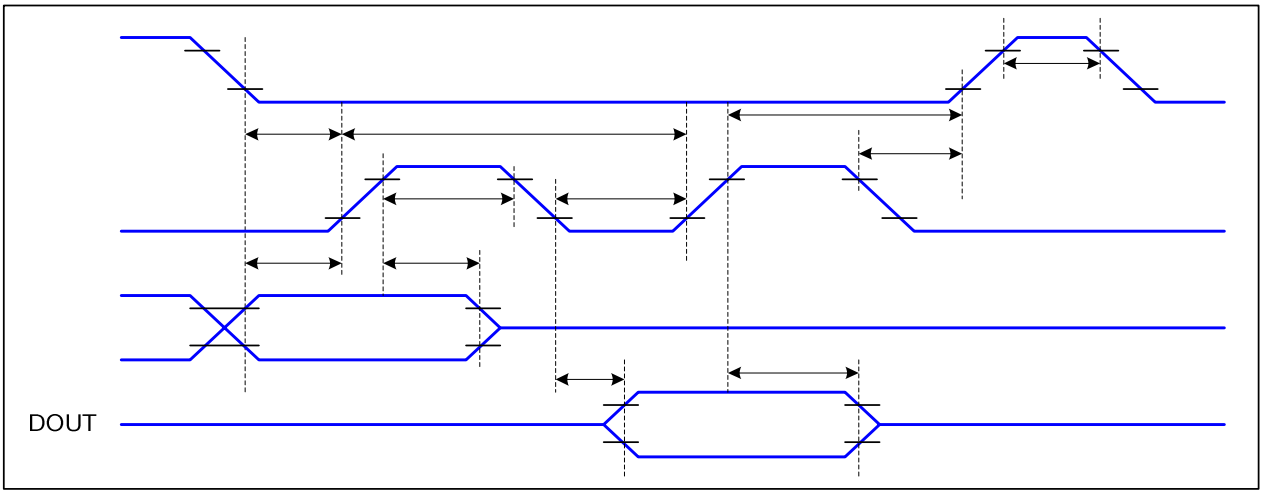


Write-to-Read and Read-to-Write Timing



Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.4.2 Serial Interface Timing Characteristics: (3-line serial)

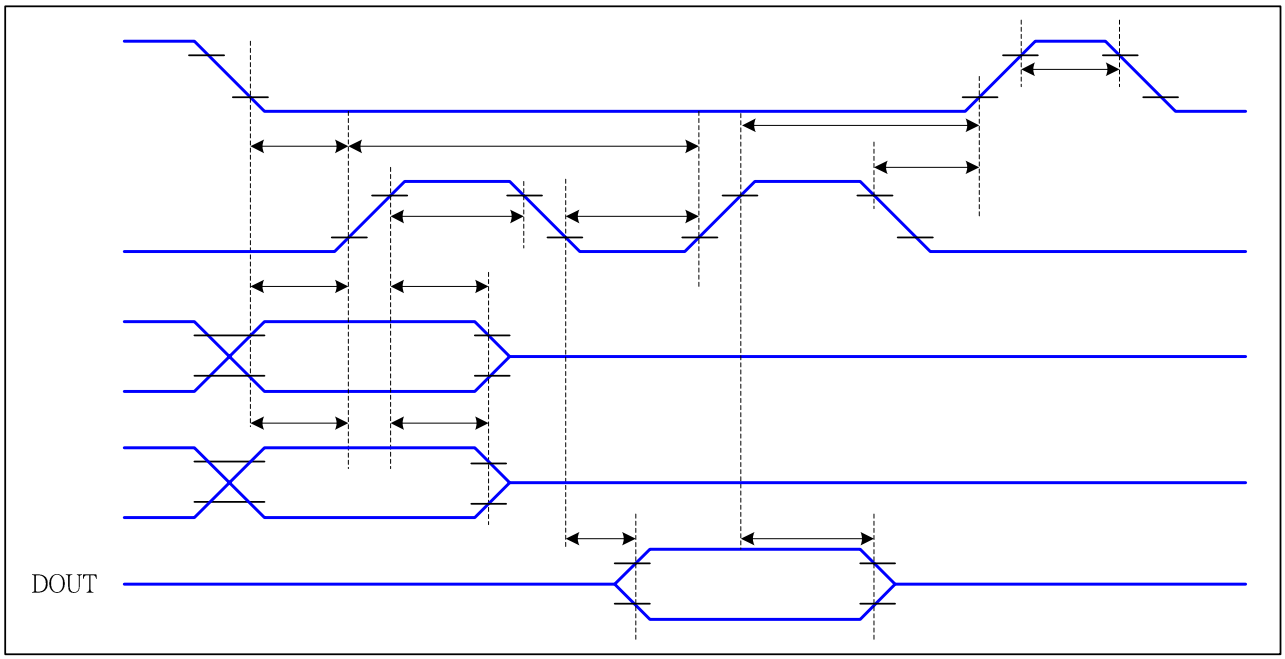


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Description	Min	Max	Unit	Remark
CSX	T_{CSS}	Chip Select Setup Time (Write)	15	-	ns	
	T_{CSH}	Chip Select Hold Time (Write)	15	-	ns	
	T_{CSS}	Chip Select Setup Time (Read)	60	-	ns	
	T_{SCC}	Chip Select Hold Time (Read)	65	-	ns	
	T_{CHW}	Chip Select “H” Pulse Width	40	-	ns	
SCL	T_{SCYCW}	Serial Clock Cycle (Write)	16	-	ns	-Write Command & Data Ram
	T_{SHW}	SCL “H” Pulse Width (Write)	7	-	ns	
	T_{SLW}	SCL “L” Pulse Width (Write)	7	-	ns	
	T_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	-Read Command & Data Ram
	T_{SHR}	SCL “H” Pulse Width (Read)	60	-	ns	
	T_{SLR}	SCL “L” Pulse Width (Read)	60	-	ns	
SDA (DIN)	T_{SDS}	Data Setup Time	7	-	ns	
	T_{SDH}	Data Hold Time	7	-	ns	
DOUT	T_{ACC}	Access Time	10	50	ns	For Maximum CL=30pF For Minimum CL=8pF
	T_{OH}	Output Disable Time	15	50	ns	

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.4.3 Serial Interface Timing Characteristics: (4-line serial)

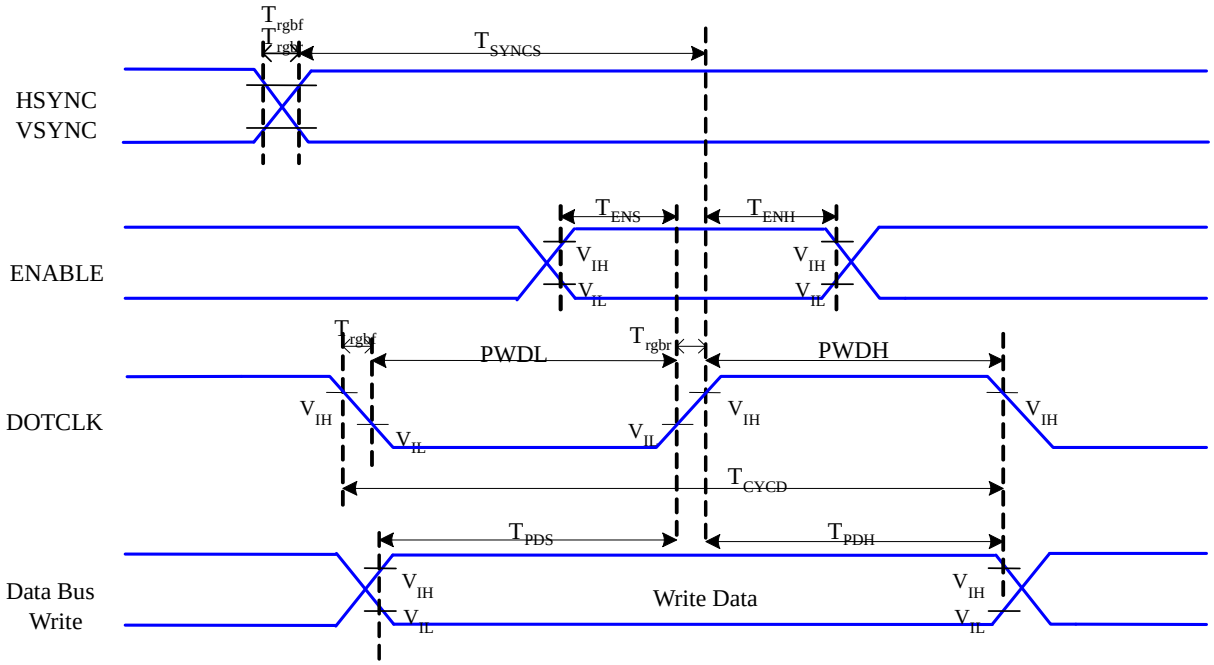


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Description	Min	Max	Unit	Remark
CSX	T_{CSS}	Chip Select Setup Time (Write)	15	-	ns	
	T_{CSH}	Chip Select Hold Time (Write)	15	-	ns	
	T_{CSS}	Chip Select Setup Time (Read)	60	-	ns	
	T_{SCC}	Chip Select Hold Time (Read)	65	-	ns	
	T_{CHW}	Chip Select “H” Pulse Width	40	-	ns	
SCL	T_{SCYCW}	Serial Clock Cycle (Write)	16	-	ns	-Write Command & Data Ram
	T_{SHW}	SCL “H” Pulse Width (Write)	7	-	ns	
	T_{SLW}	SCL “L” Pulse Width (Write)	7	-	ns	
	T_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	-Read Command & Data Ram
	T_{SHR}	SCL “H” Pulse Width (Read)	60	-	ns	
	T_{SLR}	SCL “L” Pulse Width (Read)	60	-	ns	
D/CX	T_{DCS}	D/CX setup time	10	-		
	T_{DCH}	D/CX hold time	10	-		
SDA (DIN)	T_{SDS}	Data Setup Time	7	-	ns	
	T_{SDH}	Data Hold Time	7	-	ns	
DOUT	T_{ACC}	Access Time	10	50	ns	For Maximum CL=30pF For Minimum CL=8pF
	T_{OH}	Output Disable Time	15	50	ns	

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.4.4 RGB Interface Timing Characteristics:



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25 ℃

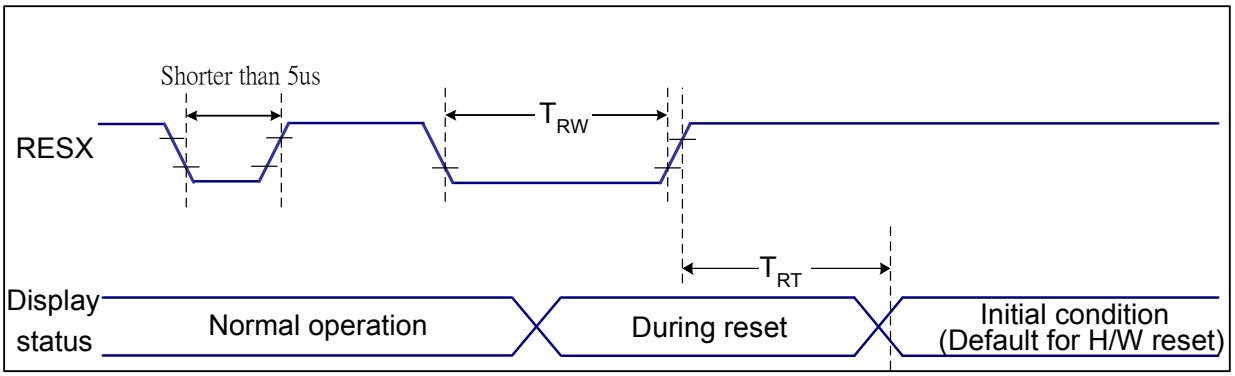
18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Description	Min	Max	Unit	Remark
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

6 Bits RGB Interface Timing Characteristics

Signal	Symbol	Description	Min	Max	Unit	Remark
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	
	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

5.4.5 RESET Timing



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25 °C

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	T_{RW}	Reset pulse duration	10	-	µs
	T_{RT}	Reset cance	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

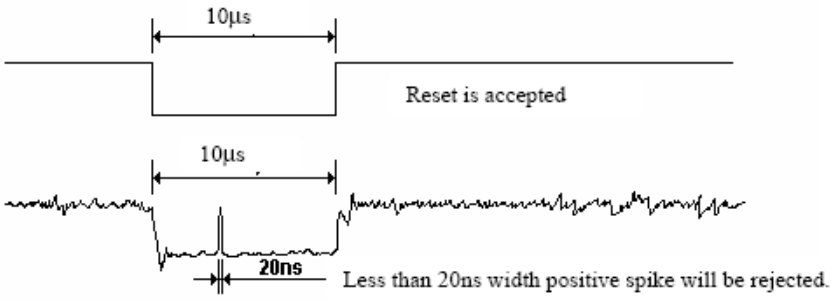
Note 1:The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5µs	Invalid Reset
Longer than 10µs	Valid Reset
Between 5µs and 10µs	Reset starts (It depends on voltage and temperature condition.)

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

Note 4:Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6:When Reset applied during Sleep Out Mode.

Note 7:It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 120hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30°C 120hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 120hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 120hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	50°C,85%RH 120hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-10°C/60°C 12 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

7 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"