DisplayModule

DM-TFT13-330

1.33’ REFLECTIVE TFT ACTIVE MATRIX COLOR MEMORY LCD

Contents

1 Revision History

Date	Changes
2015-06-25	First release

2 Main Features

Item	Specification	Unit
Resolution	128 x 128	Pixels
Module Dimension	26.82 x 31.3 x 0.745	mm
Dot pitch	0.062 x 0.186	mm
View Area	23.808 x 23.808	mm-
Pixel Arrangement	Stripe Array	
Display Colors	8 colors	-
Surface Treatment	Anti-Glare	
Weight	TBD	g

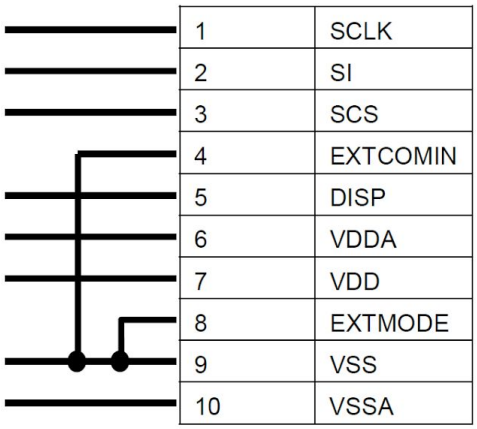
3 Pin Description

No.	Symbol	Description
1	SCLK	Serial clock signal
2	SI	Serial data input signal
3	SCS	Chip select signal (Active of Hi)
4	EXTCOMIN	External COM inversion signal input (Square wave)
5	DISP	Display ON/OFF signal
6	VDDA	Power supply (Analog)
7	VDD	Power supply (Digital)
8	EXTMODE	Control mode of COM inversion is select terminal
9	VSS	GND (Digital)
10	VSSA	GND (Analog)

Recommended Circuit

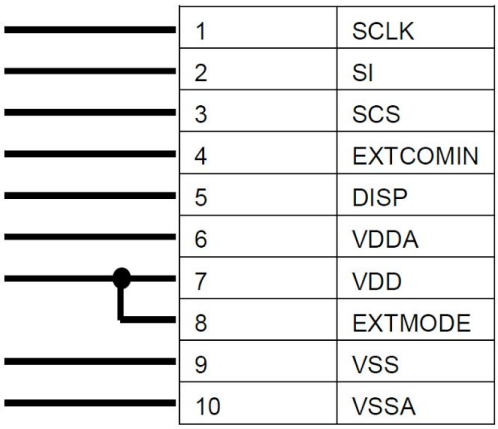
< EXTMODE="Lo" >

COM Signal Serial Flag Input

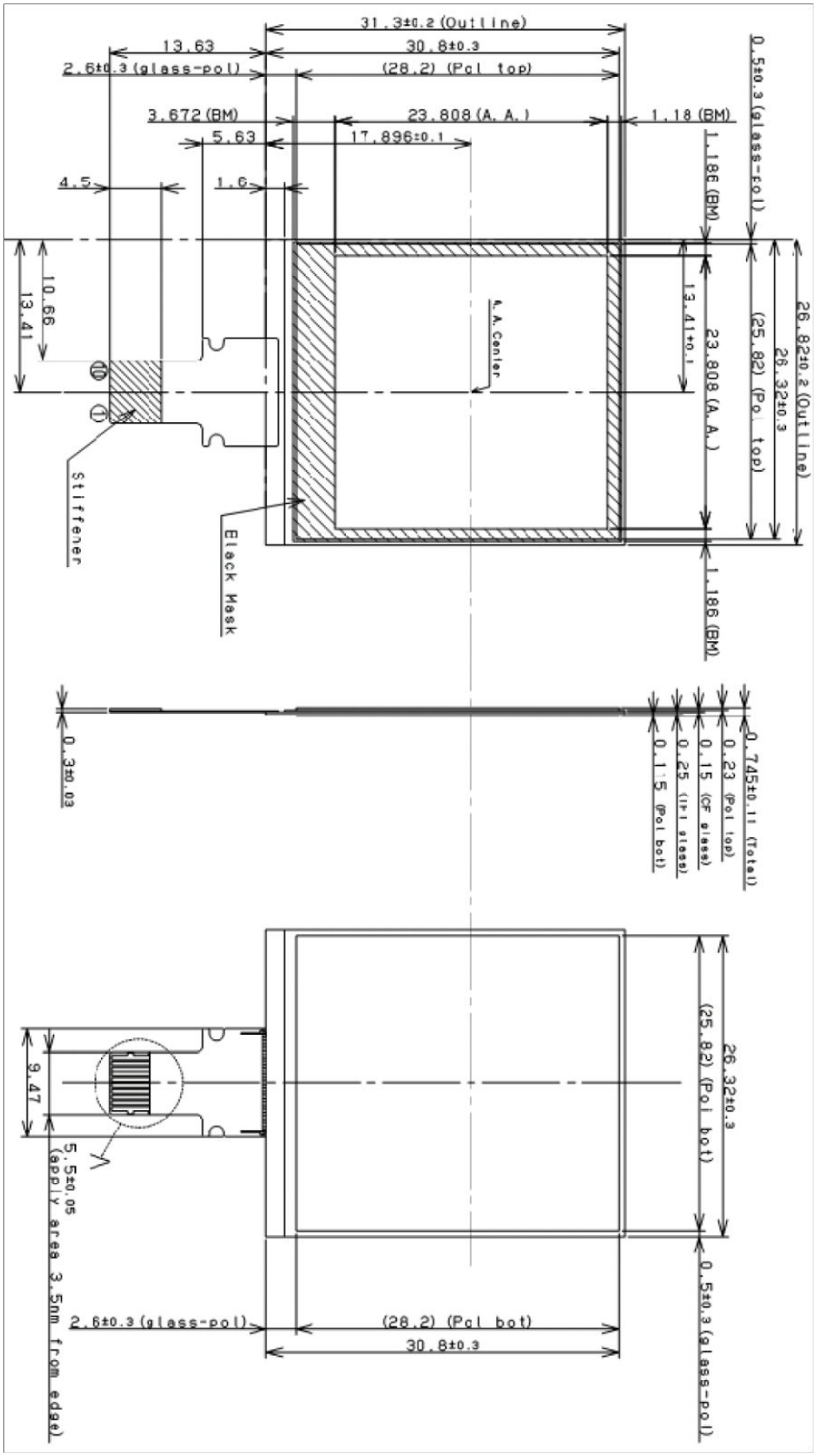


< EXTMODE="Hi" >

External COM Signal Input



4 Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD		4.8	5.0	5.5	V
Analog Power	VCC					V
Low Level Input Voltage	V_{IL}		VSS	VSS	VSS+0.15	V
High Level Input Voltage	V_{IH}		2.7	3.0	VDD	V
Low Level Output Voltage	V_{OL}					V
High Level Output Voltage	V_{OH}					V
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃

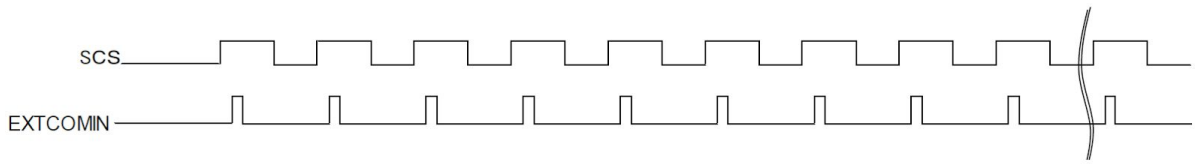
6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles Vertical	AV	40	TBD	-	
View Angles Horizontal	AH	40	TBD	-	
Response Time	Tr +Tf	-	30	-	sec
Contrast Ratio	CR	TBD	TBD	-	-
Reflectance	R%	TBD	9	-	%

7 Timing Character

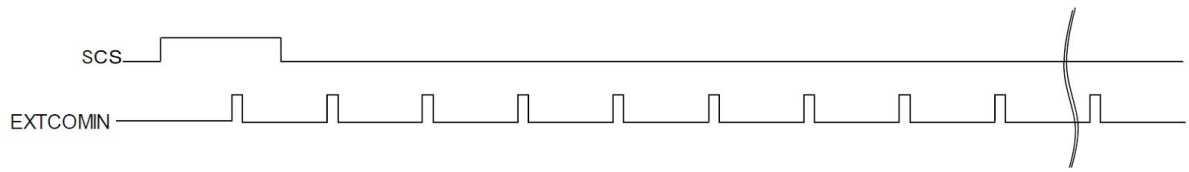
Item	Symbol	Min	Typ	Max	Unit
Frame frequency	fSCS	1	1	35	Hz
Clock frequency	fSCLK	-	1	2	MHz
Vertical Interval	tV	28.6	-	1000	ms
COM Frequency	fCOM	0.5	-	17.5	Hz
SCS Rising Time	trSCS	-	-	50	ns
SCS Falling Time	tfSCS	-	-	50	ns
SCS High duration	twSCSH	212	-	-	us
		12	-	-	us
SCS Low duration	twSCSL	1	-	-	us
SCS set up time	tsSCS	3	-	-	us
SCS hold time	thSCS	1	-	-	us
SI Rising time	trSI	-	-	50	ns
SI Folling time	tfSI	-	-	50	ns
SI set up time	tsSI	120	-	-	ns
SI hold time	thSI	190	-	-	ns
SCLK Rising time	trSCLK	-	-	50	ns
SCLK Folling time	tfSCLK	-	-	50	ns
SCLK High duration	twSCLKH	200	450	-	ns
SCLK Low duration	twSCLKL	200	450	-	ns
EXTCOMIN signal frequency	fEXTCOMIN	1	1	35	Hz
EXTCOMIN signal rising time	trEXTCOMIN	-	-	50	ns
EXTCOMIN signal folling time	twEXTCOMIN	-	-	50	ns
EXTCOMIN signal High duration	thlEXTCOMIN	1	-	-	us
DISP Rising time	trDISP	-	-	50	ns
DISP Folling time	tfDISP	-	-	50	ns

When data is writtne for displaying continuously, EXTCOMIN frequency should be made the same frame frequency or lower.

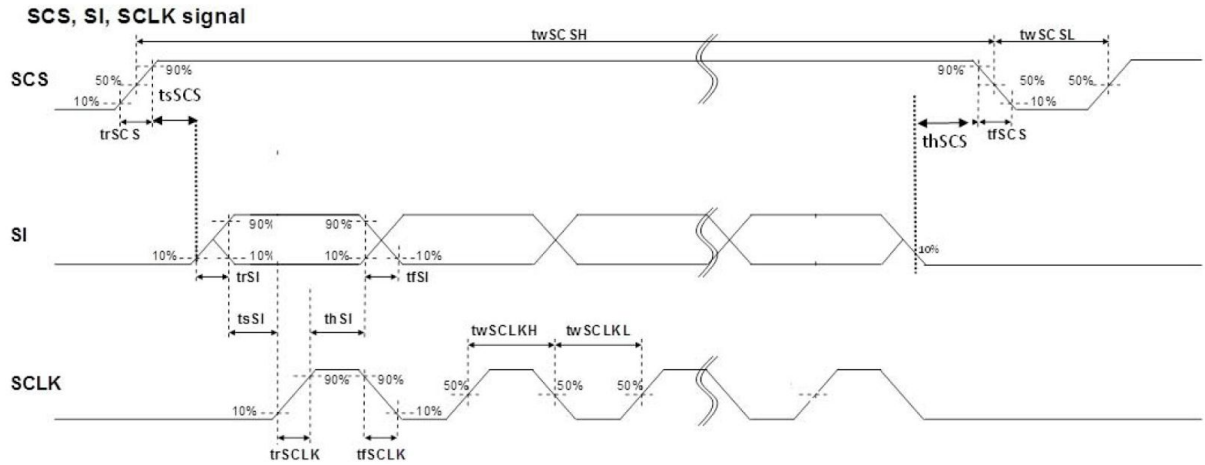


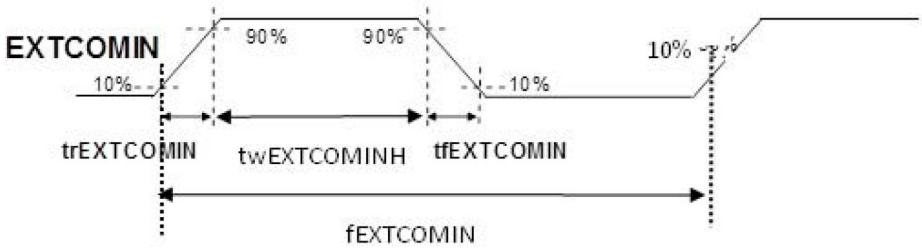
When the display is maintained after writing of the displayed data, is not applied.

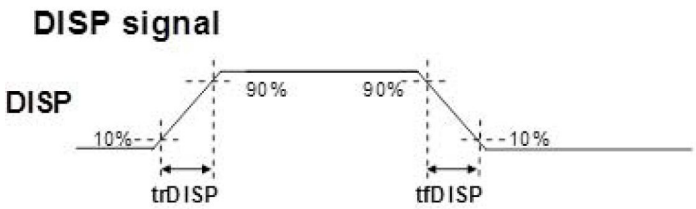
(Please keep SCS in the state of L when you maintain current display after writing of the display data.)



Signal Timing







*SCS, SI, SCLK, DISP, EXTCOMIN: 3V input voltage

8 Power Consumption

Current Consumption Ta=25℃,SCS SCLK,Si,DISP,EXTCOMIN=+3V ,VDD=+5V, VDDA=+5V

Operation Mode	Power consumption	Min	Typ	Max	Unit
Condition 1	Display mode (no display data update) Display pattern : Black display		TBD	TBD	uW
Condition 2	Data update mode with display update 1Hz (1fram/sec) Display pattern : Vertical stripe display		TBD	TBD	uW

Common inversion with VDD=5.0V、VDDA=5.0V、fCLK=1.0MHz、EXTMODE=VDD、EXTCOMIN=1Hz

(Common Note)

This is value in steady condition, not the falue of peak power at the time of COM operation.

Some marging for power supply is recommended.

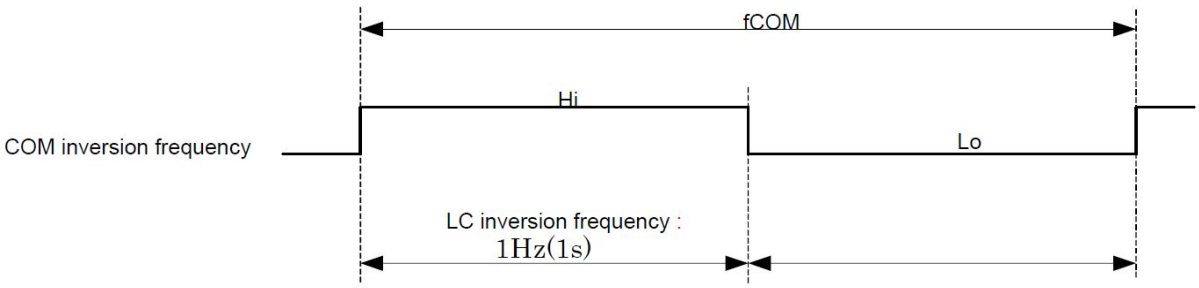
We recommend capacitor for VDD and VDDA.

(If VDD and VDDA are on separate systems, we recommend capacitor for each.)

*LC inversion : LC material is needed alternative polarity driving as changing timing which should be 1Hz.

(LC inversion frequency 1Hz is COM frequency 1Hz)

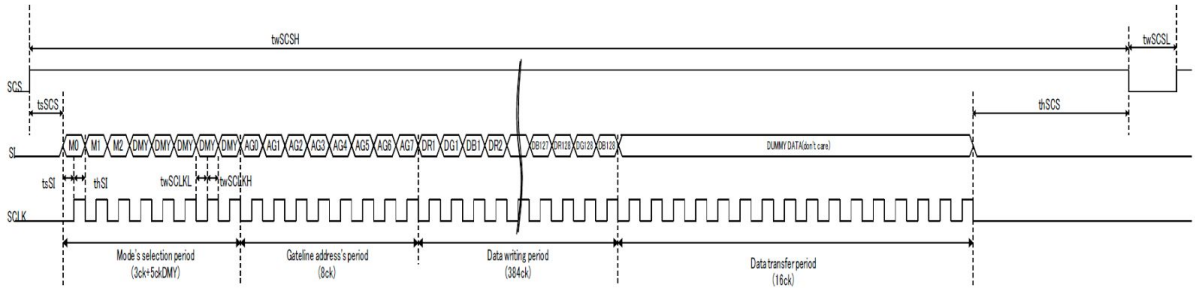
as shown COM inversion frequency



9 Input Signal Timing Chart

9.1 Data update mode (1 line)

Updates data of only one specified line. (M0="Hi"、M2="Lo")



Data update mode by 1line

M0: Mode flag.

Set for "Hi". Data update mode (Memory internal data update)

When "Lo", display mode (maintain memory internal data).

M1: Frame inversion flag.

When "Hi", outputs VCOM="Hi", and when "Lo", outputs VCOM="Lo".

When EXTMODE="Hi", it can be "Hi" or "Lo".

M2: All clear flag.

Refer to All Clear Mode to execute clear.

DUMMY DATA: Dummy data. It can be "Hi" or "Lo" ("Lo" is recommended.)

※ Data write period

Data is being stored in 1st latch block of binary driver on panel.

※ Data transfer period

Data written in 1st latch is being transferred (written) to pixel internal memory circuit

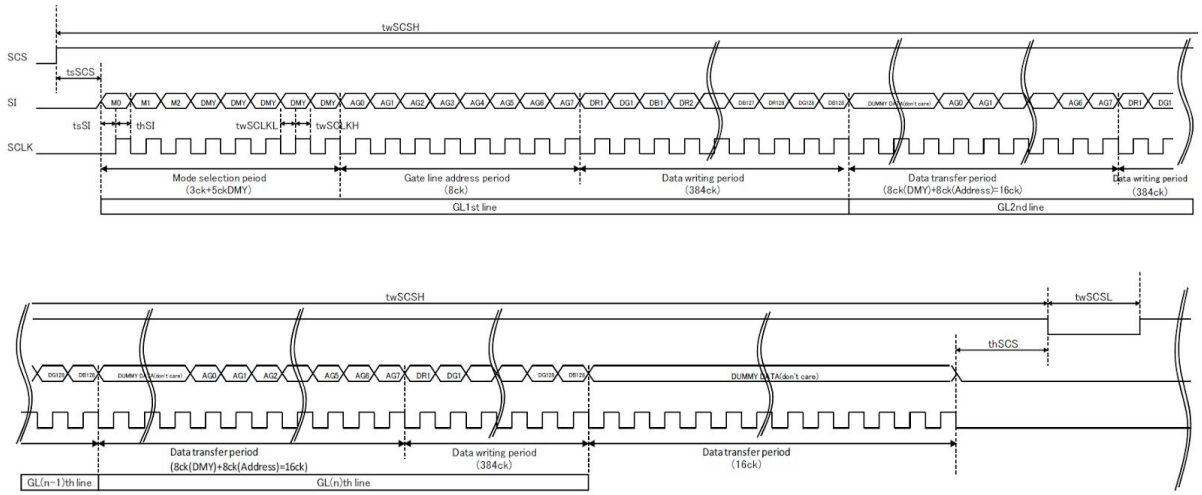
※For gate line address setting, refer to 6-7) Input Signal and Display.

※M1: Frame inversion flag is enaled when EXTMODE="Lo".

※When SCS becomes "Lo", M0 and M2 are cleared.

9.2 Data Update Mode (Multiple Lines)

Updates arbitrary multiple lines data. (M0="Hi"、M2="Lo")



Data update mode by Multiple Lines

M0: Mode flag.

Set for "Hi". Data update mode (Memory internal data update)

When "Lo", display mode (maintain memory internal data).

M1: Frame inversion flag.

When "Hi", outputs VCOM="Hi", and when "Lo", outputs VCOM="Lo".

When EXTMODE="Hi", it can be "Hi" or "Lo".

M2: All clear flag.

Refer to 6-6-4) All Clear Mode to execute clear.

DUMMY DATA: Dummy data. It can be "Hi" or "Lo" ("Lo" is recommended.)

※ Data write period

Data is being stored in 1st latch block of binary driver on panel.

※ Data transfer period

For example, during GL2nd line data transfer period, GL 2nd line address is latched and GL1stline data is transferred from 1st latch to pixel internal memory circuit at the same time.

※ For gate line address setting, refer to 6-7) Input Signal and Display.

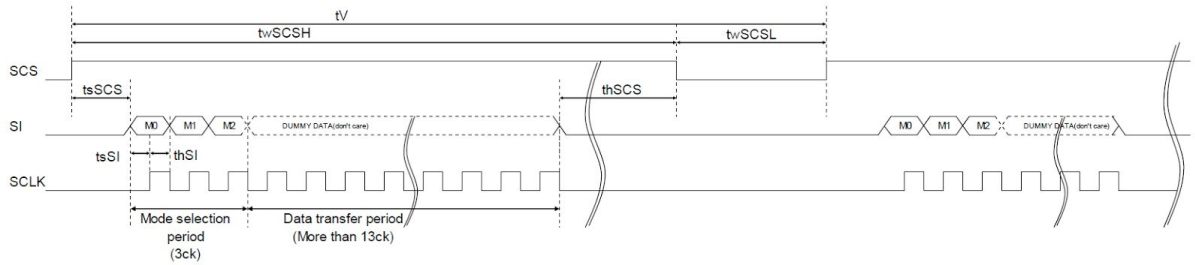
※ Input data continuously.

※ M1: Frame inversion flag is enabled when EXTMODE="Lo".

※ When SCS becomes "Lo", M0 and M2 are cleared.

9.3 Display Mode

Maintains memory internal data (maintains current display). (M0="Lo"、M2="Lo")



Display mode

M0: Mode flag.

Set for "Hi". Data update mode (Memory internal data update)

When "Lo", display mode (maintain memory internal data).

M1: Frame inversion flag.

When "Hi", outputs VCOM="Hi", and when "Lo", outputs VCOM="Lo".

When EXTMODE="Hi", it can be "Hi" or "Lo".

M2: All clear flag.

Refer to All Clear Mode to execute clear.

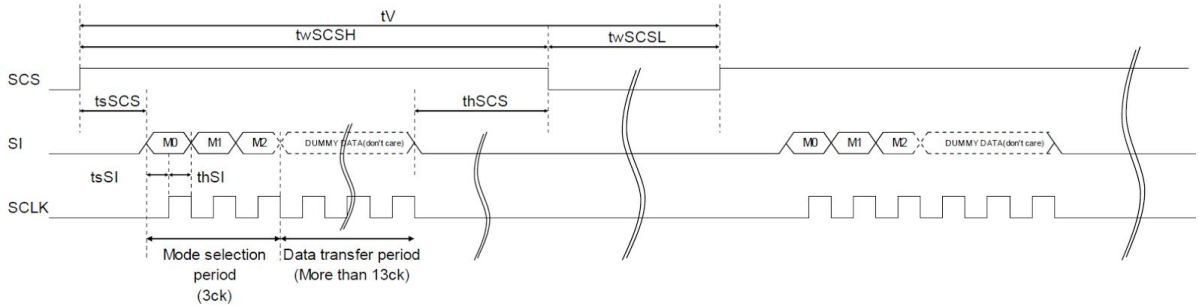
DUMMY DATA: Dummy data. It can be "Hi" or "Lo" ("Lo" is recommended.)

※ M1: Frame inversion flag is enabled when EXTMODE="Lo"

※ When SCS becomes "Lo", M0 and M2 are cleared.

9.4 All Clear Mode

Clears memory internal data and writes white. (M0="Lo"、M2="Hi")



All Clear mode

M0: Mode flag.

Set it "Lo".

M1: Frame inversion flag.

When "Hi", outputs VCOM="Hi", and when "Lo", outputs VCOM="Lo".

When EXTMODE="Hi", it can be "Hi" or "Lo".

M2: All clear flag.

Set it "Hi"

DUMMY DATA: Dummy data. It can be "Hi" or "Lo" ("Lo" is recommended.)

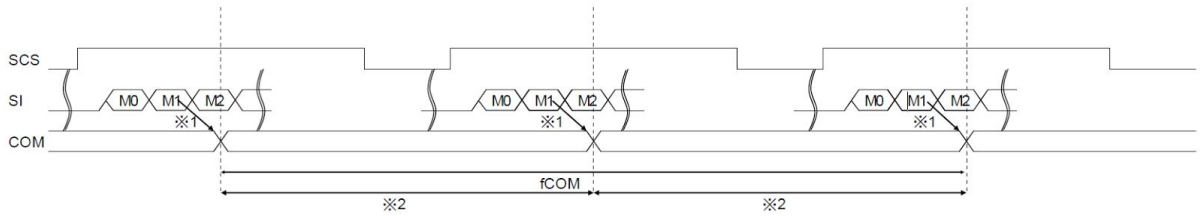
※ M1: Frame inversion flag is enabled when EXTMODE="Lo".

※ When SCS becomes "Lo", M0 and M2 are cleared.

9.5 COM Inversion

There are two types of inputs,COM signal serial input (EXTMODE="Lo") and external COM signal input (EXTMODE="Hi").

EXTMODE="Lo"



COM Inversion (EXTMODE=Lo)

M1 : LC polarity inversion flag:

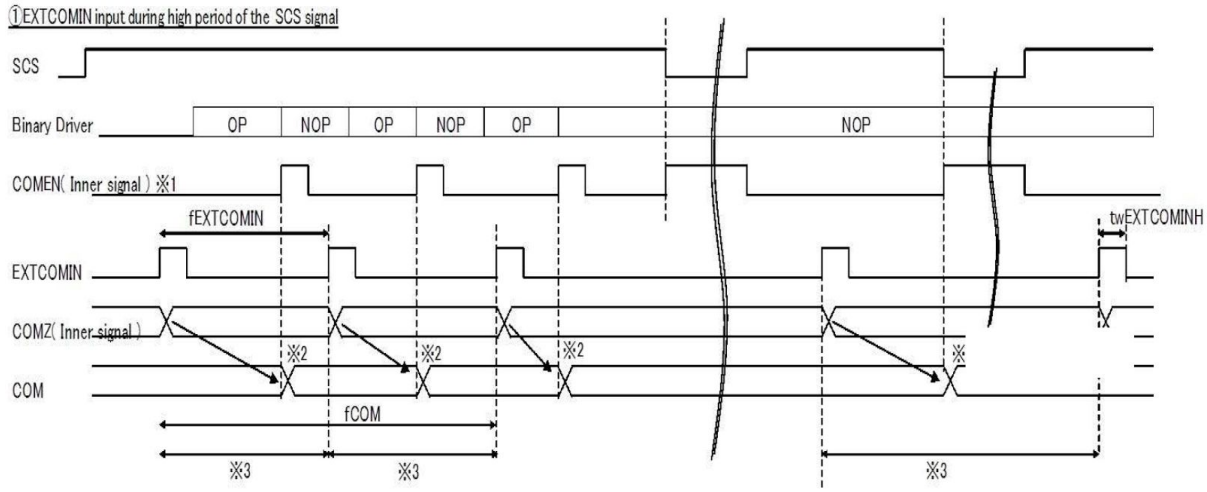
If M1 is "Hi" then VCOM="Hi" is output.

If M1 is "Lo" then VCOM="Lo" is output.

※1 : LC inversion has been changed by M1 flag statement.

※2 : The periods of plus polarity and minus polarity should be same length as much as possible.

EXTMODE="Hi" （COM inversion timing has two conditions）



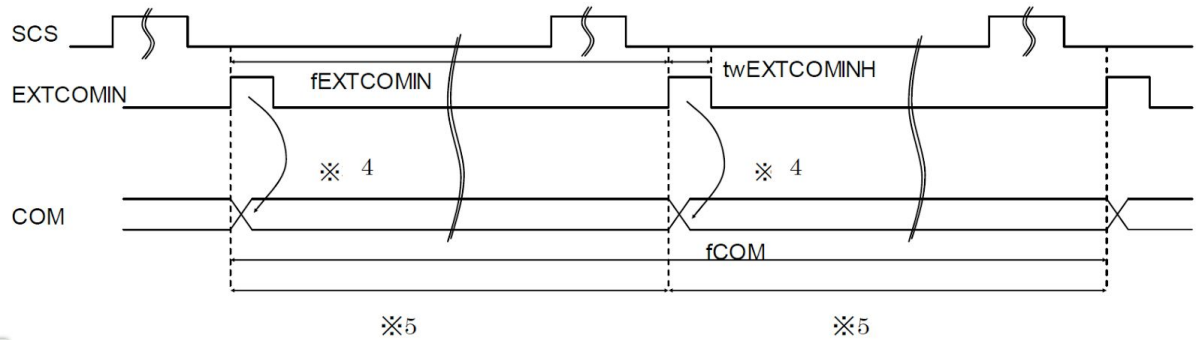
※1: COMEN is High when "SCS=Low" and certain period after Binary Drivere operation

※2: Make "COM" reversal depending on COMZ at the COMEN's rise time

※3: The period of EXTCOMIN should be constant

And the period of EXTCOMIN should be constant depending on EXTCOMIN.(with Binary Driver operate or making the period of "SCS=lOW"

②: the EXTCOMIN input during low period of the SCS signal



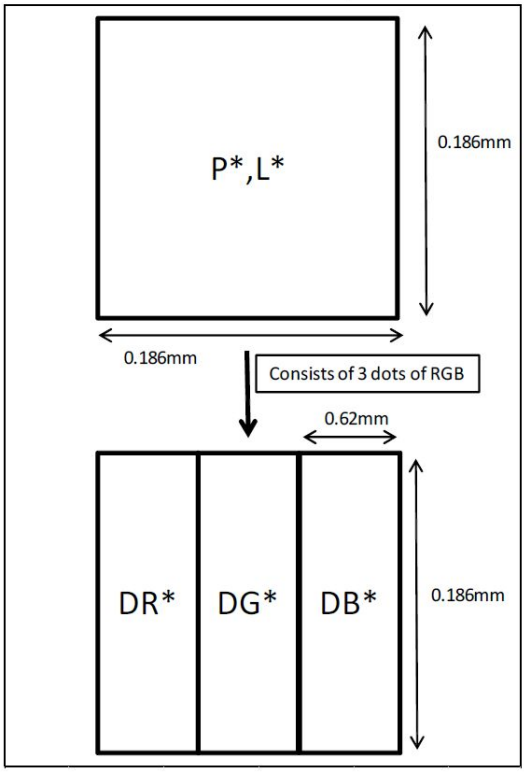
※4：LC inversion polarity has been set by the rising edge of EXTCOMIN.

※5：The period of EXTCOMIN should be constant.

COM Inversion (EXTMODE=Hi)2

10 Input Signal and Display, Gate address(Line) Setting

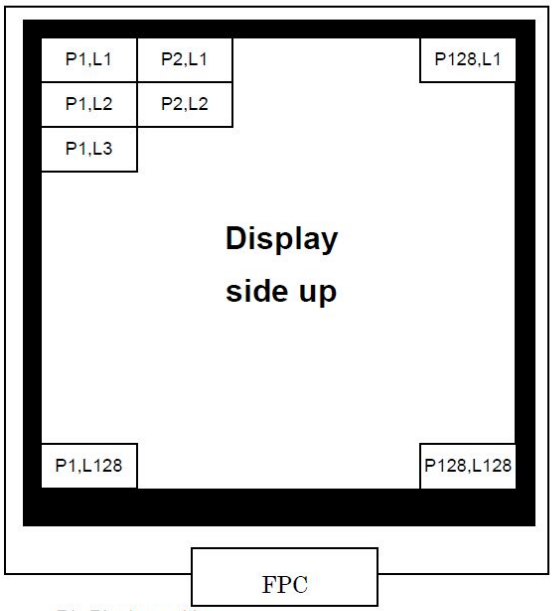
<Block diagram of the pixel>



<Color Data Table>

Color	DR*	DG*	DB*
Black	0	0	0
Red	1	0	0
Green	0	1	0
Yellow	1	1	0
Blue	0	0	1
Magenta	1	0	1
Cyan	0	1	1
White	1	1	1

<Data position in display[H,V]>



P: Pixels position*

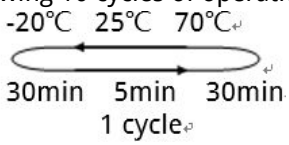
L:Gate address line*

<Gate line address setting>

GL	AG0	AG1	AG2	AG3	AG4	AG5	AG6	AG7
1	1	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0
3	1	1	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0
5	1	0	1	0	0	0	0	0
7	0	1	1	0	0	0	0	0
8	1	1	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:
121	1	0	0	1	1	1	1	0
122	0	1	0	1	1	1	1	0
123	1	1	0	1	1	1	1	0
124	0	0	1	1	1	1	1	0
125	1	0	1	1	1	1	1	0
126	0	1	1	1	1	1	1	0
127	1	1	1	1	1	1	1	0
128	0	0	0	0	0	0	0	1

GL: Gate address line

11 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.
Note3: Test performed on product itself, not inside a container

12 Warranty and Conditions

http://www.displaymodule.com/pages/faq