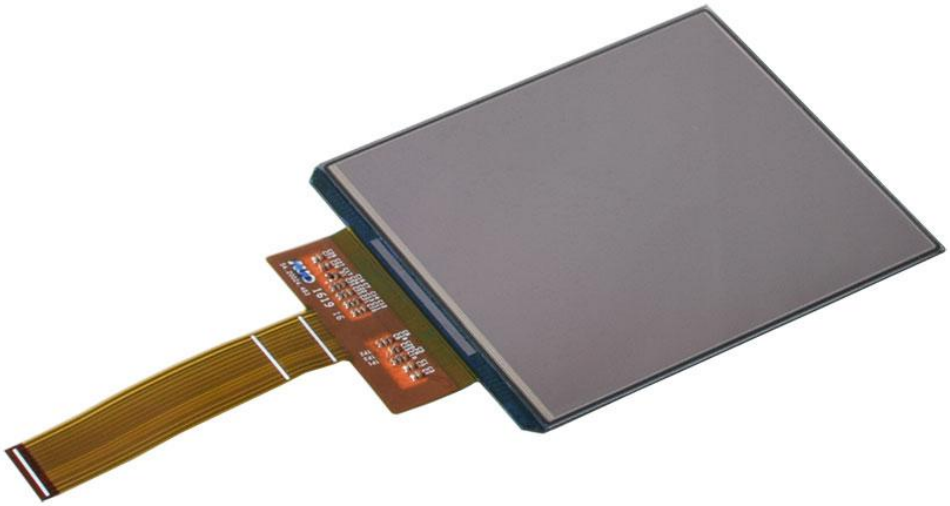
DisplayModule



DM-OLEDC38-652

3.81" 1080 × 1200 AMOLED HIGH RESOLUTION DISPLAY PANEL-MIPI

Contents

1 Revision History

Date	Changes
2019-07-04	First release

2 Main Features

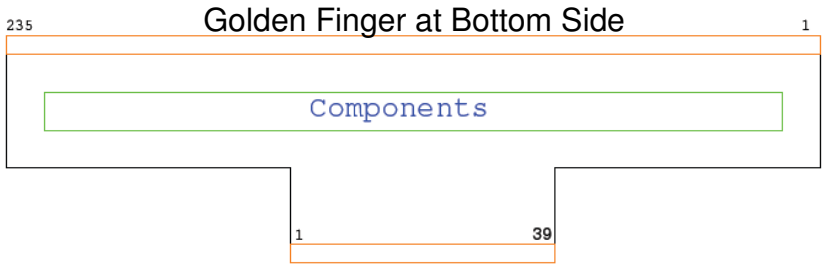
Item	Specification	Unit
Diagonal Size	3.81	inch
Display Mode	AMOLED	-
Display Colors	16.7M(Maximum)	Colors
Resolution	1080 x 1200	pixel
Controller IC	Raydium RM69071	-
Interface	MIPI	-
Active Area	64.8 x 72	mm
Panel Dimension	67.6 x 78.95 x 1.14	mm
Pixel Pitch	60	μm
Weight	TBD	g

3 Pin Description

Pin No.	Symbol	Function Description
1	OVSS	OLED Power
2	OVSS	OLED Power
3	OVSS	OLED Power
4	OVDD	OLED Power
5	OVDD	OLED Power
6	OVDD	OLED Power
7	GND	Ground
8	D2N	MIPI DSI data
9	D2P	MIPI DSI data
10	GND	Ground
11	D0N	MIPI DSI data
12	D0P	MIPI DSI data
13	GND	Ground
14	CLKN	MIPI DSI clock
15	CLKP	MIPI DSI clock
16	GND	Ground
17	D1N	MIPI DSI data
18	D1P	MIPI DSI data
19	GND	Ground
20	D3N	MIPI DSI data
21	D3P	MIPI DSI data
22	GND	Ground
23	IOVCC	Display Driver Digital Power
24	IOVCC	Display Driver Digital Power
25	VCI	Display Driver Analog Power
26	VCI	Display Driver Analog Power
27	RESX	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
28	SWIRE	DC/DC power IC control signal, please connect to power IC CTRL pin
29	AVDD_EN	DC/DC power IC control signal, please connect to power IC EN pin
30	MTP	Leave this pin OPEN
31	GND	Ground
32	AVDD	Display Driver IC Source Analog Power
33	AVDD	Display Driver IC Source Analog Power
34	OVDD	OLED Power
35	OVDD	OLED Power
36	OVDD	OLED Power
37	OVSS	OLED Power
38	OVSS	OLED Power
39	OVSS	OLED Power

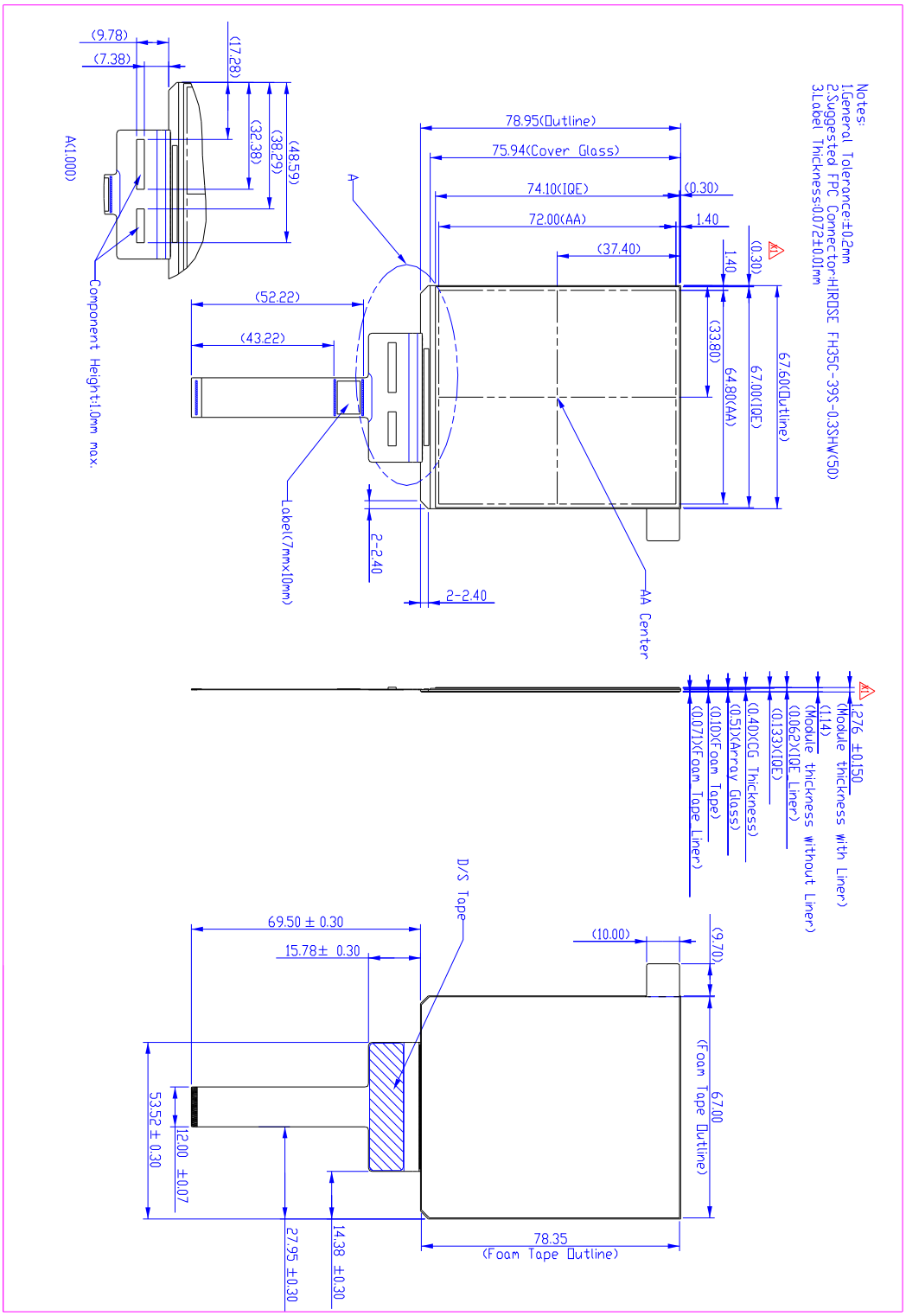
Recommended connector: Hirose FH35C-39S-0.3SHW(50)

FPC Outline



4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles TOP	Θ U	80	-	-	°	CR > 480
View Angles Bottom	Θ D	80	-	-	°	
View Angles Right	Θ R	80	-	-	°	
View Angles Left	Θ L	80	-	-	°	
C.I.E(Red)	(x) (y)	0.64 0.30	0.67 0.33	0.70 0.36	-	C.I.E.1931; Note 1
C.I.E(Green)	(x) (y)	0.186 0.661	0.236 0.711	0.286 0.761	-	
C.I.E(Blue)	(x) (y)	0.090 0.025	0.130 0.065	0.170 0.105	-	
C.I.E(White)	(x) (y)	0.28 0.29	0.30 0.31	0.32 0.33	-	
Uniformity	9 points	70	-	-	%	Note 2
Pixel Luminance	L_{br}	80	100	-	nits	-
Contrast Ratio	@ θ=0°	3000	-	-	-	-
	@ θ=60°	900	-	-	-	-
	@ θ=80°	480	-	-	-	-

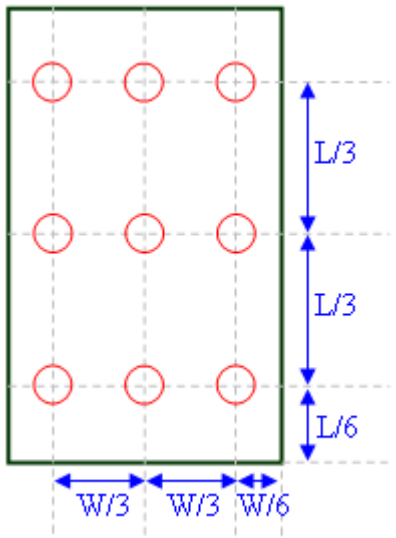
Note 1: Chromacity

Chromacity of R, G, B pattern are measured at Gray Level “255”.

Chromacity of White pattern are measured at Gray Level “255”.

Note 2: Uniformity

$$\text{Uniformity under } \textbf{White(L255)} \text{ pattern} = \frac{\text{minimum luminance of } \textbf{9}}{\text{maximum luminance of } \textbf{9}}$$



5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V_{CI}	-0.3	3.2	V
Digital Supply Voltage	IOVCC	-0.3	1.95	V
Driver IC Source Power Supply	AVDD	-	5.8	V
OLED Power Supply	OVDD	-	4.6	V
OLED Power Supply	OVSS	-	-2.9	V
Operating Temperature (Ambient)	T_{opr}	-20	70	℃
Storage Temperature (Ambient)	T_{stg}	-40	80	℃

Note：If the module exceeds the absolute maximum ratings, it may be damaged permanently.Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

5.3 DC Characteristics

5.3.1 Display DC Characteristics

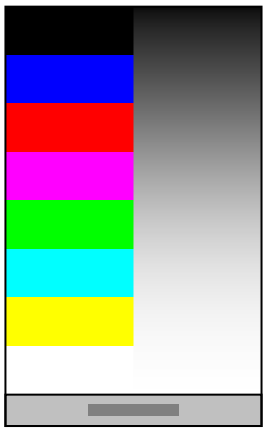
Item	Symbol	Min	Typ.	Max	Unit	Remark
Analog Supply Voltage	V_{CI}	2.8	3	3.2	V	
Digital Supply Voltage	IOVCC	1.65	1.8	1.95	V	
Driver IC Source Power Supply	AVDD	-	5.8	-	V	
OLED Power Supply	OVDD	-	4.6	-	V	
OLED Power Supply	OVSS	-	-2.9	-	V	
Low Level Input Voltage	V_{IL}	0	-	0.2 x IOVDD	V	RESX
High Level Input Voltage	V_{IH}	0.8 x IOVDD	-	IOVDD	V	RESX

Note: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

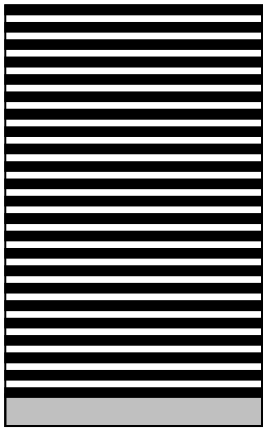
5.3.2 Display Current Consumption

Item	Symbol	Condition	Min	Typ.	Max	Unit	Remark
Normal IC	I_{AVDD}	AVDD=5.8V VCI=3V IOVDD=1.8V OVDD=4.6V OVSS=-2.9V 25℃	-	15	30	mA	Note 1
	I_{VCI}		-	3	3	mA	
	I_{IOVCC}		-	38	40	mA	
	I_{IOVDD}		-	-	16	mA	Note 2
	I_{IOVSS}		-	-	16	mA	
Idle IC	I_{AVDD}		-	-	1	μA	Display Off
	I_{VCI}		-	-	3	mA	
	I_{IOVCC}		-	-	30	μA	
	I_{IOVDD}		-	-	0	μA	
	I_{IOVSS}		-	-	0	μA	

Note 1: Typ.



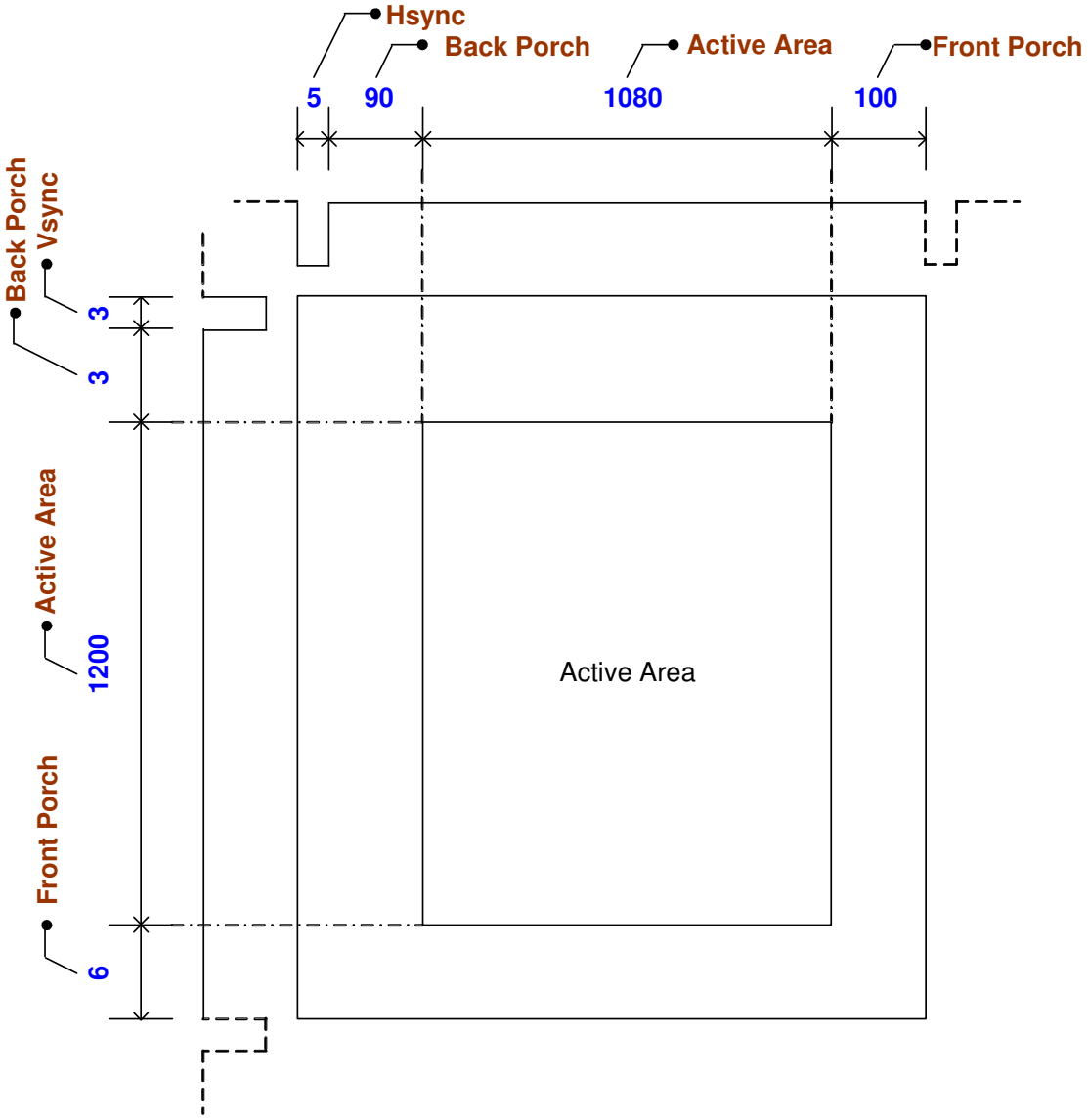
Max.



Note 2: 100 nits White.

5.4 AC Characteristics

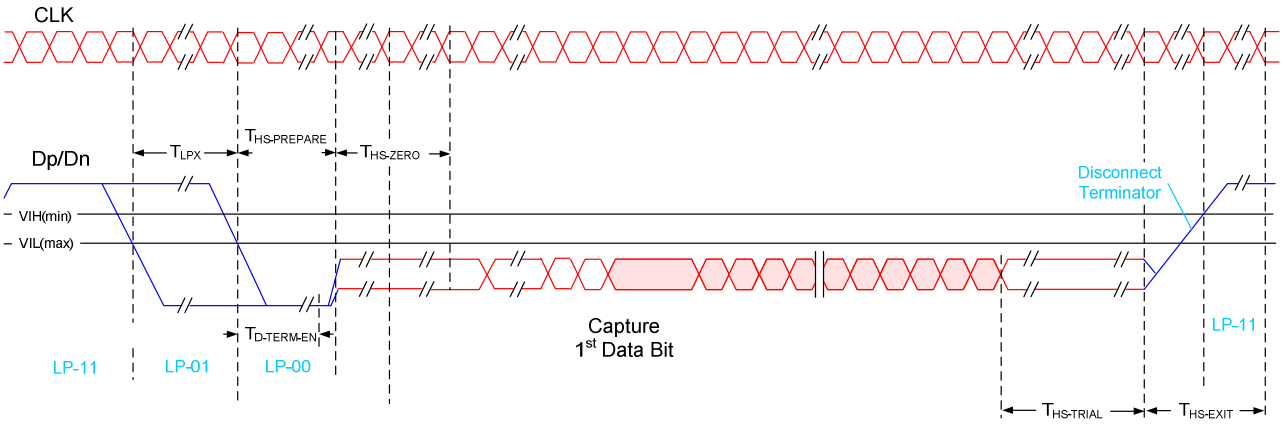
5.4.1 Display Video Timing



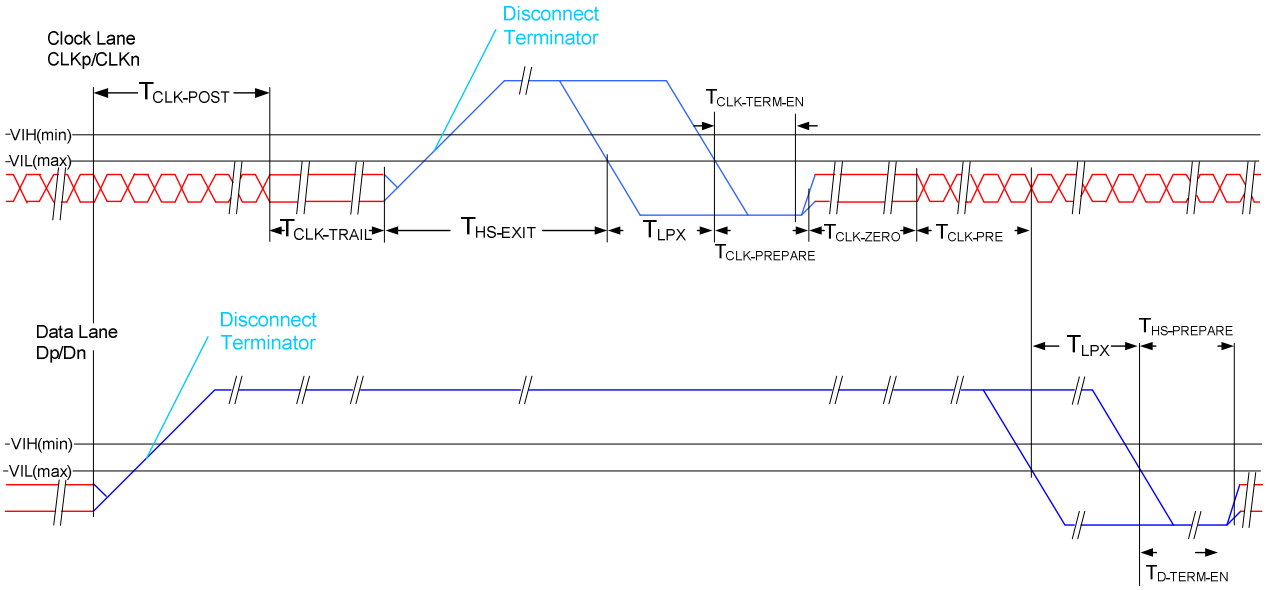
Name	Quantity	Unit
Frame Rate	90	Hz
Line Time	9.17	µs
H Sync	5	Dot
H Back Porch	90	Dot
H Active	1080	Dot
H Front Porch	100	Dot
H Total	1275	Dot
V Sync	3	Line
V Back Porch	3	Line
V Active	1200	Line
V Front Porch	6	Line
V Total	1212	Line

5.4.2 MIPI Interface Characteristics

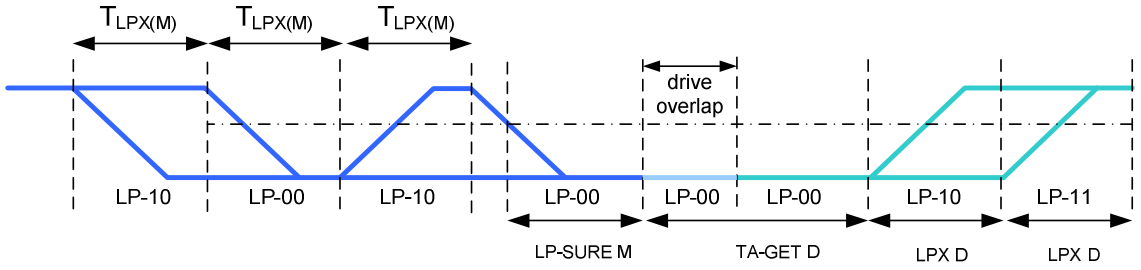
HS Data Transmission Burst



HS clock transmission



Turnaround Procedure

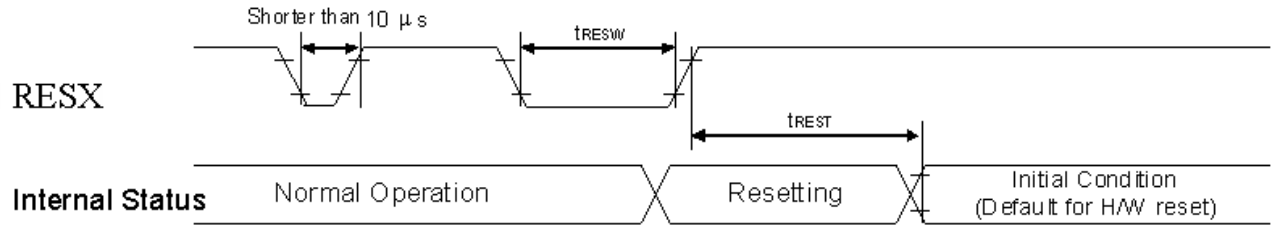


Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_{HS}-T_{RAIL} to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		2*$T_{LPX(M)}$	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*$T_{LPX(D)}$		ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*$T_{LPX(D)}$		ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		2*$T_{LPX(D)}$	ns

5.4.3 Display RESET Timing Characteristics

Reset input timing



IOVDD=1.65 to 1.95V, VDD=2.8 to 3.2V, GND=0V, Ta=-20 to 70°C

Timing Parameters

Symbol	Parameter	Related Pins	Min	Typ	Max	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

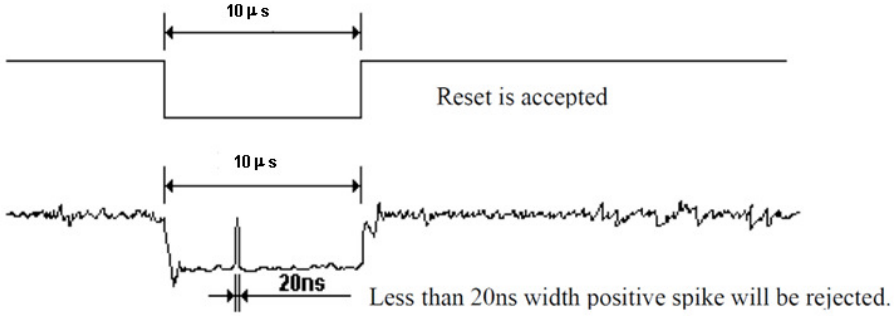
Note 1: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Invalid Reset
Longer than 10µs	Valid Reset
Between 5µs and 10µs	Reset Initialization Precedure

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In – mode) and then return to Default condition for H/W reset.

Note 3: During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

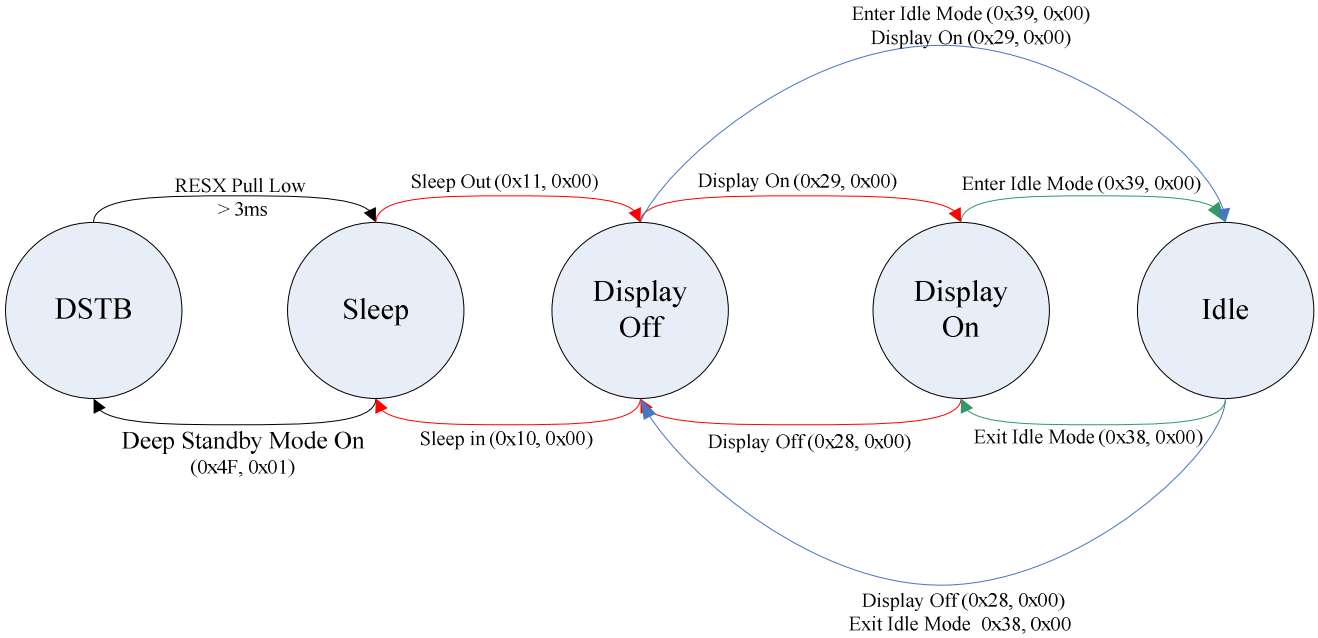
Note 4:Spike Rejection also applies during a valid reset pulse as shown below:



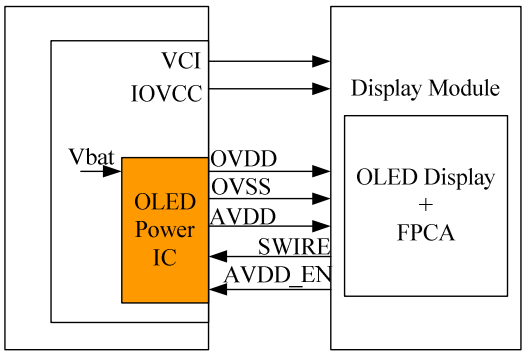
Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6 Recommended Operating Sequence

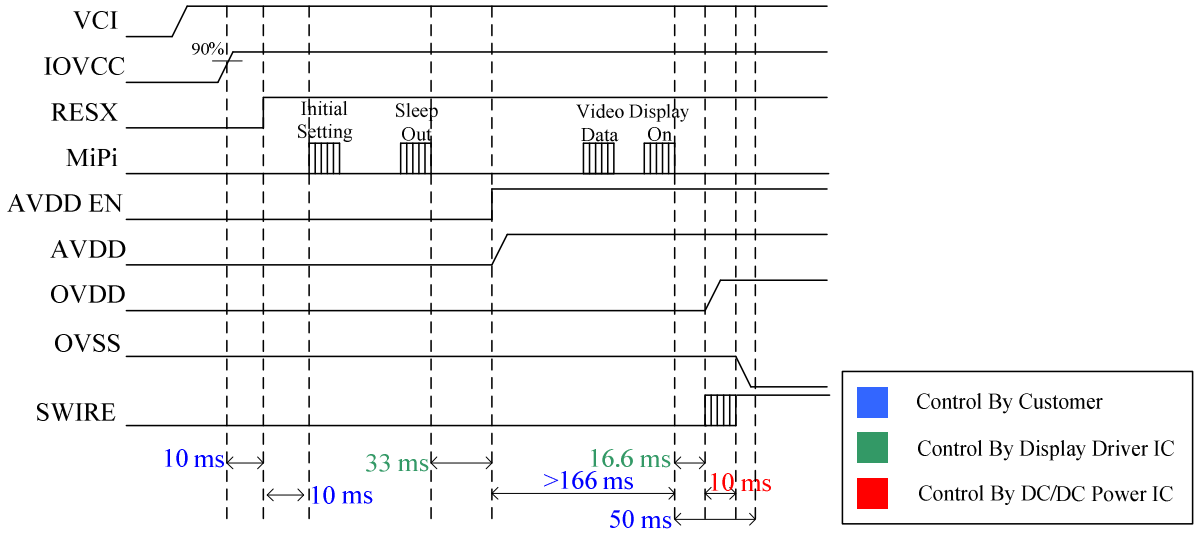
State Diagram



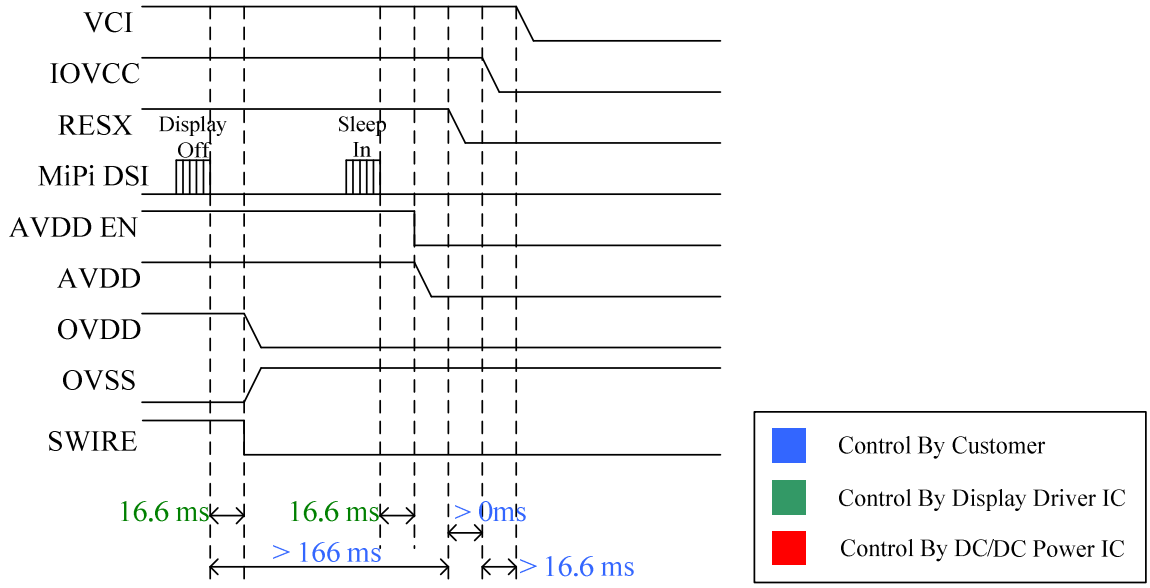
Power Structure



Power on sequence



Power off sequence



Please follow AUO's main FPC design suggestion.

Timing settings of Green are controlled by display driver IC. (The settings couldn't be adjusted.)

Timing settings of Red are controlled by DC/DC power IC. (The settings couldn't be adjusted.)

Initial Setting:

Item	Parameter Quantity	Address	P0
1	1	0xFE	0x08
2	1	0x07	0x1A
3	1	0xFE	0x00
4	1	0xC2	0x03
5	1	0x51	0x EF

Sleep Out:

Item	Parameter Quantity	Address	P0
1	1	0x11	0x00

Display On:

Item	Parameter Quantity	Address	P0
1	1	0x29	0x00

Sleep In

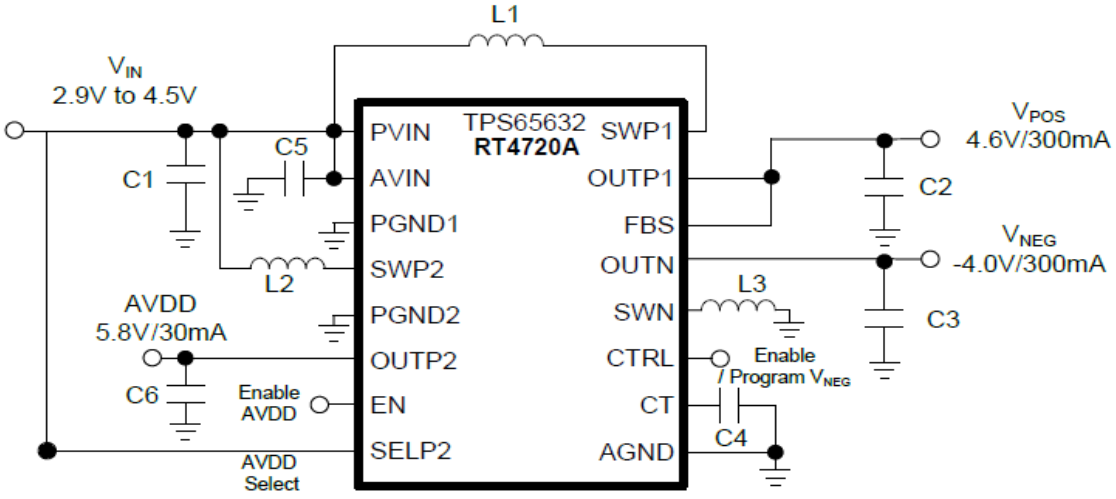
Item	Parameter Quantity	Address	P0
1	1	0x10	0x00

Display Off:

Item	Parameter Quantity	Address	P0
1	1	0x28	0x00

7 Application Circuit Reference

7.1 Recommend DC/DC Power IC Application Circuit



Note:

EN = AVDD_EN

CTRL = SWIRE

Power IC

Vendor	Model
TI	TPS65632RTER
Richtek	RT4720A

AUO don't suggest use other power IC instead of TPS65632RTER/ RT4720A , since they don't be qualified by AUO.

Bill of Materials

	Value	Part Number	Manufactuer
C1	3 x 10µF	GRM21BR71A106KE51	Murata
C2,C6	10µF	GRM21BR71A106KE51	Murata
C3	2 x 10µF	GRM21BR71A106KE51	Murata
C4,C5	100nF	GRM21BR71E104KA01	Murata
L1,L3	4.7µH	XEL4020-4R7ML	CoilCraft
L2	10µH	MMPP252012-100N	Coil Master

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 100hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 100hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 100hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 100hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 100hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-30°C/80°C 30cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"