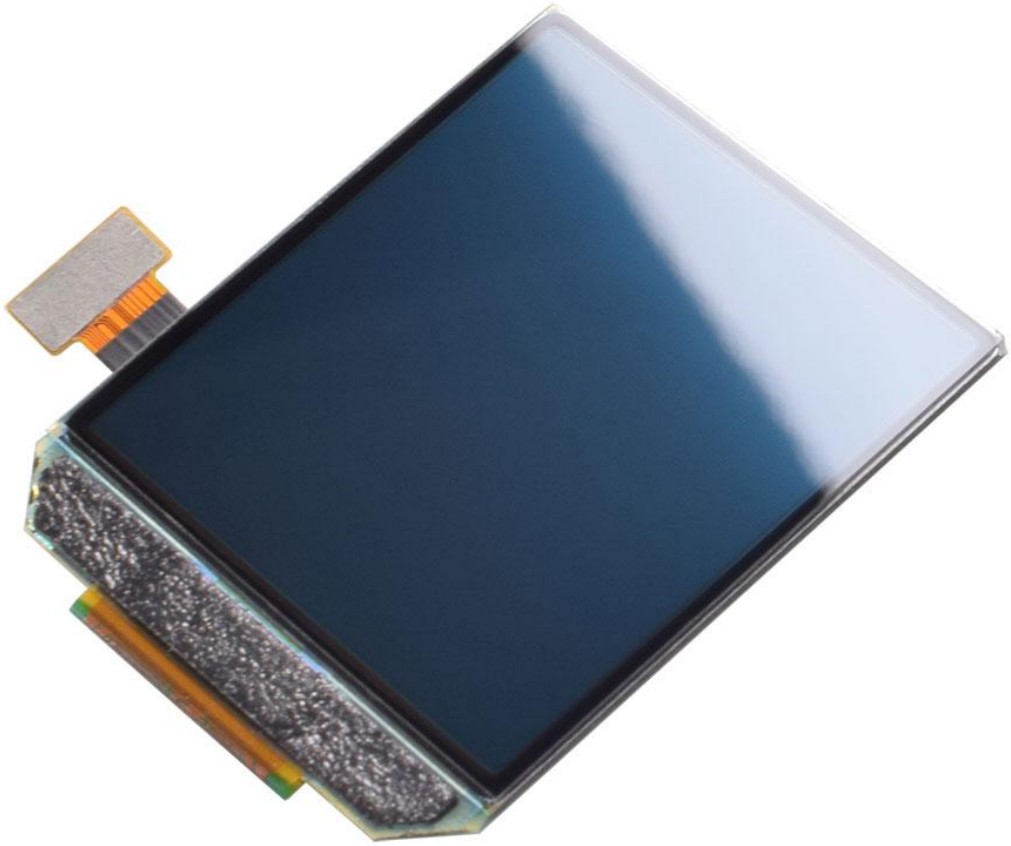
DisplayModule



DM-OLEDC145-649

1.45" 280 × 280 AMOLED FULL COLOR DISPLAY PANEL-MIPI

Contents

1 Revision History

Date	Changes
2019-06-25	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.45	inch
Display Mode	AMOLED	-
Display Colors	16.7M(Maximum)	Colors
Resolution	280 x RGB x 280	pixel
Controller IC	Raydium RM69080	-
Interface	MIPI	-
Active Area	26.04 x 26.04	mm
Panel Dimension	28.64 x 32.6 x 0.7	mm
Pixel Pitch	93	μm
NTSC Ratio	~100	%
Weight	TBD	g

3 Pin Description

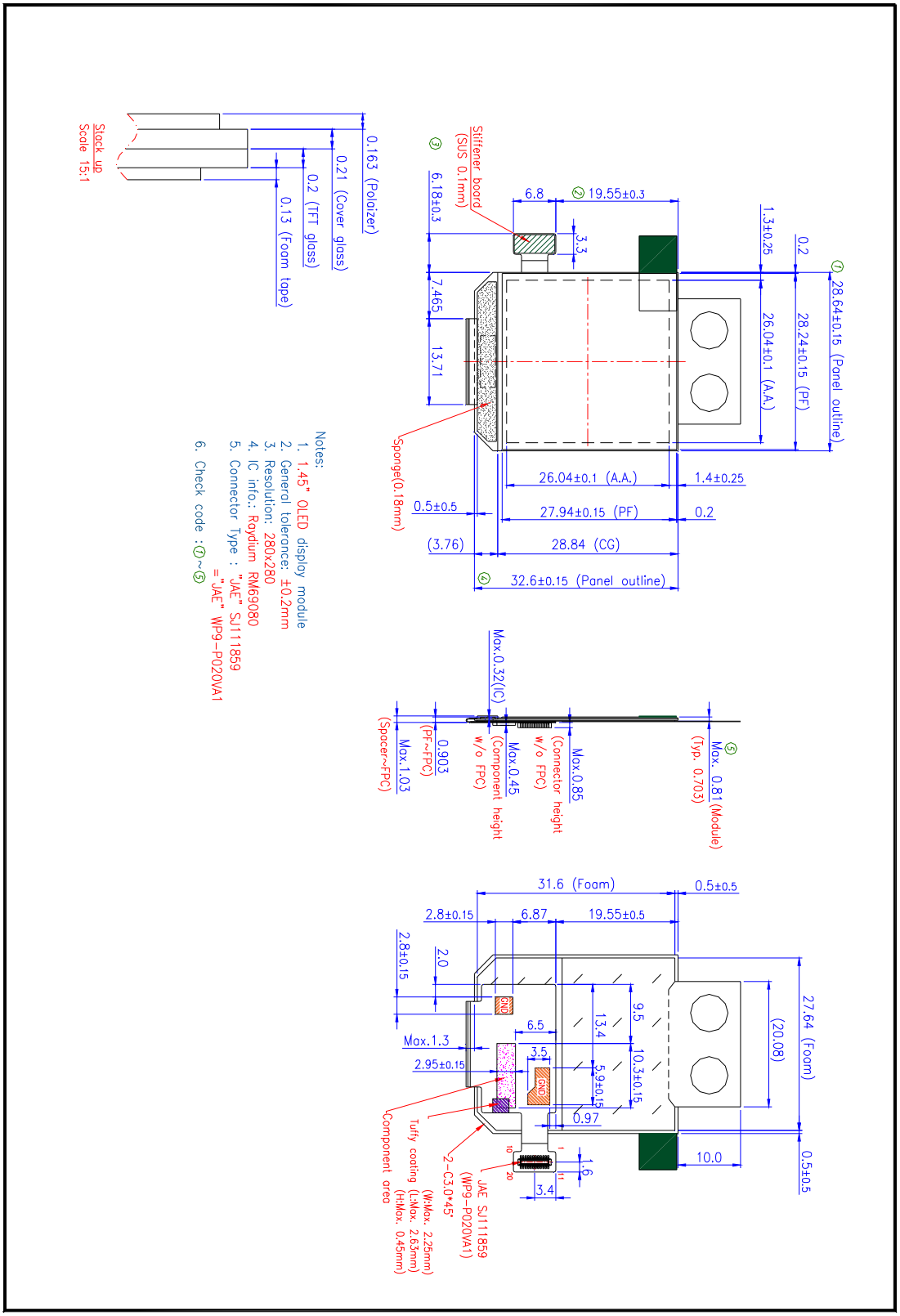
3.1 Panel Pin Description

Pin No.	Symbol	Function Description
1	ELVSS	OLED Power
2	ELVSS	OLED Power
3	ELVSS	OLED Power
4	GND	Ground
5	MIPI_CKP	MIPI DSI CLK
6	MIPI_CKN	MIPI DSI CLK
7	GND	Ground
8	MIPI_D0P	MIPI DSI data
9	MIPI_D0N	MIPI DSI data
10	GND	Ground
11	ELVDD	OLED Power
12	ELVDD	OLED Power
13	ELVDD	OLED Power
14	VDD	Analog power supply
15	IOVDD	IO power supply
16	GND	Ground
17	TE	TE output signal, if not use, please leave this pin open.
18	MTP_PWR	Panel programming power, leave this pin open.
19	RESX	
20	SWIRE	Power IC control signal,

Recommended connector: JAE WP9-P020VA1

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles TOP	ΘU	80	-	-	°	CR > 1600
View Angles Bottom	ΘD	80	-	-	°	
View Angles Right	ΘR	80	-	-	°	
View Angles Left	ΘL	80	-	-	°	
C.I.E. (White)	(x) (y)	0.273 0.287	0.303 0.317	0.333 0.347	-	C.I.E.1931 (Note)
C.I.E(Red)	(x) (y)	0.639 0.361	0.669 0.331	0.669 0.301	-	
C.I.E(Green)	(x) (y)	0.186 0.661	0.236 0.711	0.286 0.761	-	
C.I.E(Blue)	(x) (y)	0.090 0.025	0.130 0.065	0.170 0.105	-	
Pixel Luminance	L_{br}	270	300		cd/m²	
Contrast Ratio	CR	10000	-	-	-	

Note: Chromacity

Chromacity of **R, G, B** pattern are measured at Gray Level “255”.

Chromacity of **White** pattern are measured at Gray Level “255”.

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V_{DD}	-0.3	3.2	V
Digital Supply Voltage	IOVDD	-0.3	2.8	V
OLED Power supply	ELVDD	-	4.6	V
OLED Power supply	ELVSS	-	-2.4	V
Operating Temperature	T_{OPR}	-40	85	℃
Storage Temperature	T_{STG}	-55	125	℃

Note：If the module exceeds the absolute maximum ratings, it may be damaged permanently.Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

5.3 DC Characteristics

5.3.1 Display DC Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Remark
Analog Supply Voltage	V_{DD}	2.75	2.8	3	V	
Digital Supply Voltage	IOVDD	2.75	2.8	V_{DD}	V	
OLED Power supply	ELVDD	-	4.6	-	V	
OLED Power supply	ELVSS	-	-2.4	-	V	
High Level Input Voltage	V_{IH}	0.8 x IOVDD	-	IOVDD	V	RESX
Low Level Input Voltage	V_{IL}	0	-	0.1 x IOVDD	V	

Note : The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

5.3.2 Display Current Consumption

Item	Symbol	Condition	Min	Typ.	Max	Unit	Remark
Normal mode	I_{VDD}	V_{DD} = 2.8V IOVDD = 2.8V ELVDD = 4.6V ELVSS = -2.4V 25℃	-	4	5	mA	Note1
	I_{IOVDD}		-	1.2	1.5	mA	
	I_{ELVDD}		-	14	17.5	mA	
	IEL_{VSS}		-	14	17.5	mA	
Idle mode	I_{VDD}		-	2.5	2.8	mA	Note2
	I_{IOVDD}		-	1.1	1.3	mA	
	I_{ELVDD}		-	0	0	mA	
	IEL_{VSS}		-	0	0	mA	

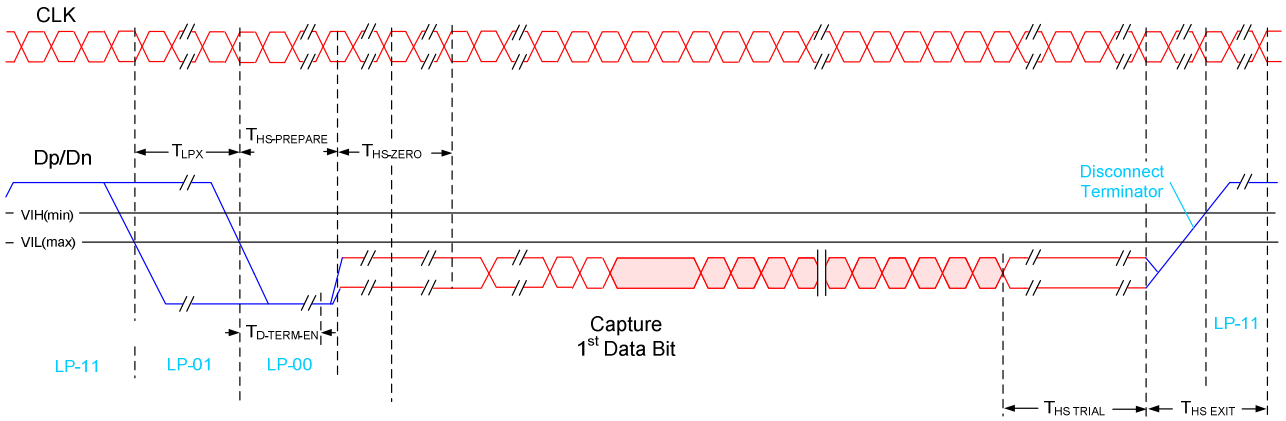
Note 1: Frame rate 60Hz. L255 & full white pattern

Note 2: Frame rate 30Hz, 10% Brightness & 10% Pixel ratio. ELVDD & ELVSS Using Internal Power.

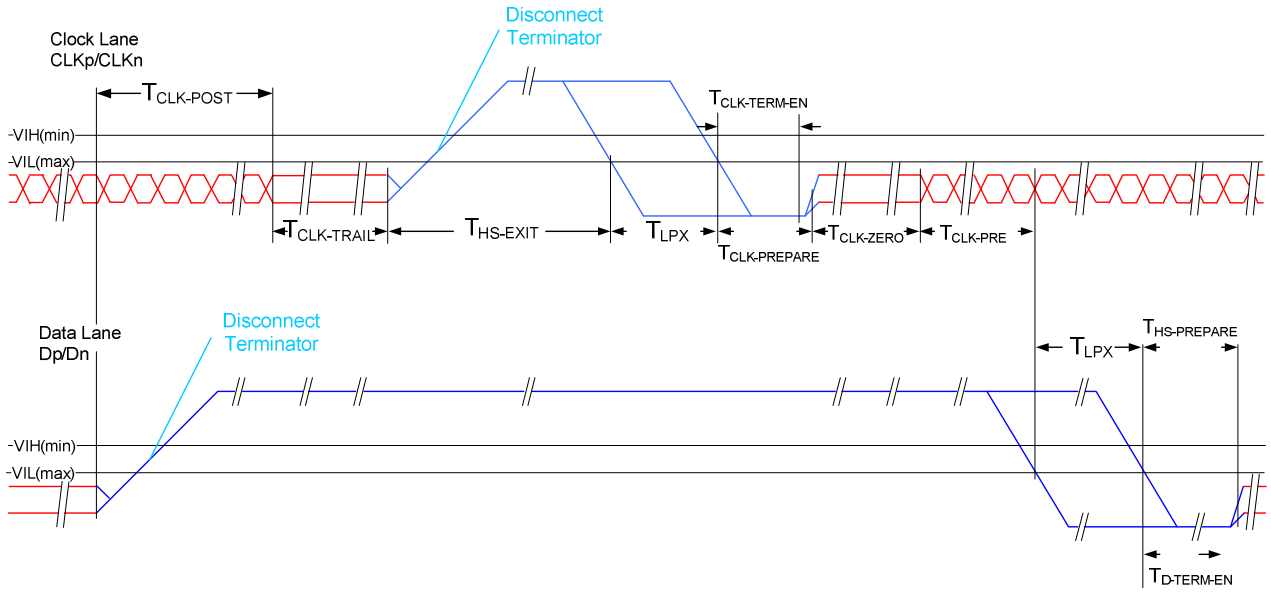
5.4 AC Characteristics

5.4.1 MIPI Interface Characteristics

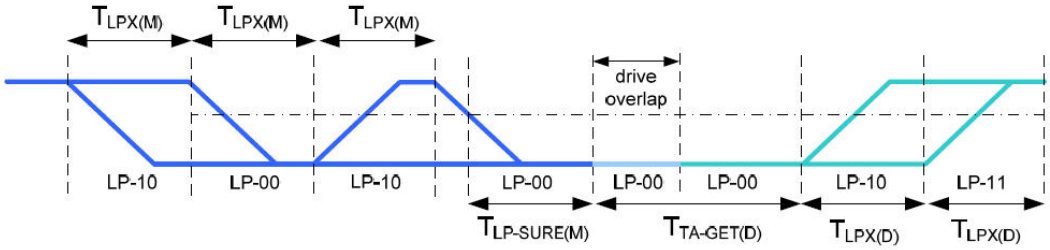
HS Data Transmission Burst



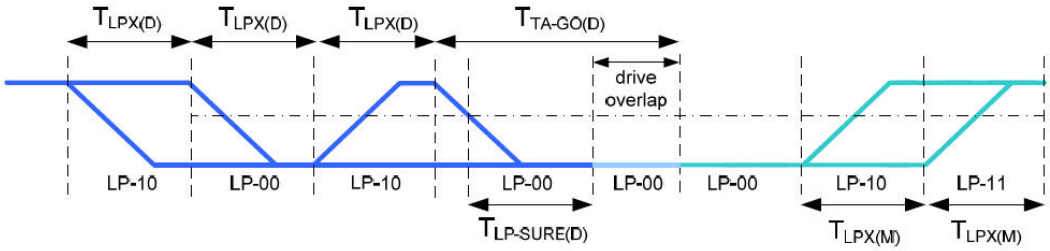
HS clock transmission



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing

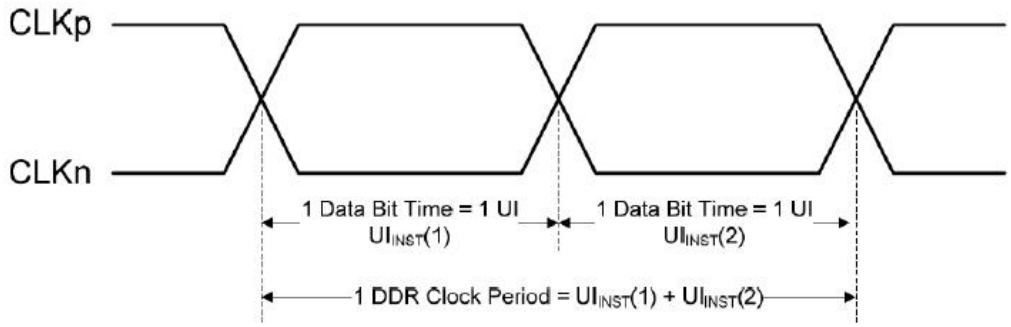


Bus turnaround (BAT) from display module to MPU timing

Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		2*$T_{LPX(M)}$	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*$T_{LPX(D)}$		ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*$T_{LPX(D)}$		ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		2*$T_{LPX(D)}$	ns

DDR Clock Definition

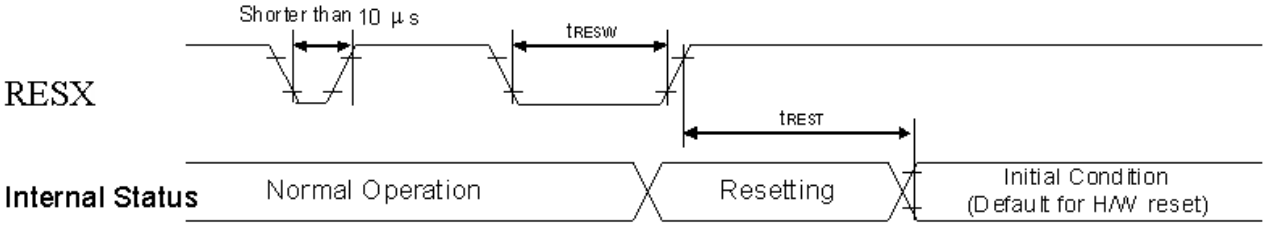


Clock Parameter	Symbol	Min	Typ	Max	Units
UI instataneous	UI_{inst}	7		12.5	ns

Note: Recommend maximum data rate is 150Mbps.

5.4.2 Display RESET Timing Characteristics

Reset input timing



IOVCC=1.65 to 1.95V, VCI=2.8 to 3.2V, GND=0V, Ta=-40 to 85℃

Timing Parameters

Symbol	Parameter	Related Pins	Min	Typ	Max	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

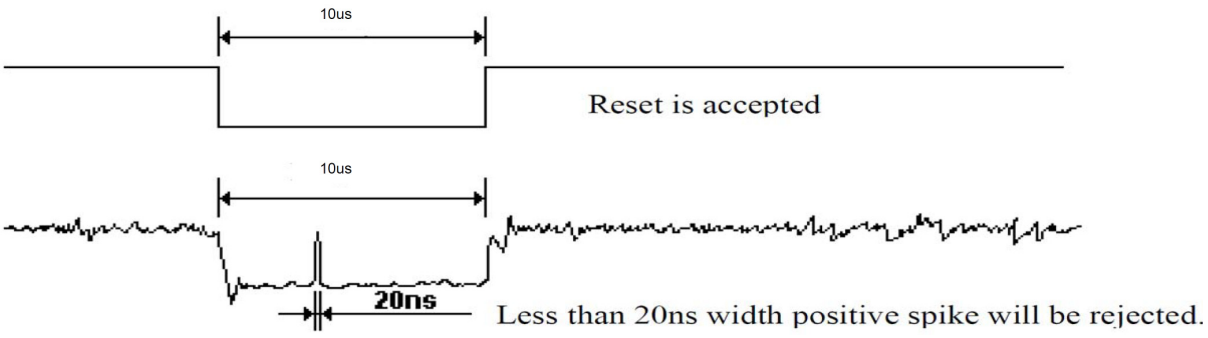
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Invalid Reset
Longer than 10µs	Valid Reset
Between 5µs and 10µs	Reset Initialigation Precedure

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out – mode. The display remains the blank state in Sleep In – mode) and then return to Default condition for H/W reset.

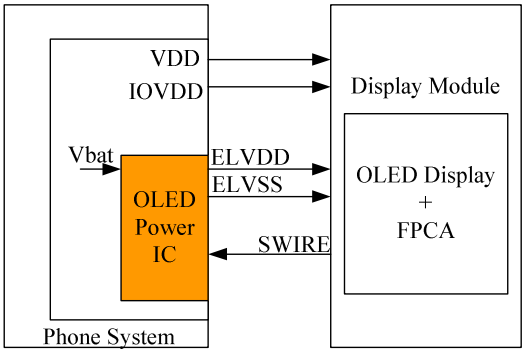
Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Power Structure



Initial Setting:

Item	Data Type	Address	P0
1	0x15	0xFE	0x 01
2	0x15	0x2A	0x 06
3	0x15	0x FE	0x 05
4	0x15	0x 05	0x 00
5	0x15	0x FE	0x 07
6	0x15	0x 07	0x 6D
7	0x15	0x FE	0x 0A
8	0x15	0x 1C	0x 1B
9	0x15	0x FE	0x 00
10	0x15	0x 35	0x 00
11	0x29	0x 2A	0x 00
12			0x 00
13			0x 01
14			0x 17
15	0x29	0x 2B	0x 00
16			0x 00
17			0x 01
18			0x 17
19	0x29	0x 31	0x 00
20			0x 00
21			0x 01
22			0x 17
23	0x05	0x 12	0x 00

Sleep Out:

Item	Parameter Quantity	Address	P0
1	1	0x11	0x00

Display On:

Item	Parameter Quantity	Address	P0
1	1	0x29	0x00

Sleep In

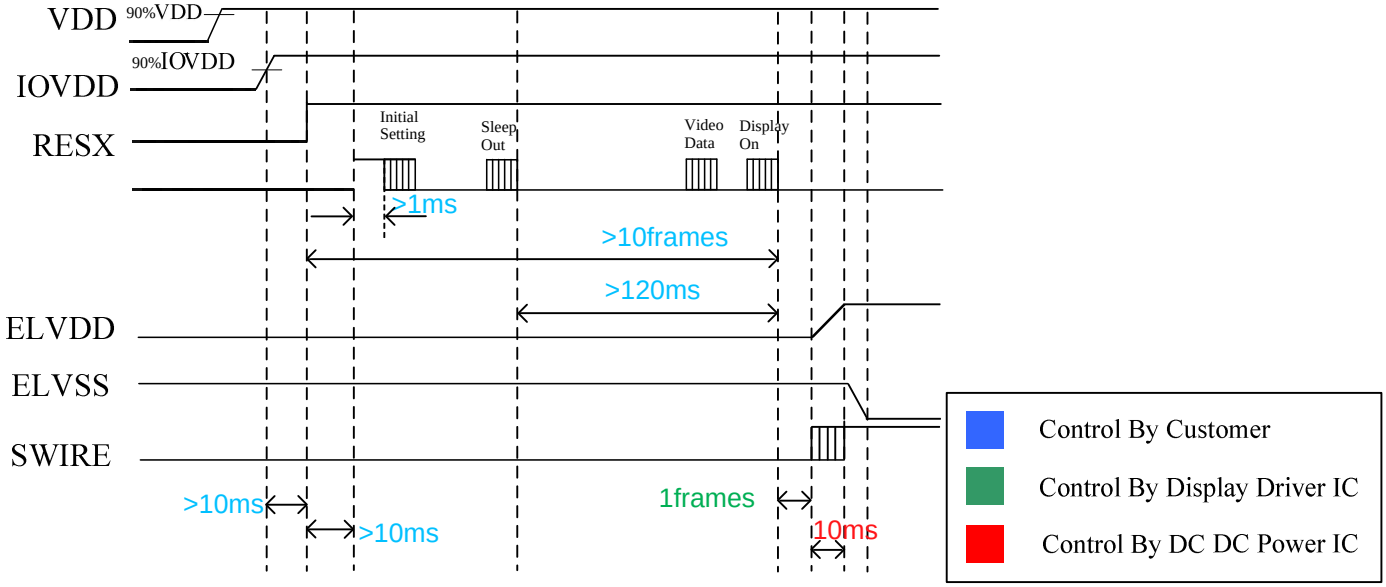
Item	Parameter Quantity	Address	P0
1	1	0x10	0x00

Display Off:

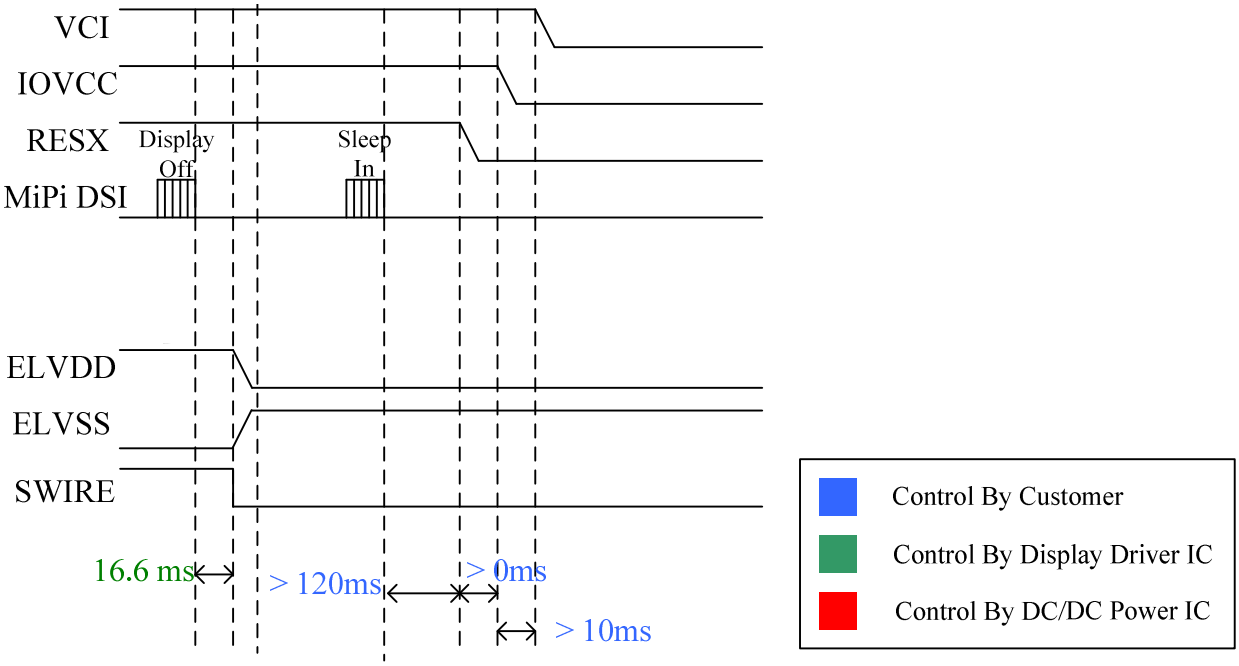
Item	Parameter Quantity	Address	P0
1	1	0x28	0x00

6 Power ON/OFF Timing Sequence

Power on sequence

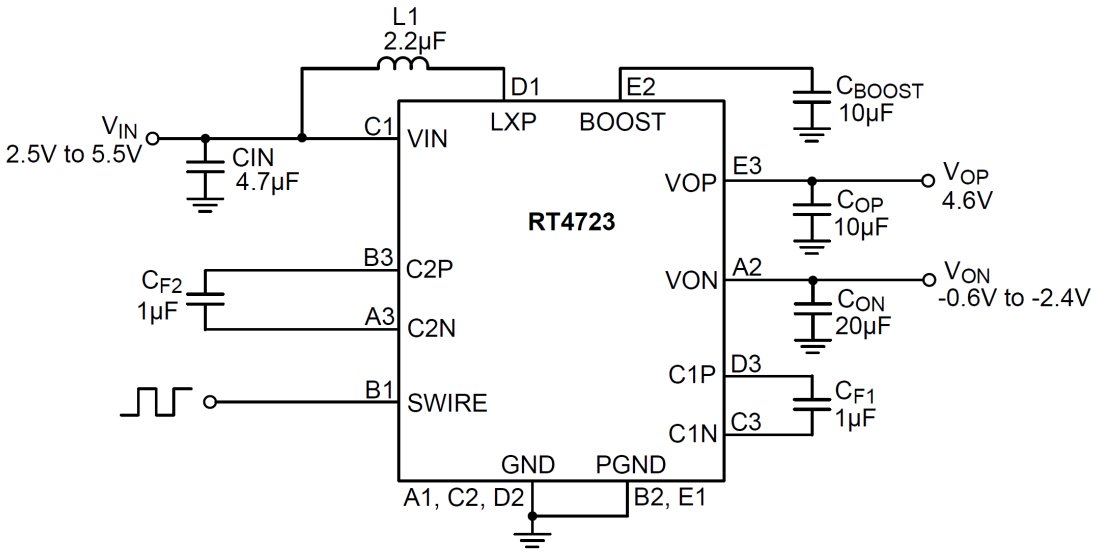


Power off sequence



7 Application Circuit Reference

7.1 Recommend DC/DC Power IC Application Circuit



8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	70℃ 168hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 168hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	60℃ 168hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 ℃ 168hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	40℃,90%RH 168hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-30℃/70℃ 30cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"