![DisplayModule logo]

DM-OLEDC141-648

1.41" 320 x 360 AMOLED FULL COLOR DISPLAY PANEL WITH IN-CELL TOUCH-MIPI

Contents

1 Revision History

Date	Changes
2019-06-20	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.41	inch
Display Mode	AMOLED	-
Display Colors	16.7M(Maximum)	Colors
Resolution	320 x RBG x 360	pixel
Controller IC	WT010	-
Interface	MIPI	-
Active Area	23.84 x 26.82	mm
Module Dimension	26.04 x 31.00 x 0.66	mm
Frame rate (normal mode)	60	Hz
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

| Pin No.	Symbol	Function Description
1	NC	Floating
2	TP_INT	TP initial signal
3	NC	Floating
4	GND	Ground
5	VCI	Driver analog power supply
6		(Power IC need to follow AUO's suggestion)
7	GND	Ground
8	SWIRE	SWIRE signal for PWR IC control (Power IC need to follow AUO's suggestion)
9	TE	Vsync (vertical sync) signal output from panel to avoid tearing effect
10	REST	Device reset signal (0 : enable ; 1 : Disable)
11	GND	Ground
12	VDDIO	Power supply for interface system except MIPI interface
13	MTP	Power supply for OTP
14	ELVDD	AMOLED positive power supply
15		(Power IC need to follow AUO's suggestion)
16	ELVSS	AMOLED negative power supply
17		(Power IC need to follow AUO's suggestion)
18	GND	Ground
19	IDF	Panel ID pin
20	GND	Ground
21	DSI_D0N	MIPI negative data signal
22	DSI_D0P	MIPI positive data signal
23	GND	Ground
24	DSI_CLKN	MIPI negative clock signal
25	DSI_CLKP	MIPI positive clock signal
26	GND	Ground
27	NC	Floating
28	TP_SDA	TP Data signal
29	TP_SCL	TP Clock signal
30	TP_RST	TP Reset signal

Note 1 : I = input ; O = output ; P = Power ; I/O = input / Output; NC= No Connection.

Note 2 : AUO suggest only use MIPI I/F, and pin of SPI I/F is connected as below.

(SCL & DCX & SDI & SDO pin is GND, and CSX is connected to VDDIO.)

4 Mechanical Drawing

4.1 Panel Mechanical Drawing
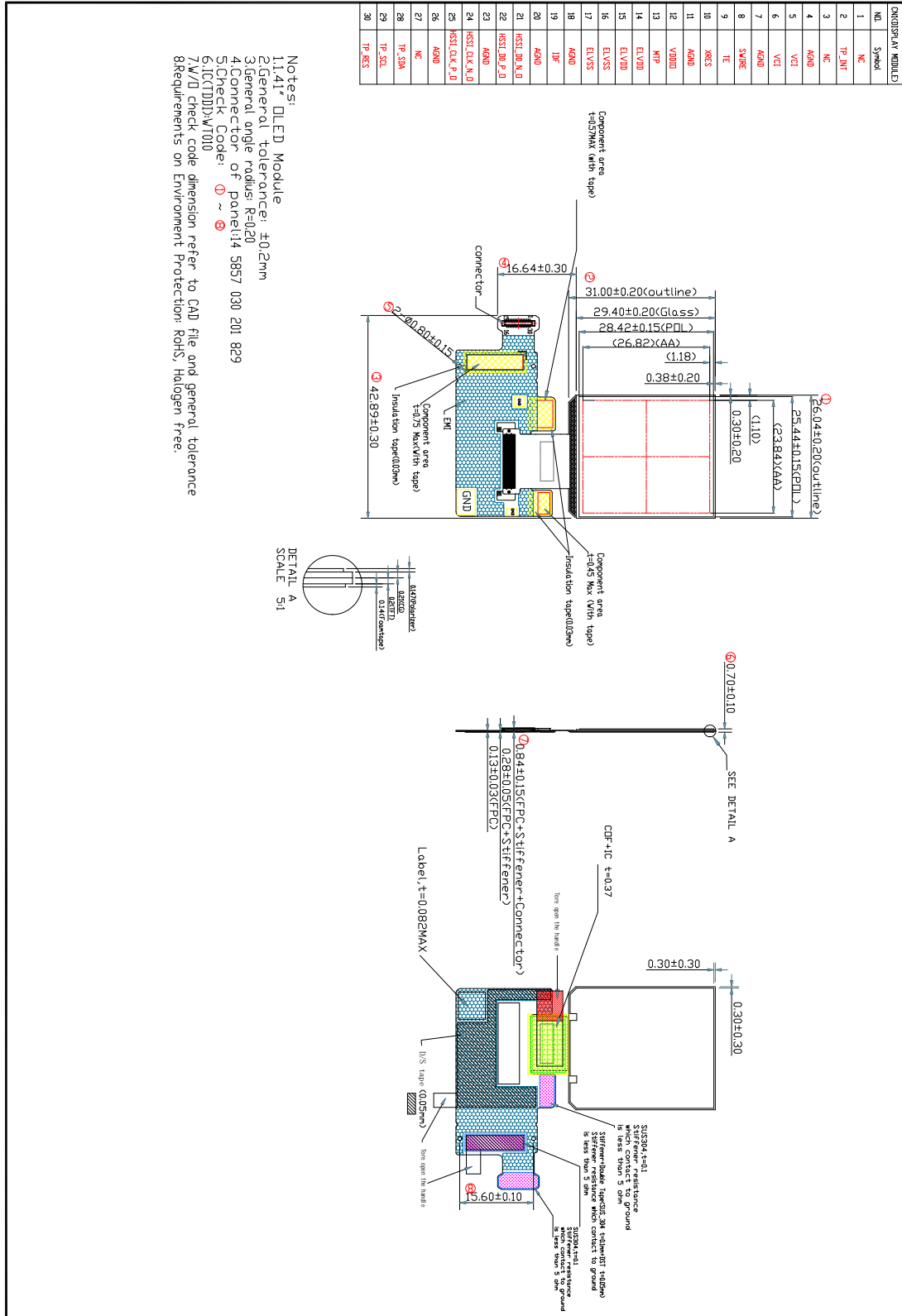
5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles TOP	Θ U	80	-	-	°	-
View Angles Bottom	Θ D	80	-	-	°	-
View Angles Right	Θ R	80	-	-	°	-
View Angles Left	Θ L	80	-	-	°	-
C.I.E. (White)	(x) (y)	0.28 0.29	0.30 0.31	0.32 0.33	-	C.I.E.1931
C.I.E(Red)	(x) (y)	0.64 0.30	0.67 0.33	0.70 0.36	-	C.I.E.1931
C.I.E(Green)	(x) (y)	0.186 0.661	0.236 0.711	0.286 0.761	-	C.I.E.1931
C.I.E(Blue)	(x) (y)	0.090 0.025	0.130 0.065	0.170 0.105	-	C.I.E.1931
Pixel Luminance	L_{br}	315	350	385	cd/m²	Note 1
Contrast Ratio	CR	10000	-	-	-	Note 2

Note 1:The brightness measurement shall be done at the center of the display with a full white image.

Note 2: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at “White” state}}{\text{Photo detector output when OLED is at “Black}}$$

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V_{CI}	-0.3	5.5	V
Digital Supply Voltage	V_{DDIO}	-0.3	5.5	V
ELVDD Supply Voltage	ELVDD	-	5.0	V
ELVSS Supply Voltage	ELVSS	-5.0	-	V

Note: If the module exceeds the absolute maximum ratings, it may be damaged permanently.

5.3 DC Characteristics

5.3.1 Display DC Characteristics

Item	Symbol	Min	Typ.	Max	Unit
Battery Supply Voltage	V_{CI}	2.75	2.8	3.0	V
Digital Supply Voltage	V_{DDIO}	1.65	1.8	1.95	V
ELVDD Supply Voltage	ELVDD	4.55	4.6	4.65	V
ELVSS Supply Voltage	ELVSS	-2.35	-2.40	-2.45	V
Low Level Input Voltage	V_{IL}	0	-	0.2 x V_{DDIO}	V
High Level Input Voltage	V_{IH}	0.8 x V_{DDIO}	-	V_{DDIO}	V
Low Level Output Voltage	V_{OL}	0	-	0.2 x V_{DDIO}	V
High Level Output Voltage	V_{OH}	0.8 x V_{DDIO}	-	V_{DDIO}	V

Note : The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

5.3.2 Display & TP Current Consumption

Item	Symbol	Condition	Min	Typ.	Max	Unit	Remark
Panel Power	P_{OLED}	ELVDD:4.6V	-	-	119	mW	Note1
	I_{OLED}	ELVSS:-2.4V	-	-	17	mA	Note1
Normal IC (with TP)	P_{VCI}	V_{CI} : 2.8V	-	13.6	15.7	mW	Note2
	I_{VCI}		-	4.9	5.6	mA	Note2
	P_{VDDIO}	V_{DDIO} :1.8V	-	4.0	4.6	mW	Note2
	I_{VDDIO}		-	2.2	2.6	mA	Note2
Sleep IC (with TP)	P_{VCI}	V_{CI} : 2.8V	-	-	0.76	mW	Note3
	I_{VCI}		-	-	0.27	mA	Note3
	P_{VDDIO}	V_{DDIO} :1.8V	-	-	0.98	mW	Note3
	I_{VDDIO}		-	-	0.54	mA	Note3

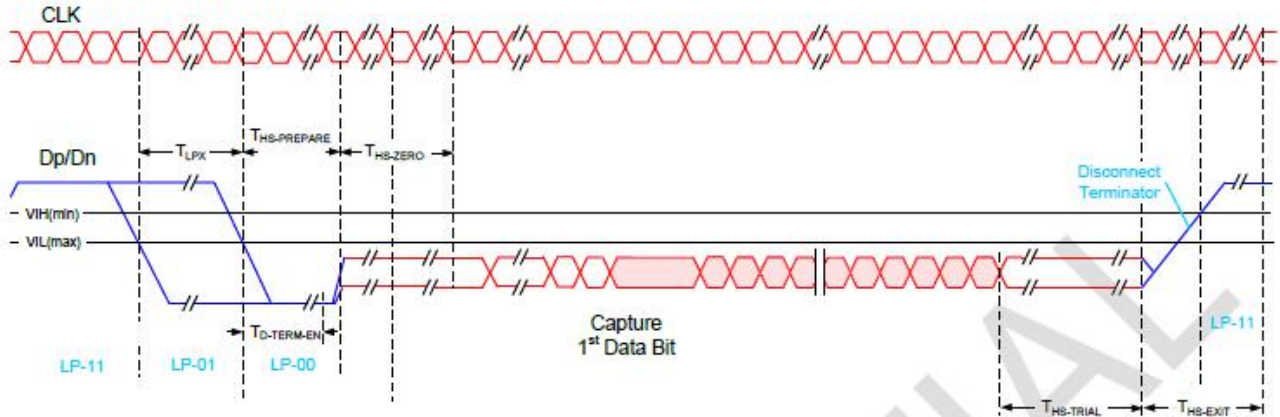Note 1: Based on L255 (350nits) full white pattern.

Note 2: Based on black pattern. MIPI-DSI frame rate 60Hz command mode.

Note 3: Power consumption spec. is base on TP FW of the engineer version. The power consumption may be revised according to the TP FW version.
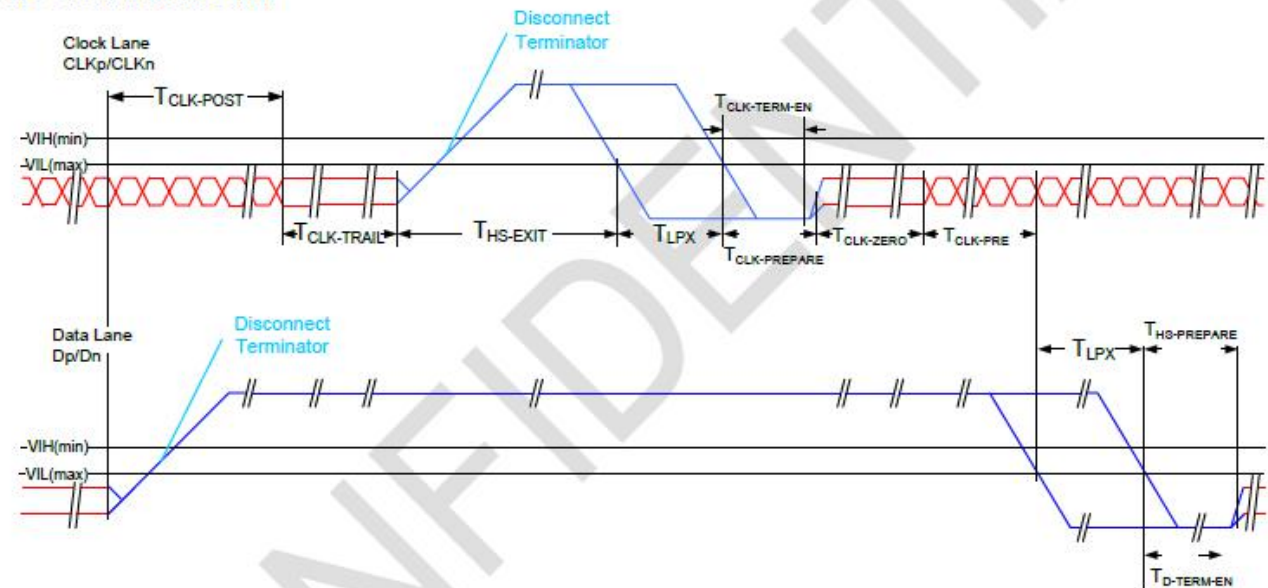
5.4 AC Characteristics
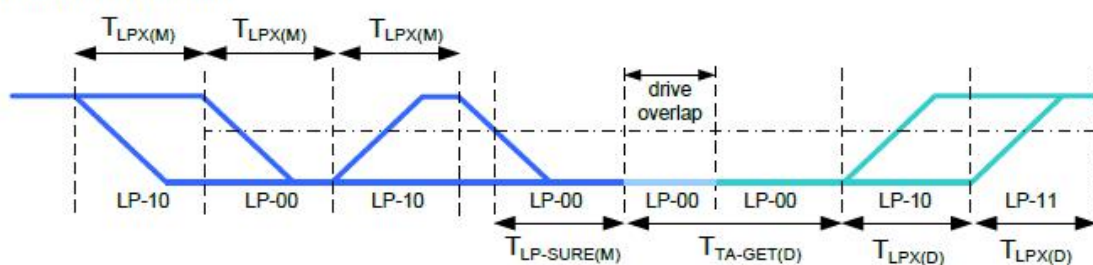
5.4.1 MIPI Interface Characteristics
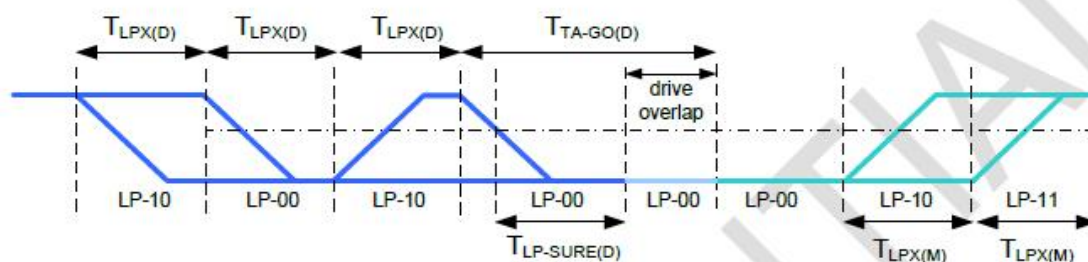
HS Data Transmission Burst

HS clock transmission

Turnaround Procedure


Bus turnaround (BAT) from MPU to display module timing

Bus turnaround (BAT) from display module to MPU timing

Timing Parameters

Symbol	Description	Min	Typ.	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL\ MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL\ MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

| $T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns

DDR Clock Definition
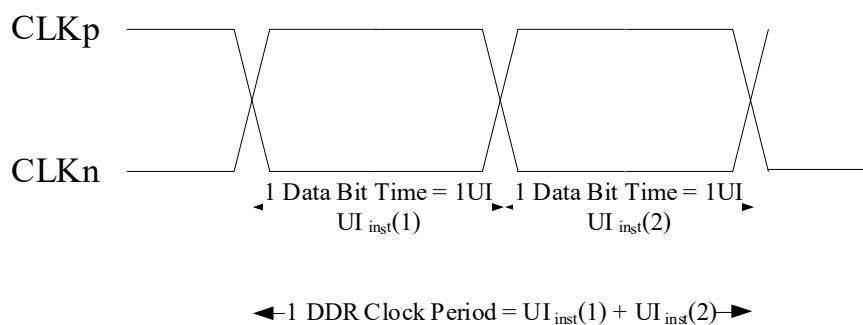
Clock Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UIinst	2		12.5	ns

5.4.2 Display RESET Timing Characteristics
Reset input timing
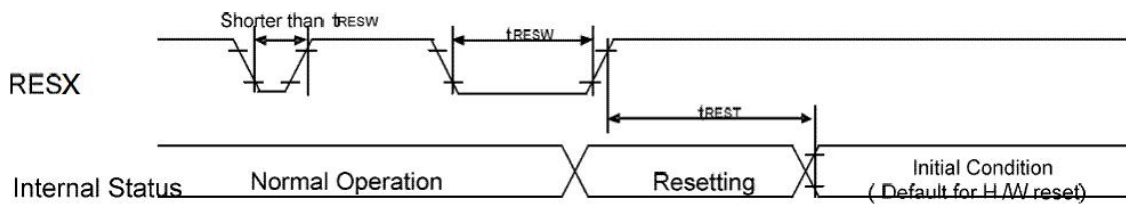
Symbol	Parameter	Related Pins	Min	Typ	Max	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Invalid Reset
Longer than 10μs	Valid Reset
Between 5μs and 10μs	Reset Initialigation Precedure

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out – mode. The display remains the blank state in Sleep In – mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

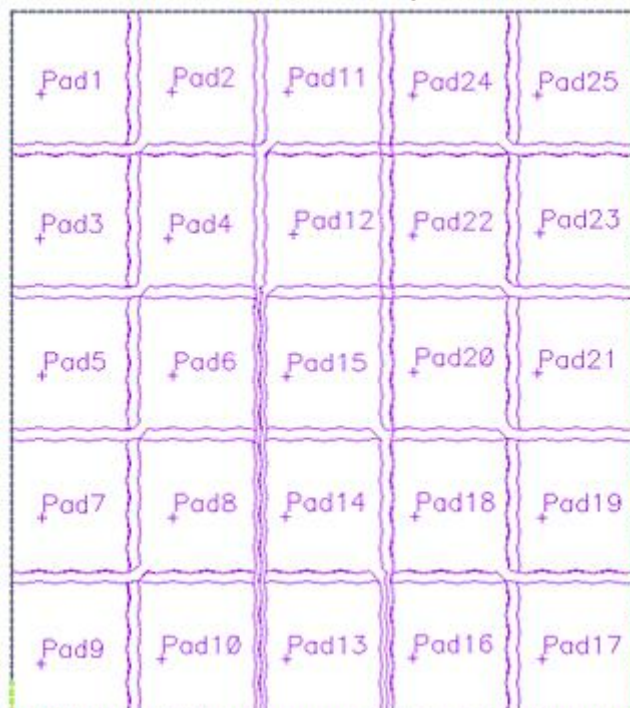Note 4. Spike Rejection also applies during a valid reset pulse as shown below:
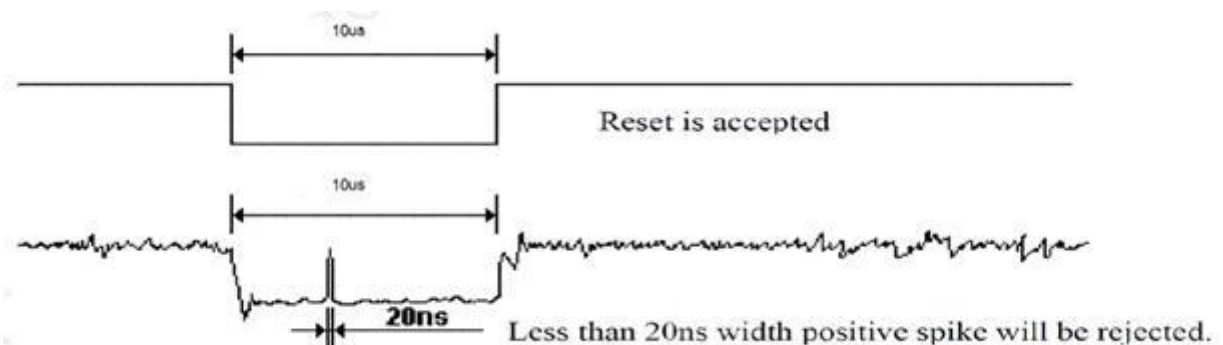
Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.4.3 Display Scan Direction & Coordinate
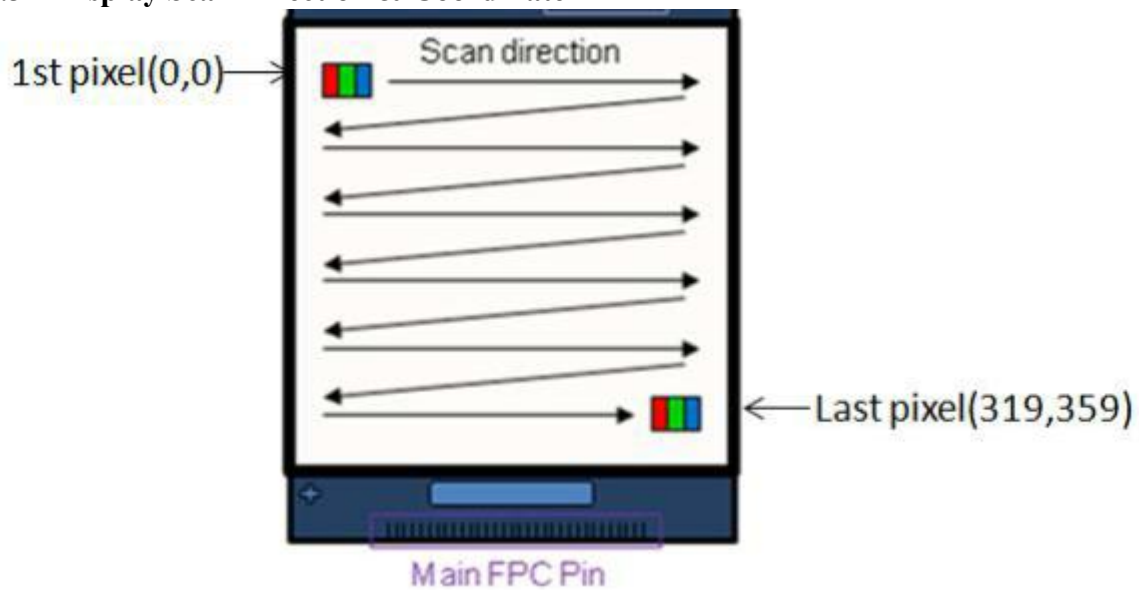
6 Touch Performance

6.1 Touch Sensor Drawing

6.2 Touch pattern design

| Item	TP sensor
Number of touch panel sensors	25

6.3 Touch Specifications

TP performance

No.	Item		Spec.
1	Multi-Finger		2
2	Report Rate		$\geqq$90Hz
3	Performance	Accuracy (at Ø 6 mm)	Non-border $\leqq$ 1.5mm, Border $\leqq$ 2mm
		Linearity (at Ø 6 mm)	Non-border $\leqq$ 1.5mm, Border $\leqq$ 2mm
		Jitter (at Ø 6 mm)	Non-border $\leqq$ 1.5mm, Border $\leqq$ 2mm

Design requirements of in-cell touch are as follows.

1．Cover lens design - Type: Glass, ε $\geqq$ 7.6, Thickness: $\leqq$ 1.2mm.

2．System gap $\geqq$ 0.6mm **(Base on cover lens thickness =0.8mm), When the cover lens is thinner, the system gap needs more.**
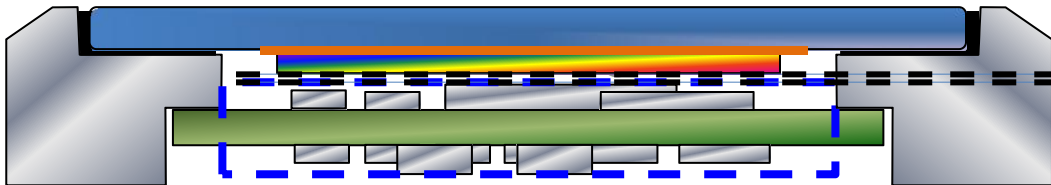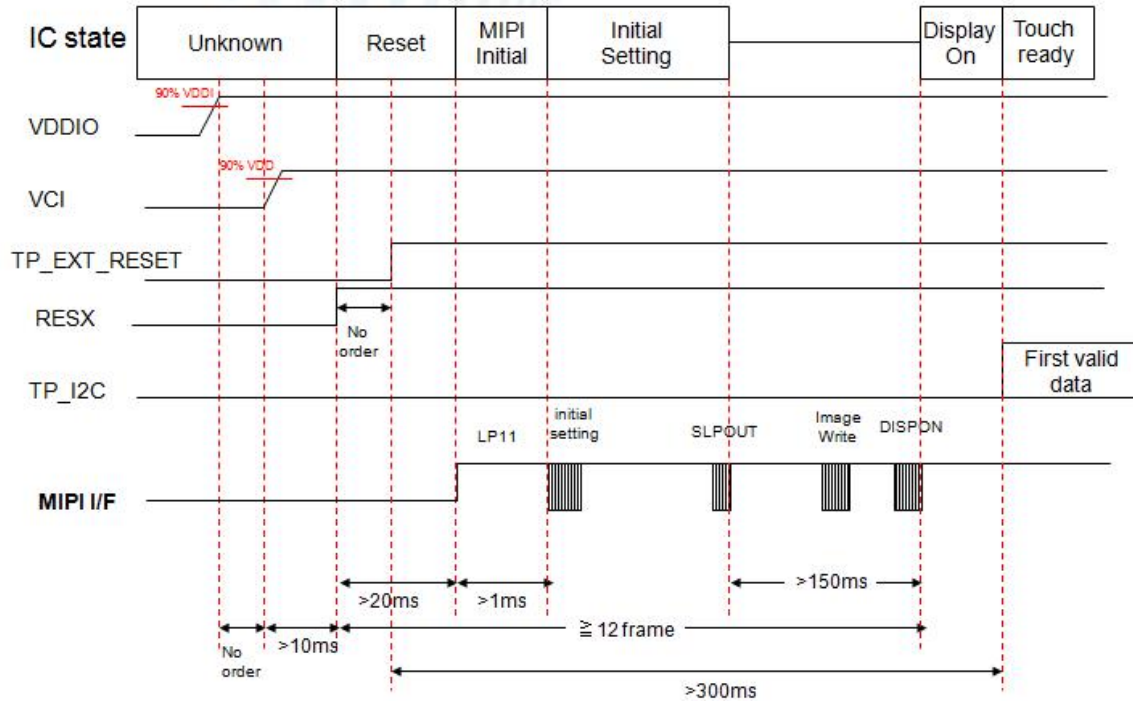

System gap:

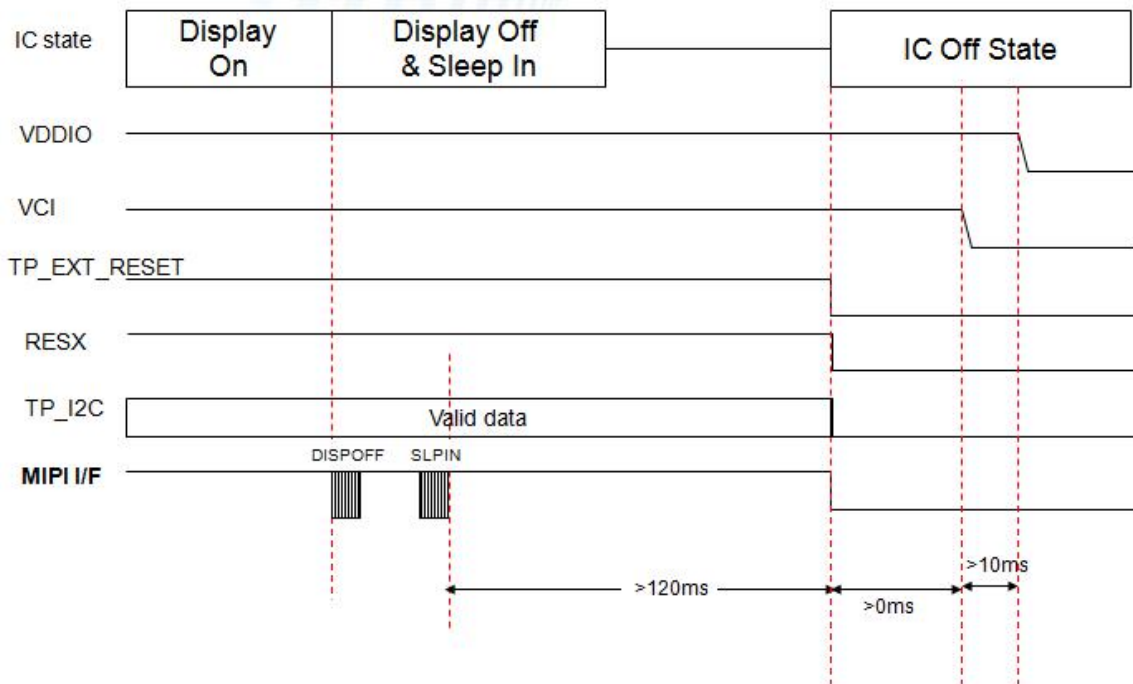1．the gap between bottom of AMOLED module and system parts/component.

2．The gap excludes system part thickness tolerance.
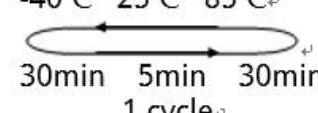
7 Power ON/OFF Timing Sequence

Power ON sequence:

Power OFF sequence:

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	70℃ 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	60℃ 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 ℃ 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 240hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation -40℃ 25℃ 85℃ 30min 5min 30min 1 cycle	-40℃/70℃ 100cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"