



DM-OLEDC139-654

**1.39" 400 × 400 AMOLED ROUND
FULL COLOR DISPLAY PANEL-MIPI**

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1 Revision History

Date	Changes
2019-07-15	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.39	inch
Display Mode	AMOLED	-
Display Colors	16.7M(Maximum)	Colors
Resolution	400 x 400	pixel
Controller IC	Raydium RM69080	-
Interface	MIPI	-
Active Area	35.4 x 35.4	mm
Panel Dimension	38.6 x 40.5 x 0.7	mm
Weight	TBD	g

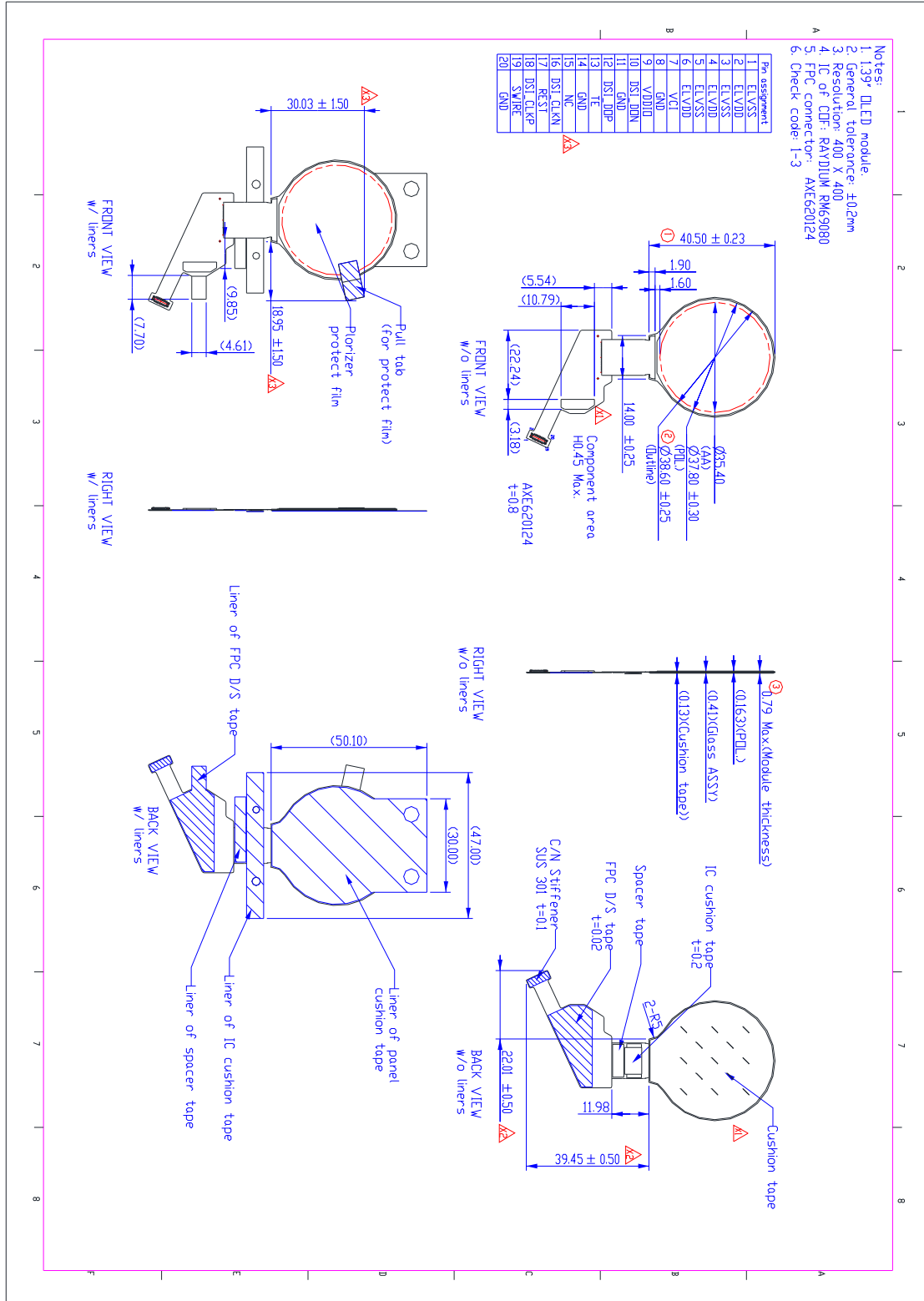
3 Pin Description

Pin No.	Symbol	Function Description
1	ELVSS	AMOLED negative power supply
2	ELVDD	AMOLED positive power supply
3	ELVSS	AMOLED negative power supply
4	ELVDD	AMOLED positive power supply
5	ELVSS	AMOLED negative power supply
6	ELVDD	AMOLED positive power supply
7	VCI	Driver analog power supply
8	GND	Ground
9	VDDIO	Power supply for Interface system except MIPI interface
10	DSI_D0N	MIPI negative data signal
11	GND	Ground
12	DSI_D0P	MIPI positive data signal
13	TE	Tearing effect output pin to synchronize MCU to frame writing.
14	GND	Ground
15	NC	No Connection
16	DSI_CLKN	MIPI negative clock signal
17	XRES	Device reset signal (0 : Enable ; 1: Disable)
18	DSI_CLKP	MIPI positive clock signal
19	SWIRE	SWIRE signal for PWR IC control
20	GND	Ground

Note: I = input ; O = output ; P = Power ; I/O = input / Output; NC= No Connection

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles TOP	⊕ U	80	-	-	°	CR > 1600
View Angles Bottom	⊕ D	80	-	-	°	
View Angles Right	⊕ R	80	-	-	°	
View Angles Left	⊕ L	80	-	-	°	
C.I.E(Red)	(x) (y)	0.645 0.295	0.675 0.325	0.705 0.355	-	C.I.E.1931;
C.I.E(Green)	(x) (y)	0.186 0.661	0.236 0.711	0.286 0.761	-	
C.I.E(Blue)	(x) (y)	0.090 0.025	0.130 0.065	0.170 0.105	-	
C.I.E(White)	(x) (y)	0.28 0.29	0.30 0.31	0.32 0.33	-	
Luminance Uniformity		85	-	-	%	300nits
Luminance		270	300	-	nits	-
Contrast Ratio	@ 25°	10000	-	-	-	Note 1
Gamma	γ	1.9	2.2	2.5	-	Note 2
Life time(LT95)		150	-	-	hrs	25°C; Note 3

- $\Delta Bp = Bp \text{ (Min.)} / Bp \text{ (Max.)} \times 100 \text{ (\%)}$
- Bp (Max.) = Maximum brightness in 5 measured spots
- Bp (Min.) = Minimum brightness in 5 measured spots.

Note 1: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at "White" state}}{\text{Photo detector output when OLED is at "Black"}}$$

Note 2 : Gamma spec. is based on Gray level 255, 250, 244, 240, 232, 224, 206, 192, 160, 128, 95, 63, 47 & 31.

Note 3: Time to 95% Luminance

To measure the burn-in effect, a test pattern with white background applied to the AMOLED display at 100% loading

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V _{CI}	-0.3	5.5	V
Digital Supply Voltage	VDDIO	-0.3	5.5	V
ELVDD Power Supply	ELVDD	-	5.0	V
ELVSS Power Supply	ELVSS	-5.0	-	V

Note: If the module exceeds the absolute maximum ratings, it may be damaged permanently.

5.3 DC Characteristics

5.3.1 Typical Operating Conditions

Item	Symbol	Min	Typ.	Max	Unit	Remark
Analog Supply Voltage	V _{CI}	2.75	2.8	3.0	V	Note1
Digital Supply Voltage	VDDIO	1.65	1.8	1.95	V	Note1
ELVDD Power Supply	ELVDD	4.55	4.60	4.65	V	Note1,2
ELVSS Power Supply	ELVSS	-2.35	-2.40	-2.45	V	Note1
Low Level Input Voltage	V _{IL}	0	-	0.2 x IOVDD	V	Note1
High Level Input Voltage	V _{IH}	0.8 x IOVDD	-	IOVDD	V	Note1
Low Level Output Voltage	V _{OL}	0	-	0.2 x IOVDD	V	Note1
High Level Output Voltage	V _{OH}	0.8 x IOVDD	-	IOVDD	V	Note1

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note 2: RT4723 Positive output voltage = 4.6V ± 0.8% at -40°C ≤ Ta ≤ +85°C

5.3.2 Display Current Consumption

Item	Symbol	Condition	Min	Typ.	Max	Unit	Remark
Panel Power	P _{NL}	ELVDD:4.6V	-	-	140.7	mW	Note 1,2
	I _{NL}	ELVSS:-2.4V	-	-	20.1	mA	Note 1,2
Normal IC	P _{VCI}	VCI : 2.8V	-	13.2	14.3	mW	Note 2
	I _{VCI}		-	4.7	5.1	mA	Note 2
	P _{VDDIO}	VDDIO :1.8V	-	4.0	5.6	mW	Note 2
	I _{VDDIO}		-	2.2	3.1	mA	Note 2
Idle IC	P _{VCI}	VCI : 2.8V	-	5.8	6.4	mW	Note 3
	I _{VCI}		-	2.1	2.3	mA	Note 3
	P _{VDDIO}	VDDIO :1.8V	-	2.0	2.2	mW	Note 3
	I _{VDDIO}		-	1.1	1.2	mA	Note 3

Note 1: Based on L255 (300nits) full white pattern

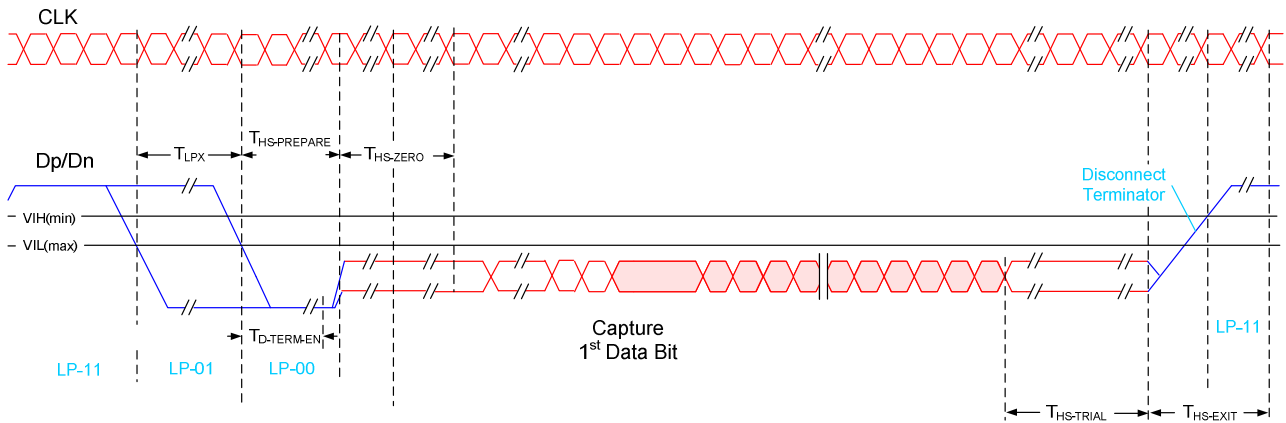
Note 2: Based on black pattern. MIPI-DSI frame rate 60Hz command mode.

Note 3: Based on black pattern. MIPI-DSI frame rate 15Hz command mode.

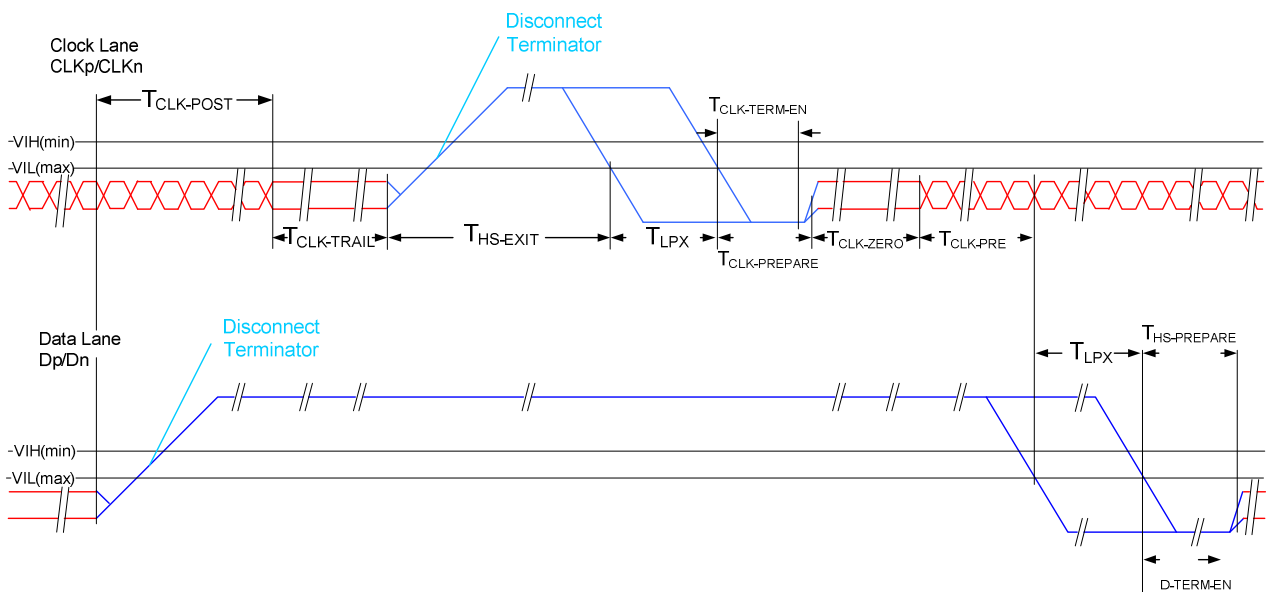
5.4 AC Characteristics

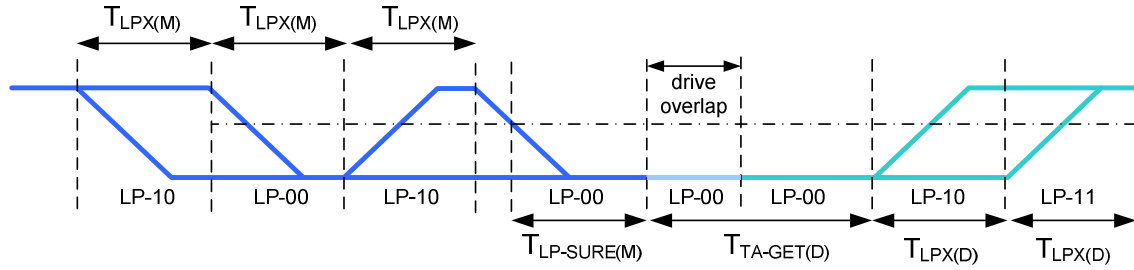
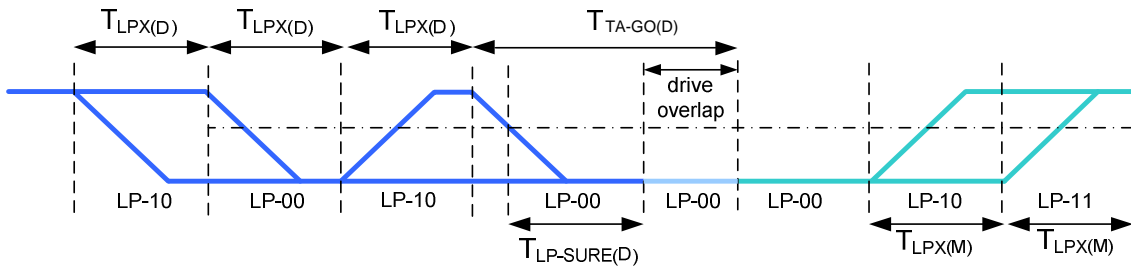
5.4.1 MIPI Interface Characteristics

HS Data Transmission Burst



HS clock transmission



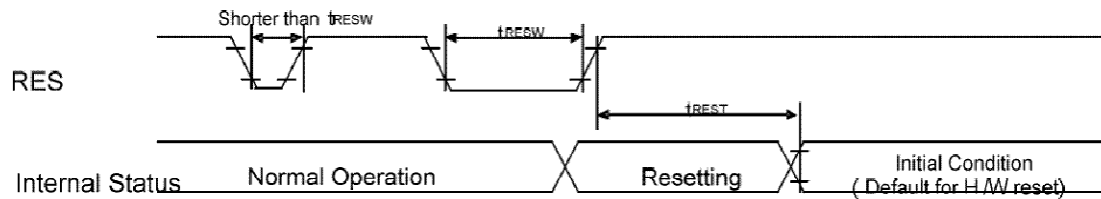
Turnaround Procedure

Bus turnaround (BAT) from MPU to display module timing


Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
T _{CLK-POST}	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T _{HS-TRAIL} to the beginning of T _{CLK-TRAIL} .	60ns + 52*UI			ns
T _{CLK-TRAIL}	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
T _{HS-EXIT}	Time that the transmitter drives LP-11 following a HS burst.	300			ns
T _{CLK-TERM-EN}	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V _{IL,MAX} .	Time for Dn to reach V _{TERM-EN}		38	ns
T _{CLK-PREPARE}	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
T _{CLK-PREPARE + T_{CLK-ZERO}}	T _{CLK-PREPARE} + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
T _{D-TERM-EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V _{IL,MAX} .	Time for Dn to Reach V _{TERM-EN}		35 ns + 4*UI	
T _{HS-PREPARE}	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
T _{HS-PREPARE + T_{HS-ZERO}}	T _{HS-PREPARE} + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
T _{HS-TRAIL}	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns
T _{LPX(M)}	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
T _{TA-SURE(M)}	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T _{LPX(M)}		2*T _{LPX(M)}	ns
T _{LPX(D)}	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
T _{TA-GET(D)}	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*T _{LPX(D)}		ns
T _{TA-GO(D)}	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*T _{LPX(D)}		ns
T _{TA-SURE(D)}	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T _{LPX(D)}		2*T _{LPX(D)}	ns

5.4.2 Display RESET Timing Characteristics

Reset input timing



Timing Parameters

Symbol	Parameter	Related Pins	Min	Typ	Max	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

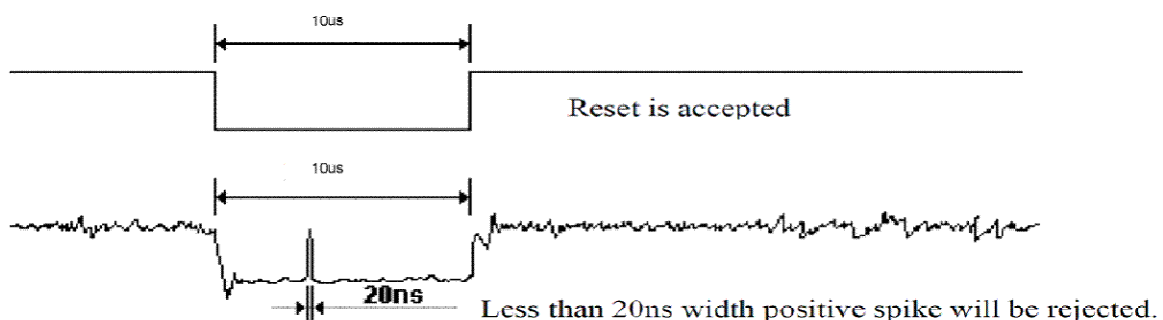
Note 1: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than $5\mu s$	Invalid Reset
Longer than $15\mu s$	Valid Reset
Between $5\mu s$ and $15\mu s$	Reset Initialization Procedure

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out - mode. The display remains the blank state in Sleep In - mode) and then return to Default condition for H/W reset.

Note 3: During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

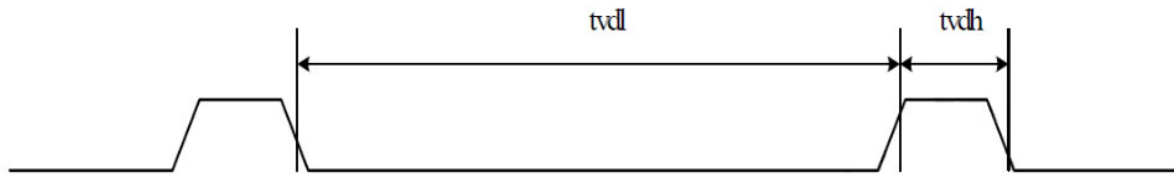
Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.4.3 TE Timing Characteristics

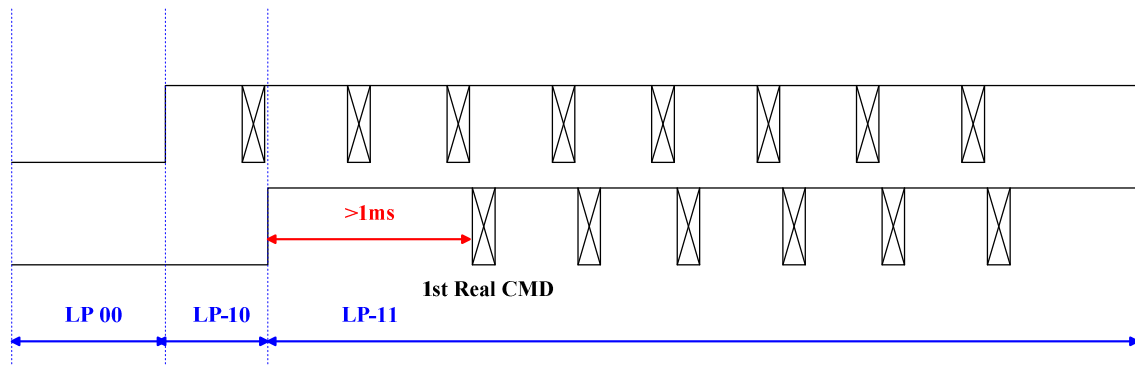
Mode1, the tearing effect output signal consists of V-sync information only.



Tvdh = The LCD display is not updated from the frame memory.

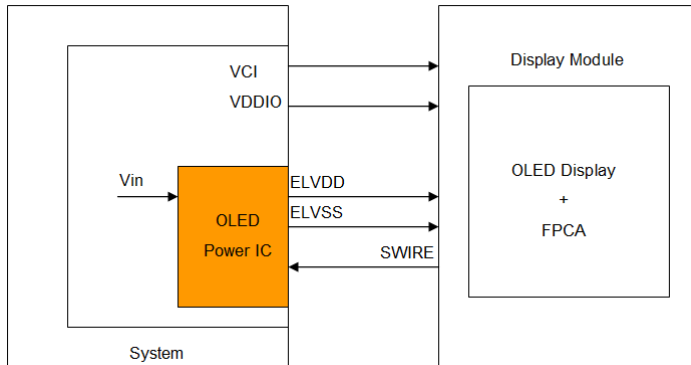
TvdL = The LCD display is updated from the frame memory.

MIPI Initial CMD Flow



6 Recommended Operating Sequence

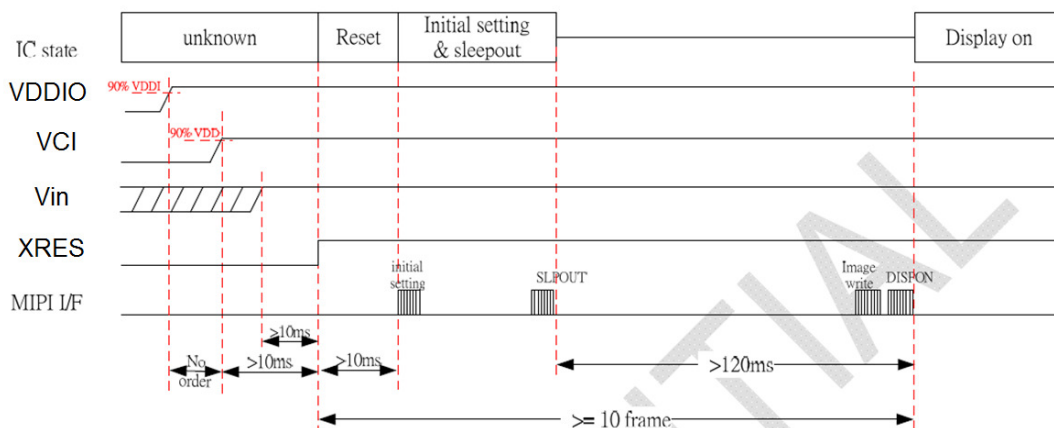
6.1 Power Structure



6.2 Display Power on / off Sequence

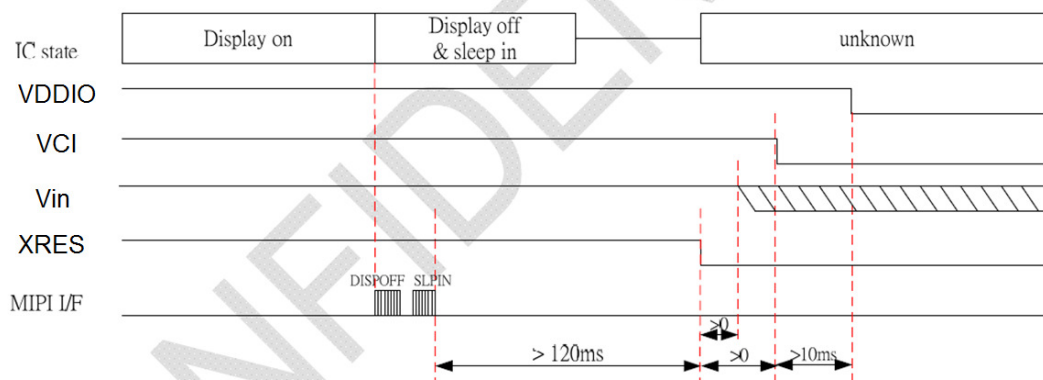
Power on sequence

Power On sequence



Power off sequence

Power Off sequence



7 Display Initial code Reference

Display Initial Setting

Recommended Power on Initial Sequence								
Step	Instruction /Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Turn on V _{CI}							V _{CI} =2.8V
2	Turn on V _{DDIO}							V _{DDIO} =1.8V
3	Delay	no limit						
4	REST pin low	20us						
5	REST pin high							
6	Delay	5 ms						
7			W	0x15	FE	FE00	05	
8			W	0x15	05	0580	00	
9			W	0x15	FE	FE00	07	
10			W	0x15	07	07A0	6D	
11			W	0x15	FE	FE00	0A	
12			W	0x15	1C	1CD0	1B	
13			W	0x15	FE	FE00	00	
14			W	0x15	35	3500	00	
15	Sleep out		W	0x05	11	1100	00	
16	Turn on peripheral packet			0x32				Video Turn On
17	Delay	300 ms						
18	Display on		W	0x05	29	2900	00	
Recommended Power off Initial Sequence								
Step	Instruction /Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Display Off		W	0x05	28	2800	00	
2	Sleep in		W	0x05	10	1000	00	
3	delay	120ms						
4	Power off							

Idle mode Flow

(1) Normal to Idle

Recommended Idle Initial Sequence								
Step	Instruction /Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Enter Idle mode		W	0x05	39	3900	00	Idle mode 15HZ

(2) Idle to Normal

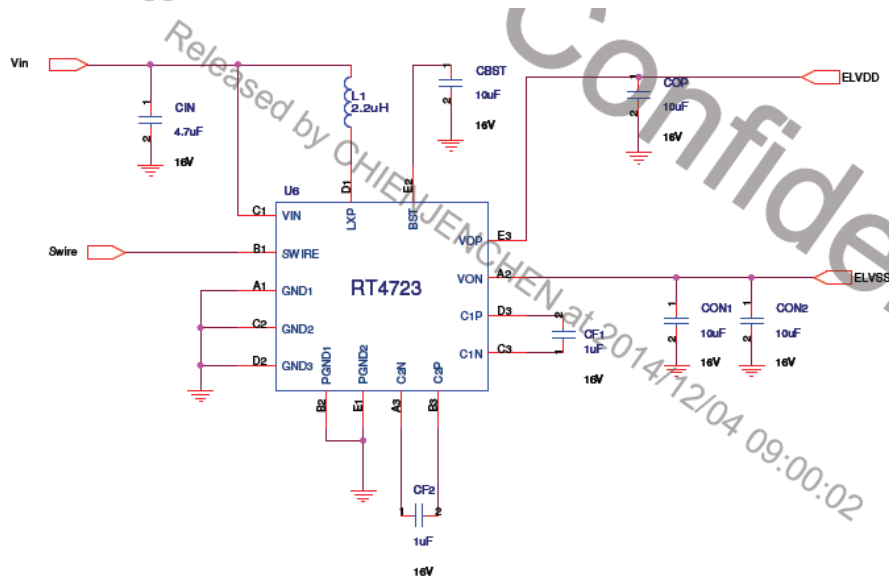
Recommended Power on Initial Sequence								
Step	Instruction /Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Idle mode Off		W	0x05	38	3800	00	Normal mode 60HZ

Brightness Control

Recommended Power on Initial Sequence								
Instruction /Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description	
				MIPI	Others			
Brightness control		W	0x05	51	5100	Value	Value form 0~255(FF)	

8 Application Circuit Reference

8.1 Power IC Application Circuit



1. AUO 1.39" panel has to be used with power IC RT4723, Richtek.

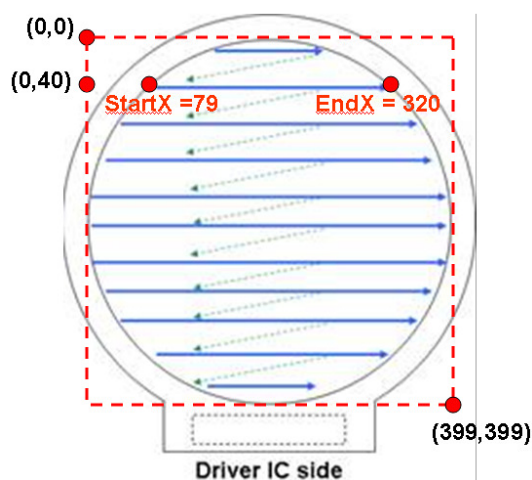
AUO don't suggest use other power IC instead of RT4723, since they don't be qualified by AUO.

2. Recommend power inductor L1

a. [TOKO - DFE252010C (1269AS-H-2R2N=P2)] 2.2uH 2.5mm*2.0mm*1.0mm

b. [Taiyo - MDKK2020T2R2MM] 2.2uH 2.0mm*2.0mm*1.0mm

8.2 Display Scan Direction & Coordinate



Panel Start Point = (0 , 0)

Panel End Point = (399 , 399)

Each Line = (Start x , y) ~ (End x , y)

Coordinate

Y	start X	start Y	Total	Y	start X	start Y	Total	Y	start X	start Y	Total
0	187	212	26	52	65	334	270	104	24	375	352
1	176	223	48	53	64	335	272	105	24	375	352
2	169	230	62	54	63	336	274	106	23	376	354
3	163	236	74	55	62	337	276	107	23	376	354
4	158	241	84	56	61	338	278	108	22	377	356
5	154	245	92	57	60	339	280	109	22	377	356
6	150	249	100	58	59	340	282	110	21	378	358
7	146	253	108	59	58	341	284	111	21	378	358
8	143	256	114	60	57	342	286	112	20	379	360
9	139	260	122	61	56	343	288	113	20	379	360
10	136	263	128	62	55	344	290	114	19	380	362
11	133	266	134	63	54	345	292	115	19	380	362
12	131	268	138	64	53	346	294	116	18	381	364
13	128	271	144	65	52	347	296	117	18	381	364
14	125	274	150	66	51	348	298	118	17	382	366
15	123	276	154	67	50	349	300	119	17	382	366
16	121	278	158	68	49	350	302	120	17	382	366
17	118	281	164	69	49	350	302	121	16	383	368
18	116	283	168	70	48	351	304	122	16	383	368
19	114	285	172	71	47	352	306	123	15	384	370
20	112	287	176	72	46	353	308	124	15	384	370
21	110	289	180	73	45	354	310	125	14	385	372
22	108	291	184	74	44	355	312	126	14	385	372
23	106	293	188	75	44	355	312	127	14	385	372
24	104	295	192	76	43	356	314	128	13	386	374
25	102	297	196	77	42	357	316	129	13	386	374
26	101	298	198	78	41	358	318	130	13	386	374
27	99	300	202	79	40	359	320	131	12	387	376
28	97	302	206	80	40	359	320	132	12	387	376
29	96	303	208	81	39	360	322	133	11	388	378
30	94	305	212	82	38	361	324	134	11	388	378
31	92	307	216	83	38	361	324	135	11	388	378
32	91	308	218	84	37	362	326	136	10	389	380
33	89	310	222	85	36	363	328	137	10	389	380
34	88	311	224	86	35	364	330	138	10	389	380
35	86	313	228	87	35	364	330	139	9	390	382
36	85	314	230	88	34	365	332	140	9	390	382
37	84	315	232	89	33	366	334	141	9	390	382
38	82	317	236	90	33	366	334	142	9	390	382
39	81	318	238	91	32	367	336	143	8	391	384
40	79	320	242	92	31	368	338	144	8	391	384
41	78	321	244	93	31	368	338	145	8	391	384
42	77	322	246	94	30	369	340	146	7	392	386
43	76	323	248	95	30	369	340	147	7	392	386
44	74	325	252	96	29	370	342	148	7	392	386
45	73	326	254	97	28	371	344	149	7	392	386
46	72	327	256	98	28	371	344	150	6	393	388
47	71	328	258	99	27	372	346	151	6	393	388
48	70	329	260	100	27	372	346	152	6	393	388
49	68	331	264	101	26	373	348	153	6	393	388
50	67	332	266	102	25	374	350	154	5	394	390
51	66	333	268	103	25	374	350	155	5	394	390

Y	start X	start Y	Total	Y	start X	start Y	Total	Y	start X	start Y	Total
156	5	394	390	209	0	399	400	262	10	389	380
157	5	394	390	210	0	399	400	263	10	389	380
158	4	395	392	211	0	399	400	264	11	388	378
159	4	395	392	212	0	399	400	265	11	388	378
160	4	395	392	213	1	398	398	266	11	388	378
161	4	395	392	214	1	398	398	267	12	387	376
162	4	395	392	215	1	398	398	268	12	387	376
163	3	396	394	216	1	398	398	269	13	386	374
164	3	396	394	217	1	398	398	270	13	386	374
165	3	396	394	218	1	398	398	271	13	386	374
166	3	396	394	219	1	398	398	272	14	385	372
167	3	396	394	220	1	398	398	273	14	385	372
168	3	396	394	221	1	398	398	274	14	385	372
169	2	397	396	222	1	398	398	275	15	384	370
170	2	397	396	223	1	398	398	276	15	384	370
171	2	397	396	224	2	397	396	277	16	383	368
172	2	397	396	225	2	397	396	278	16	383	368
173	2	397	396	226	2	397	396	279	17	382	366
174	2	397	396	227	2	397	396	280	17	382	366
175	2	397	396	228	2	397	396	281	17	382	366
176	1	398	398	229	2	397	396	282	18	381	364
177	1	398	398	230	2	397	396	283	18	381	364
178	1	398	398	231	3	396	394	284	19	380	362
179	1	398	398	232	3	396	394	285	19	380	362
180	1	398	398	233	3	396	394	286	20	379	360
181	1	398	398	234	3	396	394	287	20	379	360
182	1	398	398	235	3	396	394	288	21	378	358
183	1	398	398	236	3	396	394	289	21	378	358
184	1	398	398	237	4	395	392	290	22	377	356
185	1	398	398	238	4	395	392	291	22	377	356
186	1	398	398	239	4	395	392	292	23	376	354
187	0	399	400	240	4	395	392	293	23	376	354
188	0	399	400	241	4	395	392	294	24	375	352
189	0	399	400	242	5	394	390	295	24	375	352
190	0	399	400	243	5	394	390	296	25	374	350
191	0	399	400	244	5	394	390	297	25	374	350
192	0	399	400	245	5	394	390	298	26	373	348
193	0	399	400	246	6	393	388	299	27	372	346
194	0	399	400	247	6	393	388	300	27	372	346
195	0	399	400	248	6	393	388	301	28	371	344
196	0	399	400	249	6	393	388	302	28	371	344
197	0	399	400	250	7	392	386	303	29	370	342
198	0	399	400	251	7	392	386	304	30	369	340
199	0	399	400	252	7	392	386	305	30	369	340
200	0	399	400	253	7	392	386	306	31	368	338
201	0	399	400	254	8	391	384	307	31	368	338
202	0	399	400	255	8	391	384	308	32	367	336
203	0	399	400	256	8	391	384	309	33	366	334
204	0	399	400	257	9	390	382	310	33	366	334
205	0	399	400	258	9	390	382	311	34	365	332
206	0	399	400	259	9	390	382	312	35	364	330
207	0	399	400	260	9	390	382	313	35	364	330
208	0	399	400	261	10	389	380	314	36	363	328

Y	start X	start Y	Total	Y	start X	start Y	Total
315	37	362	326	360	81	318	238
316	38	361	324	361	82	317	236
317	38	361	324	362	84	315	232
318	39	360	322	363	85	314	230
319	40	359	320	364	86	313	228
320	40	359	320	365	88	311	224
321	41	358	318	366	89	310	222
322	42	357	316	367	91	308	218
323	43	356	314	368	92	307	216
324	44	355	312	369	94	305	212
325	44	355	312	370	96	303	208
326	45	354	310	371	97	302	206
327	46	353	308	372	99	300	202
328	47	352	306	373	101	298	198
329	48	351	304	374	102	297	196
330	49	350	302	375	104	295	192
331	49	350	302	376	106	293	188
332	50	349	300	377	108	291	184
333	51	348	298	378	110	289	180
334	52	347	296	379	112	287	176
335	53	346	294	380	114	285	172
336	54	345	292	381	116	283	168
337	55	344	290	382	118	281	164
338	56	343	288	383	121	278	158
339	57	342	286	384	123	276	154
340	58	341	284	385	125	274	150
341	59	340	282	386	128	271	144
342	60	339	280	387	131	268	138
343	61	338	278	388	133	266	134
344	62	337	276	389	136	263	128
345	63	336	274	390	139	260	122
346	64	335	272	391	143	256	114
347	65	334	270	392	146	253	108
348	66	333	268	393	150	249	100
349	67	332	266	394	154	245	92
350	68	331	264	395	158	241	84
351	70	329	260	396	163	236	74
352	71	328	258	397	169	230	62
353	72	327	256	398	176	223	48
354	73	326	254	399	187	212	26
355	74	325	252				
356	76	323	248				
357	77	322	246				
358	78	321	244				
359	79	320	242				

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	70°C 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30°C 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	60°C 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 240hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-40°C/70°C 100cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

10 Warranty and Conditions

<http://www.displaymodule.com/pages/faq> HYPERLINK

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