DisplayModule

DM-OLEDC13-621P

1.27" 128X96 RGB COLOR OLED DISPLAY PANEL - SPI, MCU

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1 Revision History

Date	Changes
2015-03-13	First release
2018-05-29	Mainboard update to new version ,Interface change to SPI

2 Main Features

Item	Specification	Unit
Diagonal Size	1.27	inch
Display Mode	Passive Matrix OLED	-
Display Colors	262,144	Colors
Resolution	128(RGB) x 96	pixel
Controller IC	SSD1351	-
Duty	1/96	duty
Interface	3/4 wire SPI, 8 bit 68XX/80XX	-
Power Supply	2.8V	V
Active Area	25.708 x 19.28	mm
Module Dimension	33.7 x 26.9	mm
Weight	2.92	g

3 Pin Description

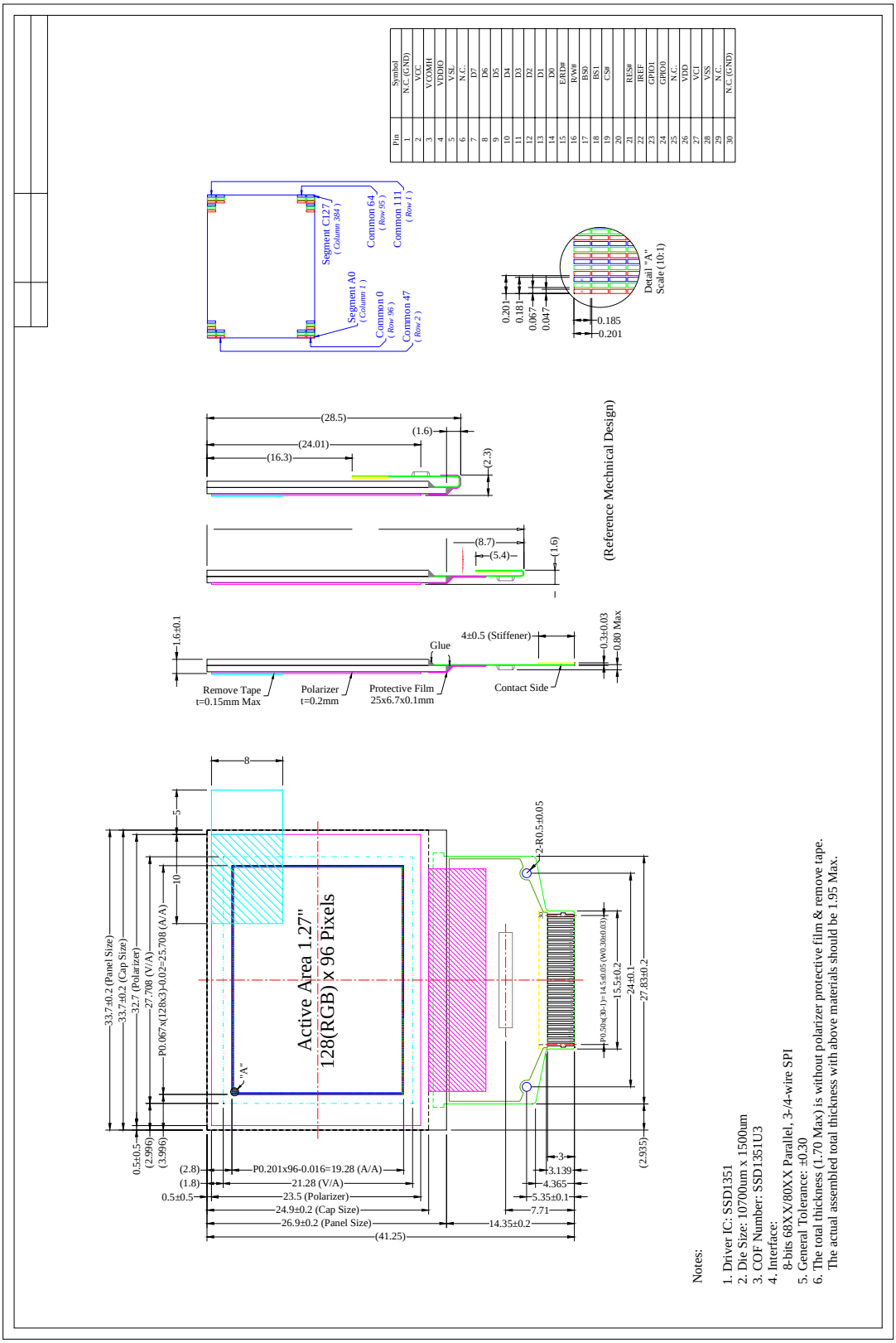
3.1 Panel Pin Description

Pin No.	Symbol	Function Description
1	NC(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.
2	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.
3	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
4	VDDIO	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.
5	VSL	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
6	N.C.	Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design.
7~14	D7~D0	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2.
15	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
16	R/W#	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
17 18	BS1 BS0	Communicating Protocol Select These pins are MCU interface selection input. See the following table:

	BS0	BS1
3-wire SPI	1	0
4-wire SPI	0	0

		68XX-parallel (8-bit) | 1 | 1 80XX-parallel (8-bit) | 0 | 1
19	CS#	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
20	D/C#	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When 3-wire serial mode is selected, this pin must be connected to VSS.
21	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed.
22	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5uA.
23 24	GPIO0 GPIO1	General Purpose Input/Output These pins could be left open individually or have signal inputted/outputted. They are able to use as the external DC/DC converter circuit enabled/disabled control or other applications.
25	N.C.	Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design.
26	VDD	Power Supply for Core Logic Circuit This is a voltage supply pin which is regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
27	VCI	Power Supply for Operation This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
28	VSS	Ground of OEL System This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
29	N.C.	Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design.
30	N.C.(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

4 Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	3.3	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	VCC	Note1	11.5	12	12.5	V
Operation Current for VCI	I_{CI}		-	240	300	mA
Low Level Input Voltage	V_{IL}		0	-	$0.2xV_{DDIO}$	V
High Level Input Voltage	V_{IH}		$0.8xV_{DD}$	-	V_{DDIO}	V
Low Level Output Voltage	V_{OL}		0		$0.1xV_{DDIO}$	V
High Level Output Voltage	V_{OH}		$0.9xV_{DDIO}$		V_{DDIO}	V
Operating Temperature	TOP	Absolute Max	-30		70	℃
Storage Temperature	TST	Absolute Max	-40		80	℃

Note1 :Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer’s request.

6 Optical Characteristics

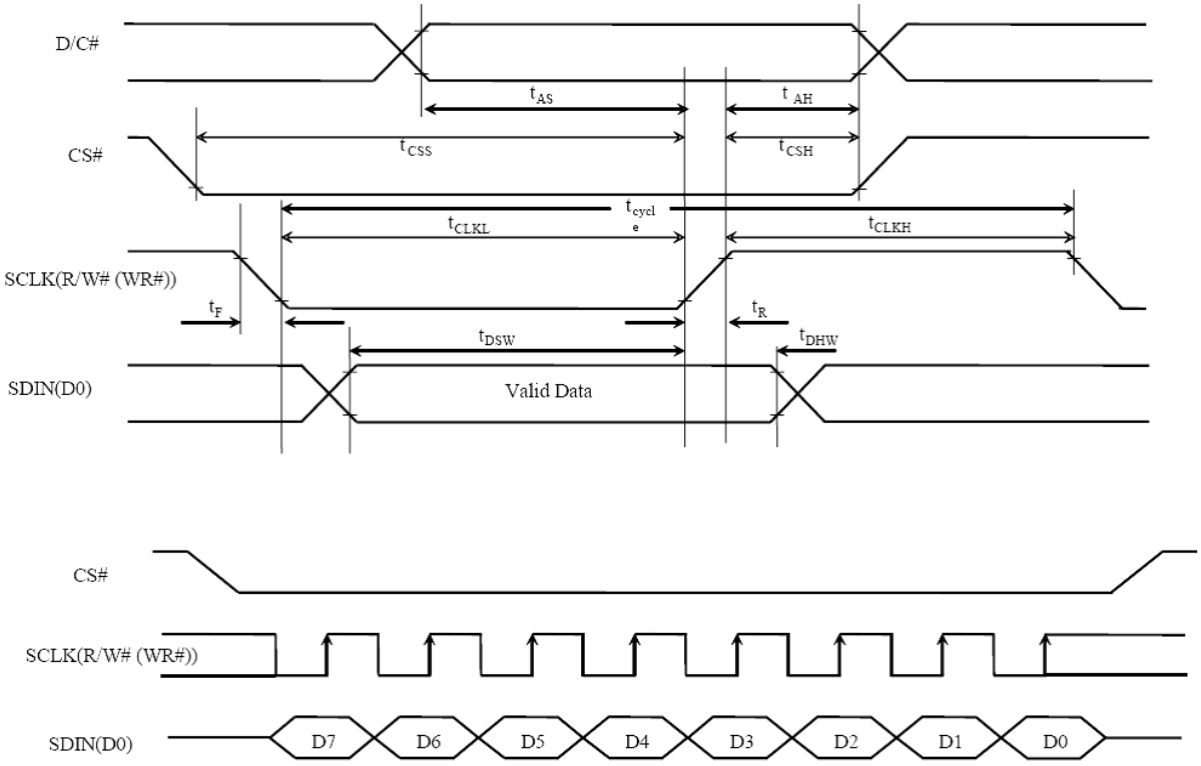
Item	Symbol	Min	Typ	Max	Unit
View Angles Top	AV		80		°
View Angles Bottom	AV		80		°
View Angles Left	AH		80		°
View Angles Right	AH		80		°
Response Time (25℃)	Tr + Tf		20		us
Brightness		80	100		cd/m^2
Contrast Ratio	CR		2,000:1		
Lifetime		10,000			Hrs

7 Timing Characteristics

7.1 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15			ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-		ns
t_{CLKL}	Clock Low Time	20	-		ns
t_{CLKH}	Clock High Time	20			ns
t_R	Rise Time	-		15	ns
t_F	Fall Time	-		15	ns

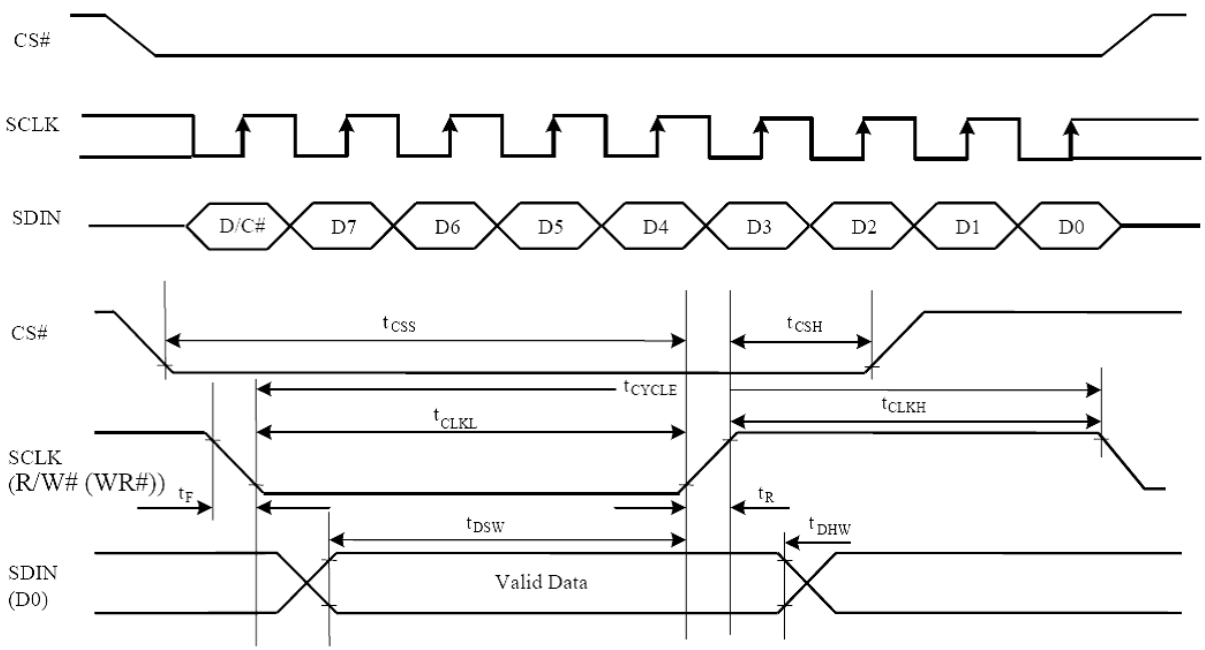
V_{DD}-V_{SS} =2.4V to 2.6V, V_{DDIO}=1.65V, V_{CI}=2.8V, Ta=25 ℃



7.2 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-		ns
t_{CLKL}	Clock Low Time	20	-		ns
t_{CLKH}	Clock High Time	20			ns
t_R	Rise Time	-		15	ns
t_F	Fall Time	-		15	ns

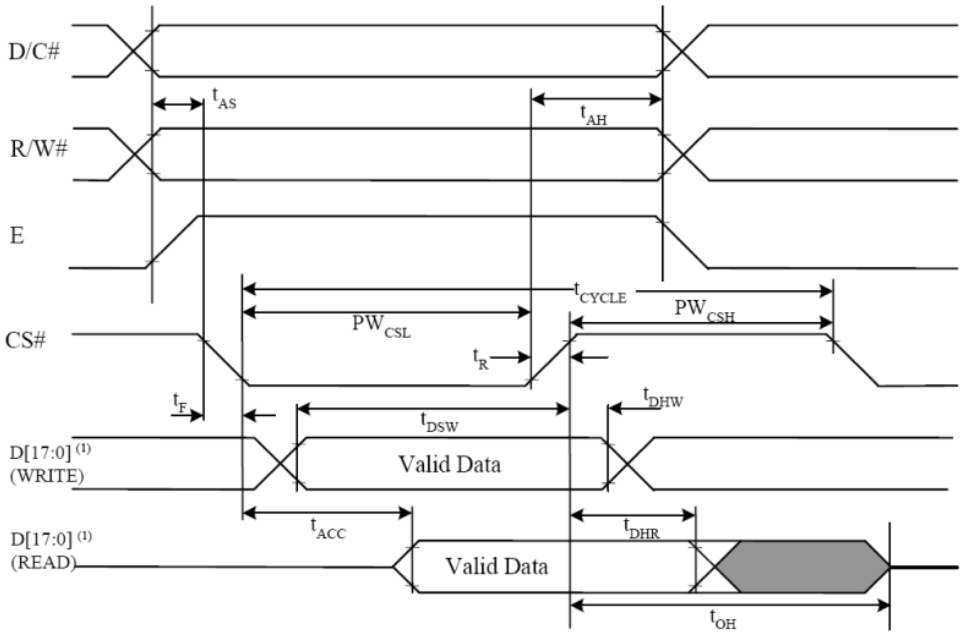
V_{DD}-V_{SS} =2.4V to 2.6V, V_{DDIO}=1.65V, V_{CI}=2.8V, Ta=25 ℃



7.3 68XX-Seriel MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 2.8V, T_a = 25°C)

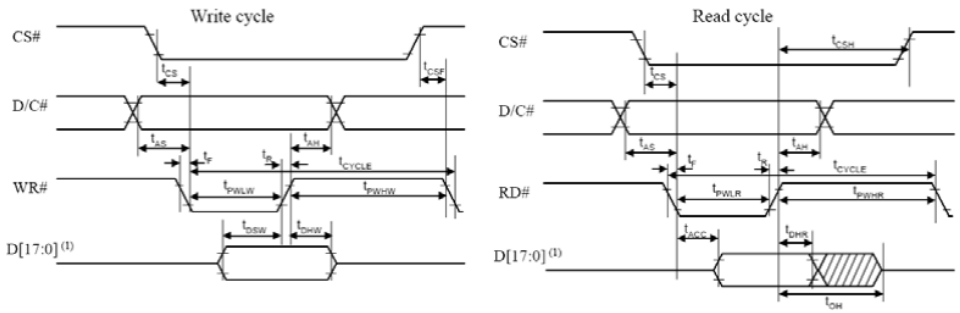


* (1) When 8-bit Used: D[7:0] Instead

7.4 80XX-Seriel MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
CSH	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 2.8V, T_a = 25°C)



* (1) When 8-bit Used: D[7:0] Instead

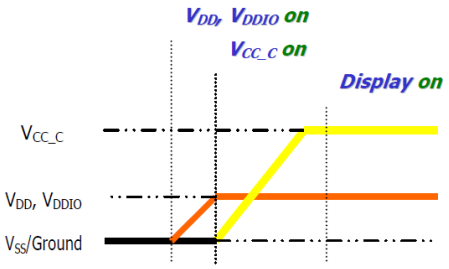
8 Functional Specification

8.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

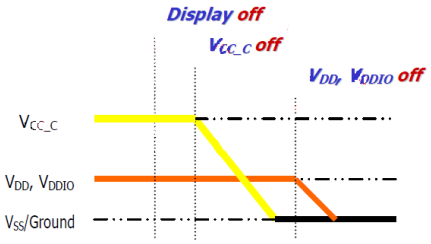
8.1.1 Power up Sequence

1. Power up V_{DD}&V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms(When V_{CC} is stable)
7. Send Display on command



8.1.2 Power down Sequence

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD} &V_{DDIO}



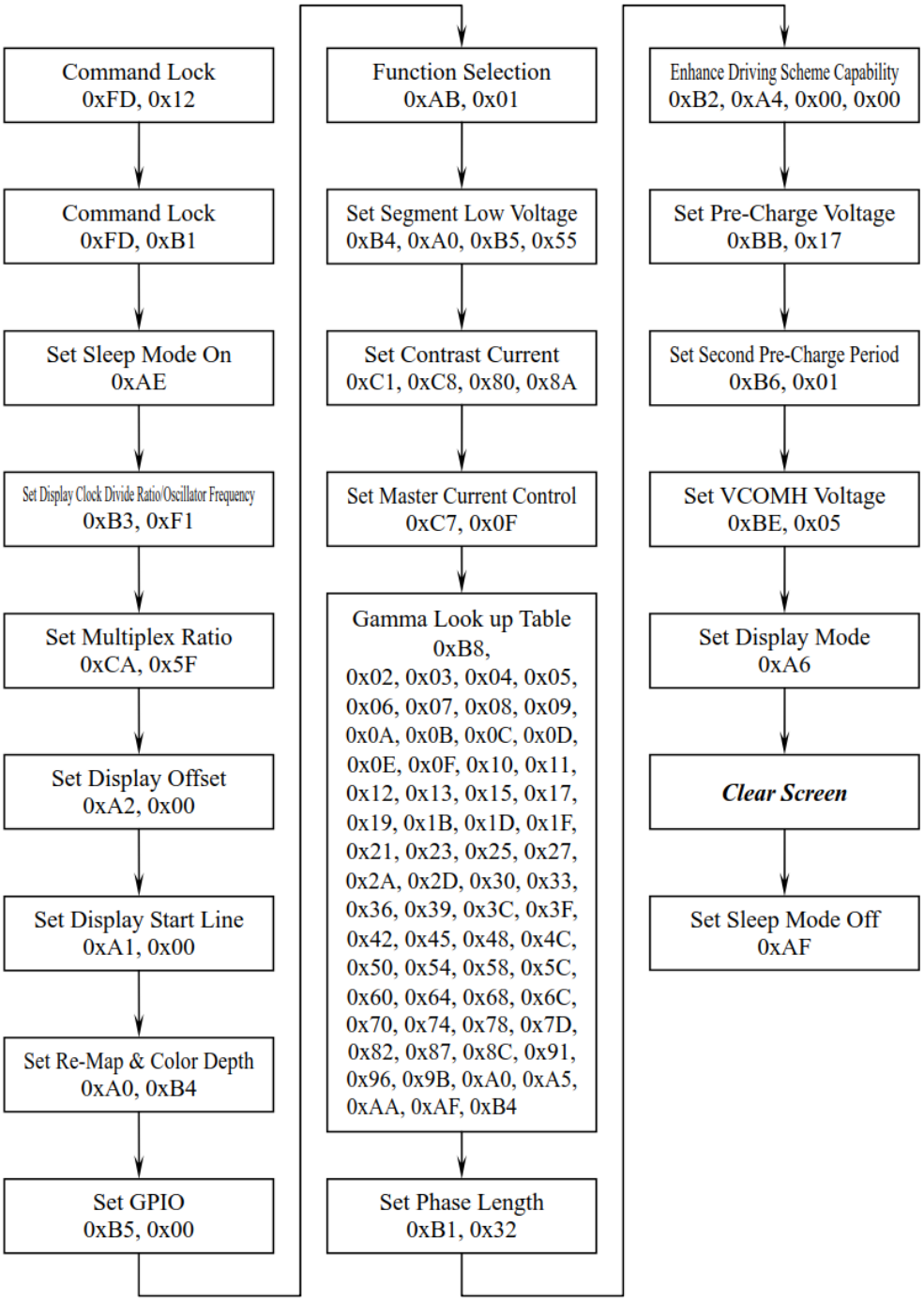
8.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128(RGB) x 128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Command A2h, B1h, B3h, BBh, BEh are locked by command FDh

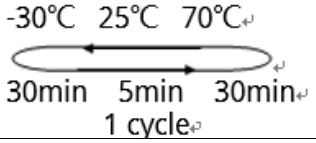
9 Actual Application Example

<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

10 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30 °C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-30°C/70°C 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container.

11 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"