DisplayModule

DM-OLED55-672

5.5" 256 × 64 MONOCHROME GRAPHIC OLED DISPLAY MODULE -MCU,SPI,

Contents

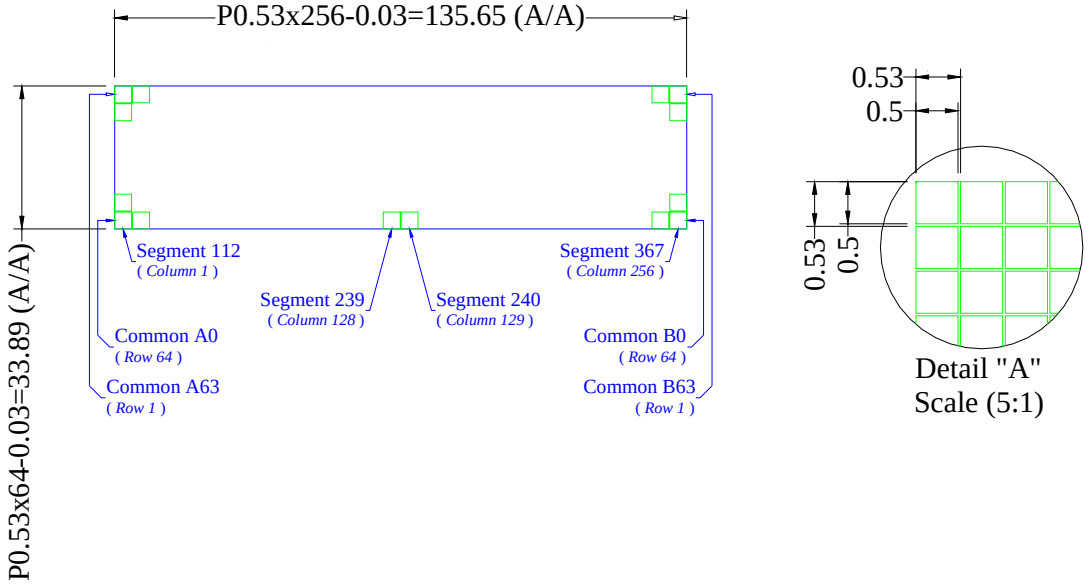
1 Revision History

Date	Changes
2022-08-25	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	5.5	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome	Colors
Resolution	256 × 64	pixel
Controller IC	SSD1322	-
Interface	6060/8080MCU、SPI	-
Active Area	135.65 × 33.89	mm
Panel Dimension	146 × 45 × 2	mm
Pixel Size	0.53 × 0.53	mm
Pixel Pitch	0.50 × 0.50	mm
Weight	27.1	g

2.1 Active Area & Pixel Construction



3 Pin Description

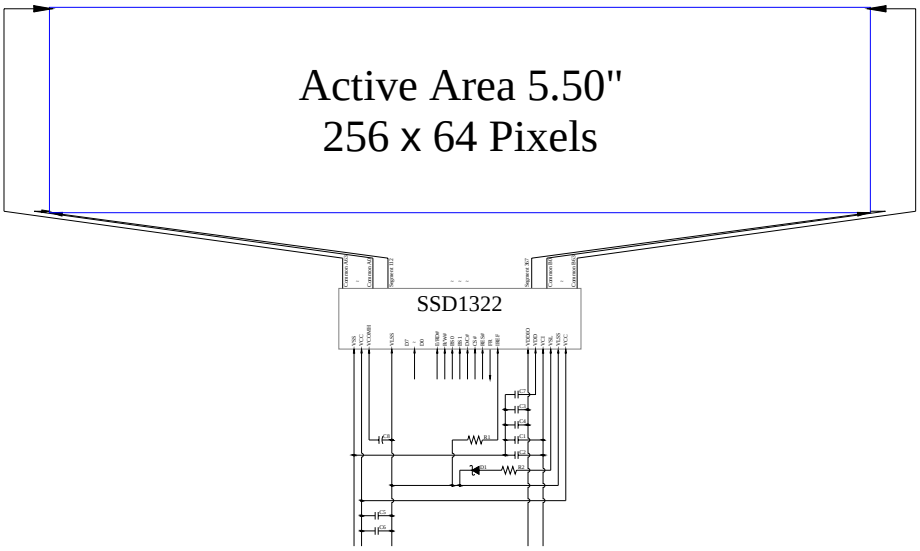
3.1 Panel Pin Description

Pin Number	Symbol	Type	Function
Power Supply			
26	VCI	P	*Power Supply for Operation* This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
25	VDD	P	*Power Supply for Core Logic Circuit* This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
24	VDDIO	P	*Power Supply for I/O Pin* This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.
2	VSS	P	*Ground of Logic Circuit* This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3, 29	VCC	P	*Powe Supply for OEL Panel* These are the most positive voltage supply pin of the chip. They must be connected to external source.
5, 28	VLSS	P	*Ground of Analog Circuit* These are the analog ground pins. They should be connected to VSS externally.
Driver			
22	IREF	I	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA.
4	VCOMH	P	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
27	VSL	P	*Voltage Output Low Level for SEG Signal* This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
Testing Pads			
21	FR	O	*Frame Frequency Triggering Signal* This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>16
17</td><td>BS0
BS1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS0</td><td>BS1</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>20</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>18</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>14</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>15</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>6~13</td><td>D7~D0</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
Unused pins must be connected to VSS except for D2 in serial mode.</td></tr>
</table>

Pin Number	Symbol	I/O	Function
Reserve			
23	N.C.	-	*Reserved Pin* The N.C. pin between function pins are reserved for compatible and flexible design.
1, 30	N.C. (GND)	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

3.2 FUNCTION BLOCK DIAGRAM

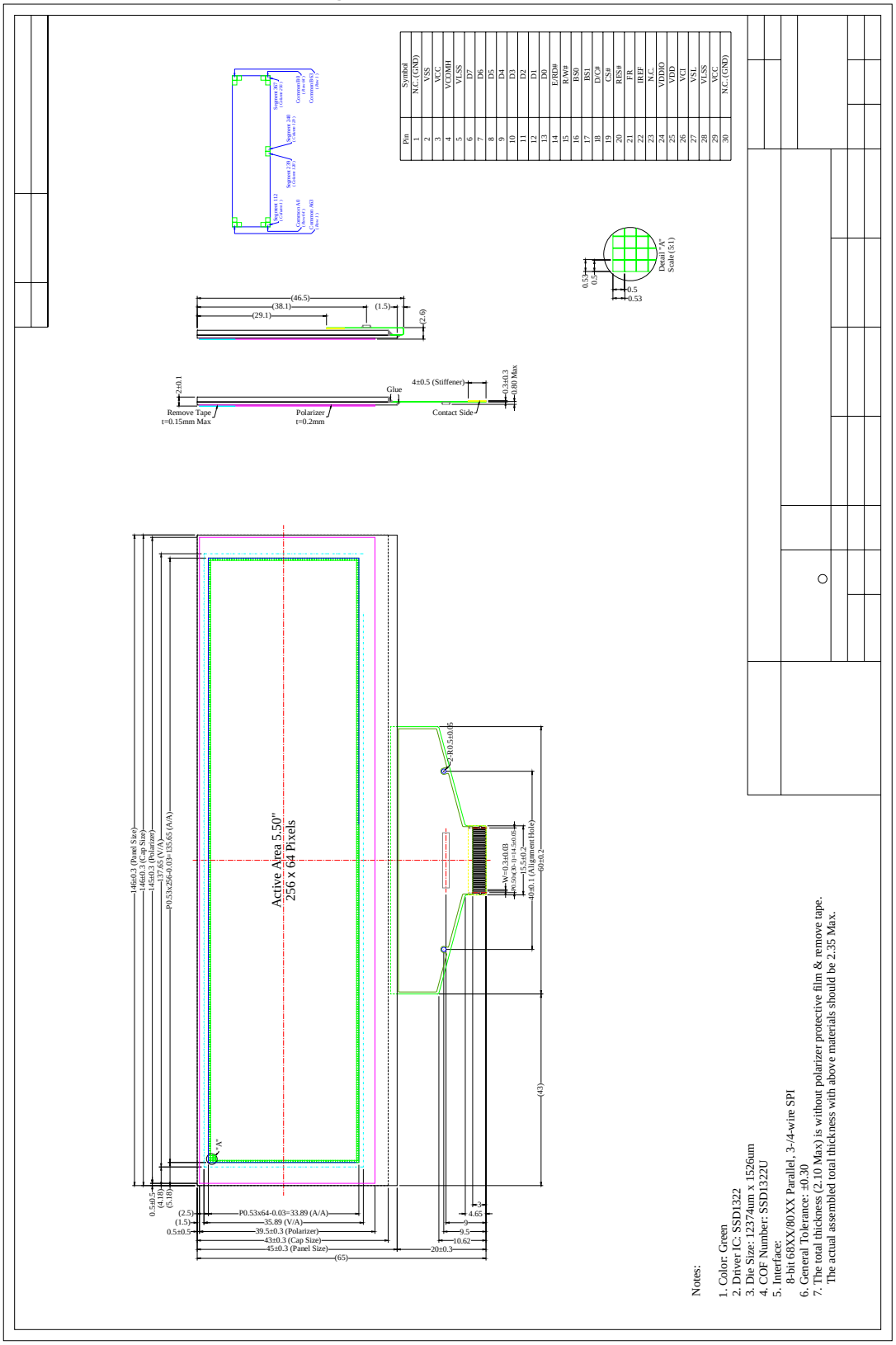


MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#

C1, C3, C5: 0.1µF
C2, C4: 4.7 F
C6: 20µF
C7: 1µF
C8: 4.7uF / 25V Tantalum Capacitor
R1: 910kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Current for V_{CC}	I_{CC}	-	80	mA	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

6 Optics & Electrical Characteristics

6.1 Optical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	60	80	-	cd/m^2
C.I.E. (Green)	(x) (y)	Without Polarizer	0.27 0.58	0.31 0.62	0.35 0.66	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 15V.
Software configuration follows Section 4.4 Initialization.

6.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V	V
Supply Voltage for Display	V_{CC}	Note 3	14.5	15	15.5	V
High Level Input	V_{IH}		$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2\times V_{DDIO}$	V
High Level Output	V_{OH}	I_{out} = 100µA, 3.3MHz	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} = 100µA, 3.3MHz	0	-	$0.1\times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	39.8	49.8	mA
		Note 5	-	64.0	80.0	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	1	5	µA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	µA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{CI} = 2.8V, V_{CC} = 15V, 50% Display Area Turn on.
Note 5: V_{CI} = 2.8V, V_{CC} = 15V, 100% Display Area Turn on.

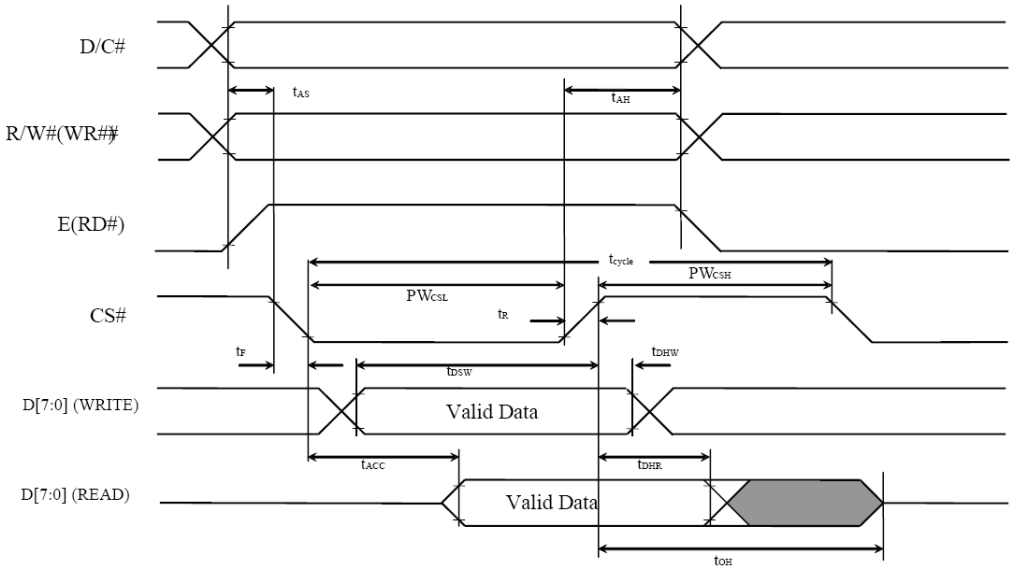
* Software configuration follows Section 4.4 Initialization.

6.3 AC Characteristics

7.2.1. 68XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

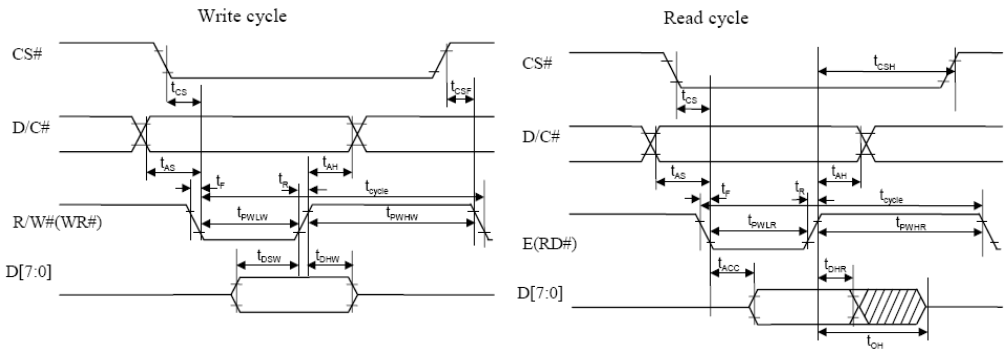
* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



7.2.2. 80XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

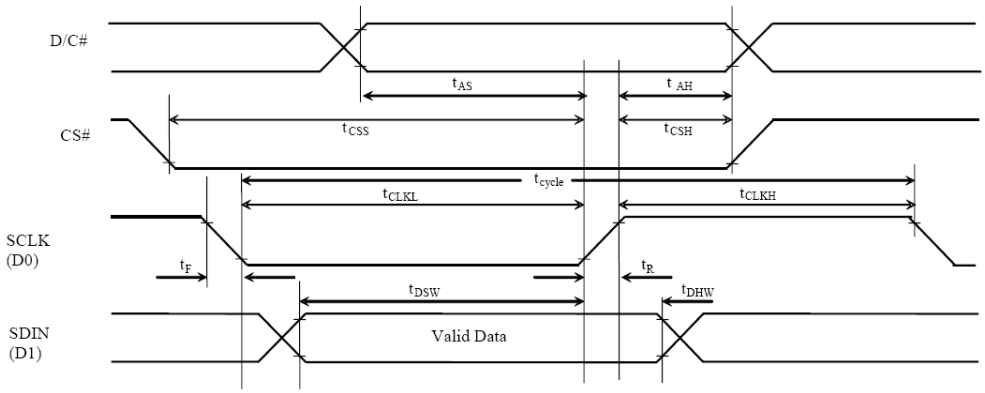
* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

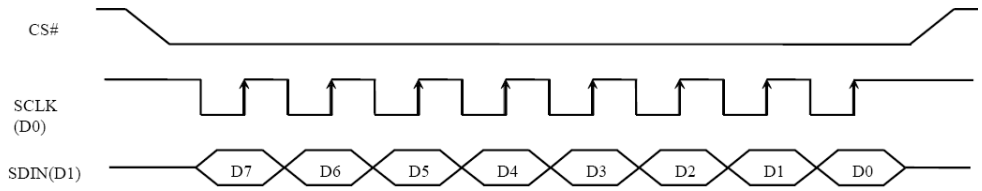


7.2.3. Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

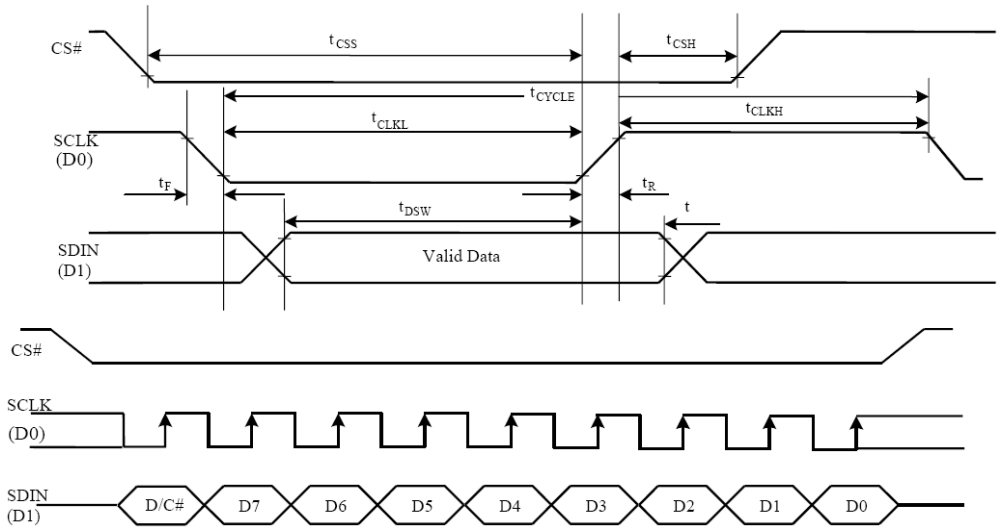




7.2.4. Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



7 Functional Specification

7.1 Commands

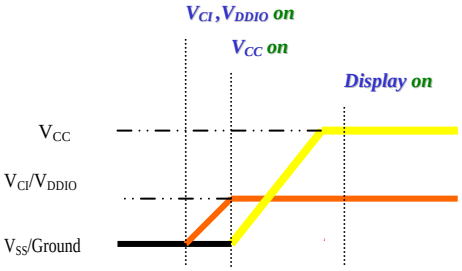
Refer to the Technical Manual for the SSD1322

7.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/downroutine should include a delay period between high voltage and low voltage powersources during turn on/off. It gives the OEL panel enough time to complete theaction of charge and discharge before/after the operation.

7.2.1. Power up Sequence:

1. Power up VCI& VDDIO
2. Send Display off command3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 100ms(When Vcc is stable)
7. Send Display on command

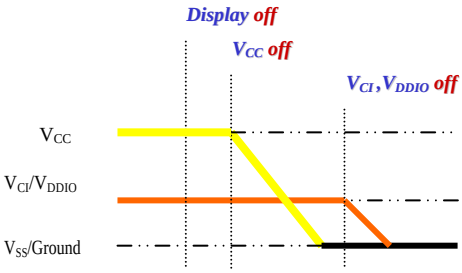


7.2.2. Power down Sequence:

1. Send Display off command
2. Power down VCC
3. Delay 100ms

(When VCCis reach 0 and panelis completely discharges)

4. Power down VCI& VDDIO



7.3 Reset Circuit

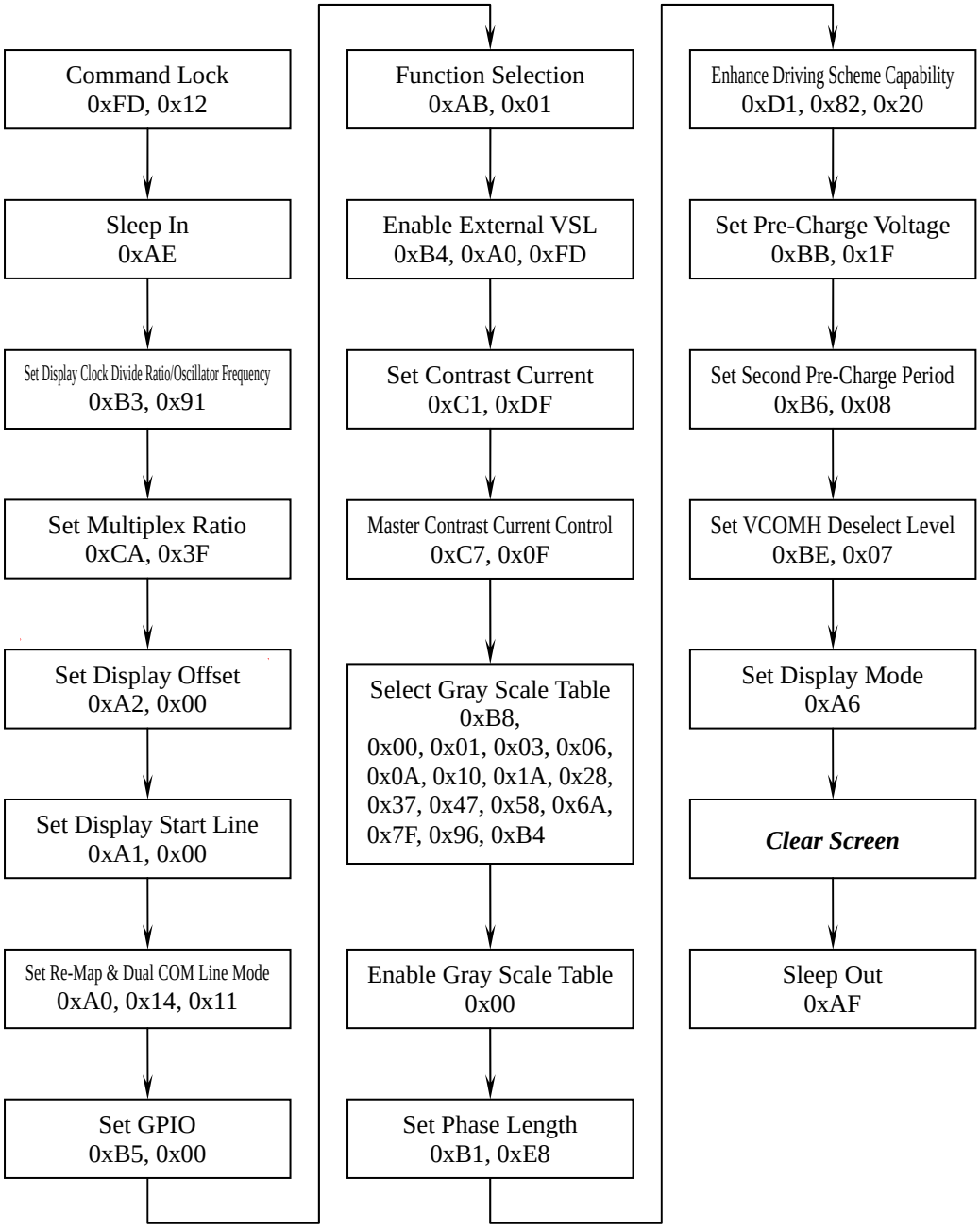
When RES# input is low, the chip isinitialized withthe following status:

1. Display is OFF
2. 480×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control registers is set at 7Fh

7.4 Actual Application Example

Command usage and explanation of an actual example<Initialization>

<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

8 Reliability

8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Storage	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

8.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	40,000	-	hr	80 cd/m^2, 50% Checkerboard	6

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

8.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"