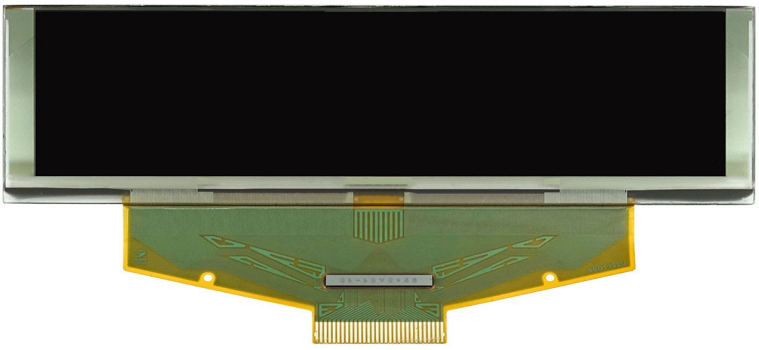
DisplayModule



DM-OLED32-648

MONOCHROME GRAPHIC OLED DISPLAY PANEL-SPI,MCU

Contents

1 Revision History

Date	Changes
2019-05-31	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	3.2	inch
Display Mode	OLED	-
Display Colors	Monochrome White/Yellow/Blue/Green	
Resolution	256 x 64	pixel
Controller IC	SSD1322	-
Duty	1/64	
Interface	8-Bit 6800/8080 Parallel、3/4-Wire Serial SPI	
Power Supply	3.3V/5V	V
Viewing Area	78.78 x 21.18	mm
Weight	9.95	g

3 Pin Description

Pin No.	Symbol	Function Description
1	N.C(GND)	Reserved Pin(Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.
2	VSS	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3	VCC	Power supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.
4	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.
6-13	D7-D0	Host Data Input/ Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.
14	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
15	R/W#	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must

<table>
<tr><td></td><td></td><td>be connected to VSS.</td></tr>
<tr><td>16-17</td><td>BS0
BS1</td><td>Communicating Protocol Select

These pin are MCU interface selection input. See the following table:

<table><tr><td></td><td>BS0</td><td>BS1</td></tr><tr><td>3-wire SPI</td><td>1</td><td>0</td></tr><tr><td>4-wire SPI</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr></table></td></tr>
<tr><td>18</td><td>D/C#</td><td>Data/Command Control

This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>19</td><td>CS#</td><td>Chip Select

This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>20</td><td>RES#</td><td>Power Reset for Controller and Driver

This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>21</td><td>FR</td><td>Cascade Application Connection Pin

This pin is No Connection pins. Nothing should be connected to this pin. It should be left open individually</td></tr>
<tr><td>22</td><td>IREF</td><td>Current Reference for Brightness Adjustment

This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA</td></tr>
<tr><td>23</td><td>N.C</td><td>Reserved Pin

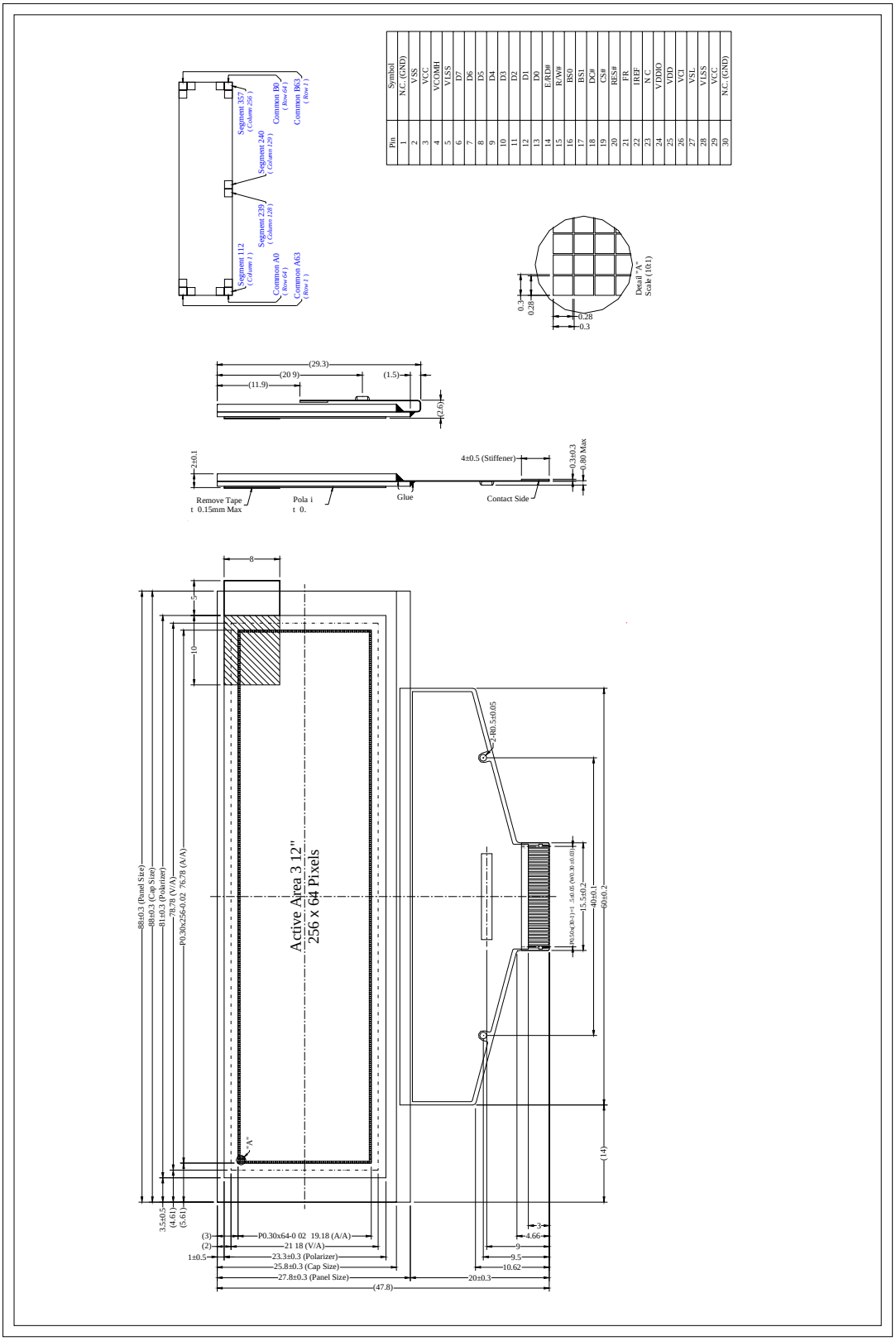
No connection</td></tr>
<tr><td>24</td><td>VDDIO</td><td>Power Supply for I/O Pin

This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.</td></tr>
<tr><td>25</td><td>VDD</td><td>Power Supply for Core Logic Circuit

This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.</td></tr>
<tr><td>26</td><td>VCI</td><td>Power Supply for Operation</td></tr>
</table>

		This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
27	VSL	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
28	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.
29	VCC	Power supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.
30	N.C(GND)	Reserved Pin(Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

4 Mechanical Drawing



5 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1,2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1,2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1,2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1,2
Operating Current for V_{CC}	I_{CC}	-	55	mA	1,2
Operating Temperature	T_{OP}	-30	85	℃	
Storage Temperature	T_{STG}	-40	90	℃	

Note1:All above voltage are on the basis of “VSS=0V”.

Note2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to the “Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

6 Electrical Characteristics

6.1 DC Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note1	11.5	12.0	12.5	V
Low Level Input Voltage	V_{IL}		0	-	0.2 V_{DDIO}	V
High Level Input Voltage	V_{IH}		0.8 V_{DDIO}	-	V_{DDIO}	V
Low Level Output Voltage	V_{OL}	Iout=100uA, 3.3MHz	0		0.1 V_{DDIO}	V
High Level Output Voltage	V_{OH}	Iout=100uA, 3.3MHz	0.9 V_{DDIO}		V_{DDIO}	V
Operating Current for V_{CI}	I_{CI}	Note2	-	1.8	2.25	mA
		Note3		1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note2	-	25.5	31.9	mA
		Note3		40.1	51.1	mA
Sleep Mode Current for V_{CI}	$I_{CI,SLEEP}$		-	1	5	uA
Sleep Mode Current for V_{CC}	$I_{CC,SLEEP}$		-	1	5	uA

Note1 : Brightness (Lbr) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer’s request.
Note2: V_{CI} = 2.8V, V_{CC} = 12V, 50% Display Area Turn on.
Note3: V_{CI} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.

6.2 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles Left			80		°
View Angles Right			80		°
View Angles Top			80		°
View Angles Bottom			80		°
C.I.E(Yellow)	(x) (y)	Without Polarizer	0.44 0.46	0.48 0.50	0.52 0.54
Contrast Ratio	CR		＞2000:1		
Brightness	L_{br}	60	80		cd/m ²

Note: Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 12V

7 MCU Interface

MCU interface assignment under different bus interface mode

Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	TieLOW		CS#	D/C#	RES#

7.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

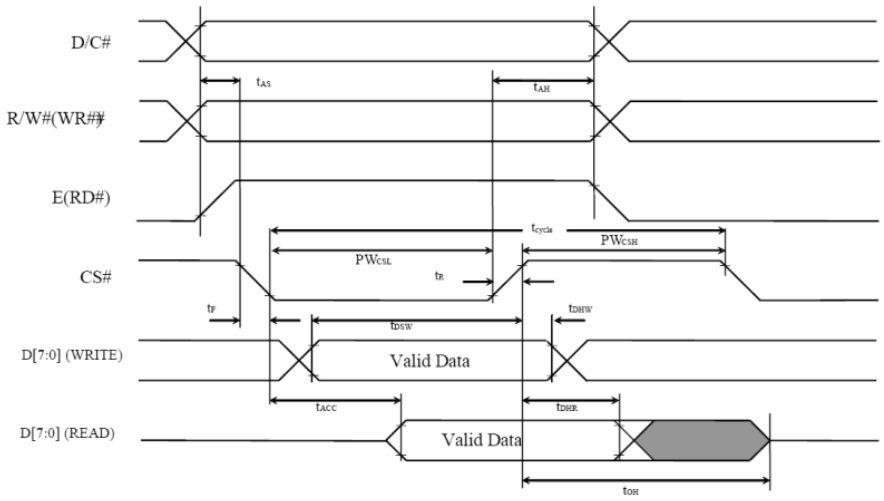
A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note: ↓stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



7.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

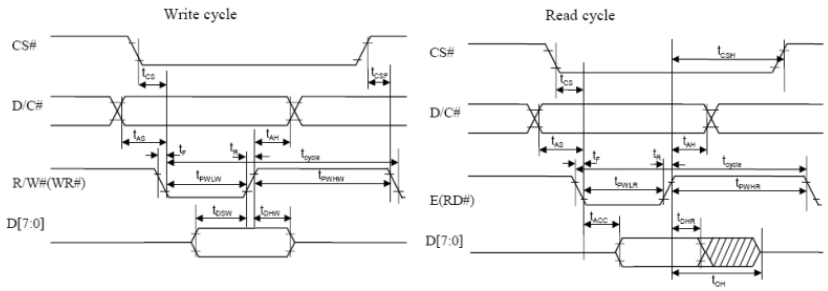
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note: ↑ stands for rising edge of signal
H stands for HIGH in signal
L stands for LOW in signal

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



7.3 MCU Serial Interface (4-wire SPI)

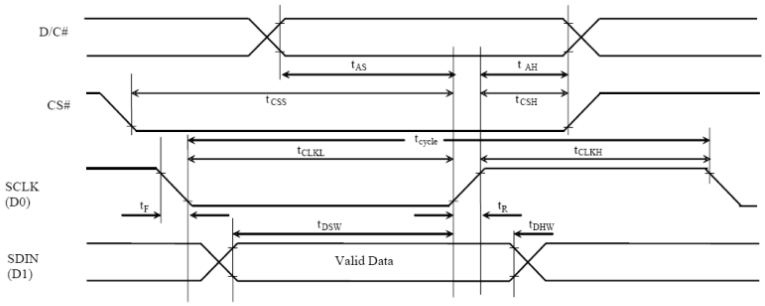
The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

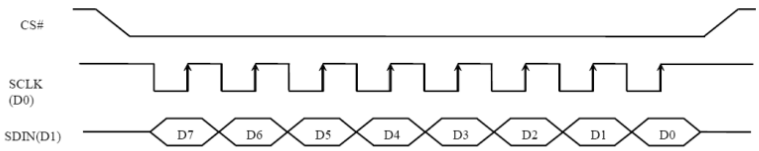
Function	E(RD#)	R/W#(WR#)	CS#	DC#	D0#
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note: H stands for HIGH in signal
L stands for LOW in signal

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)





7.4 MCU Serial Interface (3-wire SPI)

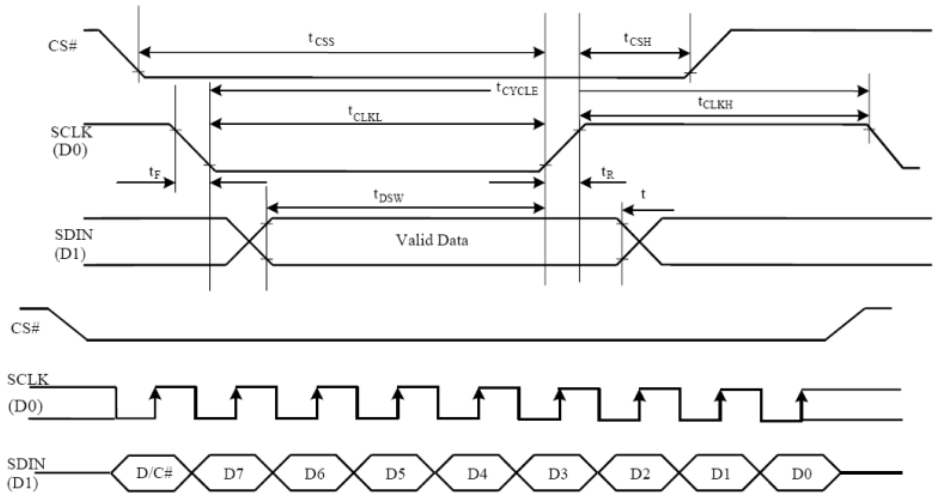
The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

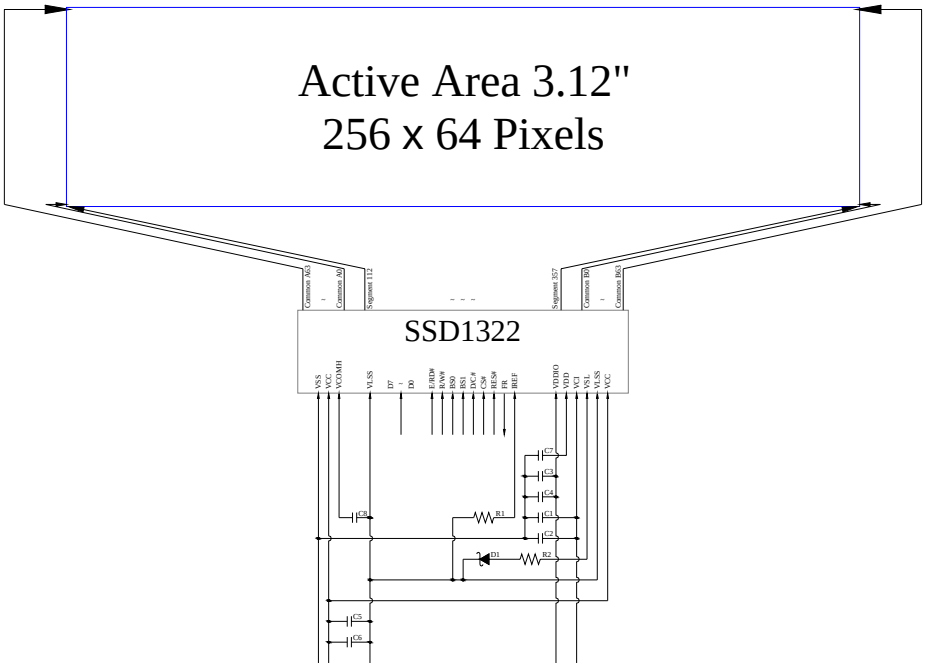
Note: L stands for LOW in signal

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



8 Block Diagram

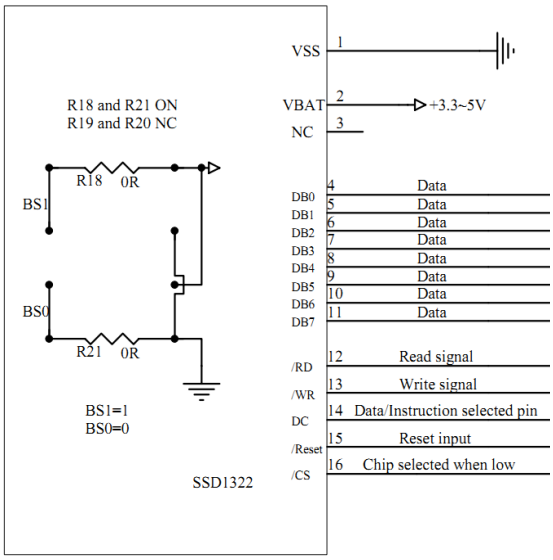


MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#

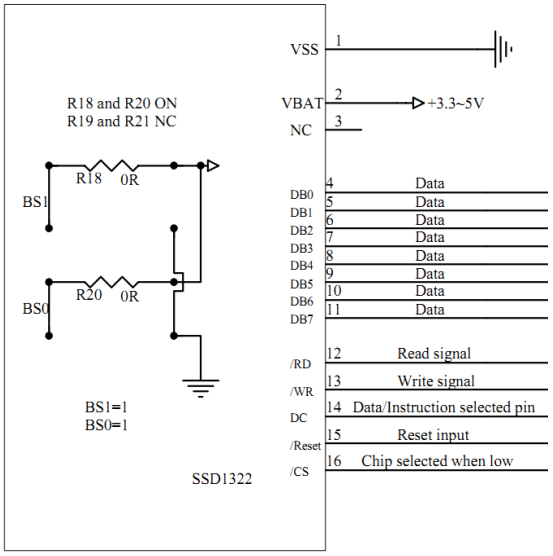
C1, C3, C5: 0.1µF
C2, C4: 4.7µF
C6: 10µF
C7: 1µF
C8: 4.7uF / 25V Tantalum Capacitor
R1: 680kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

9 Application Reference

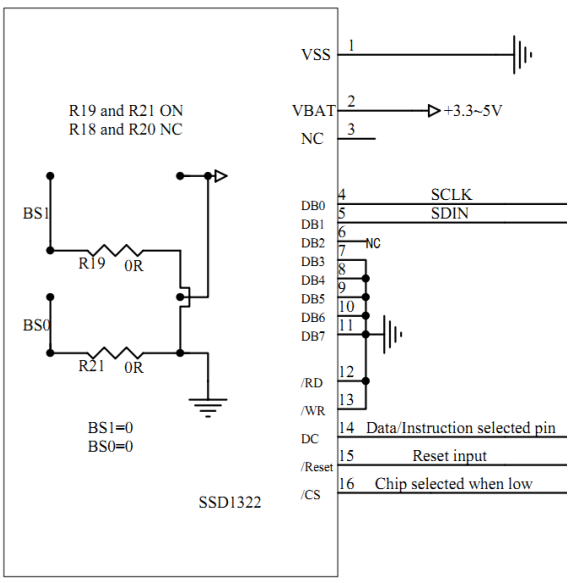
The Parallel (8080 Series MCU)Reference Example



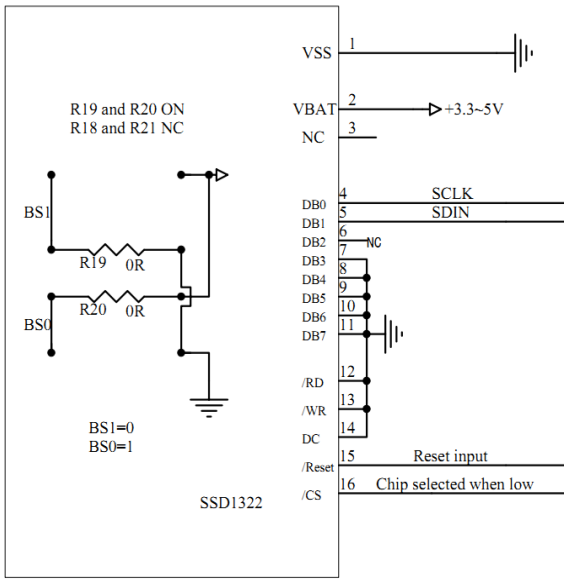
The Parallel (6800 Series MCU)Reference Example



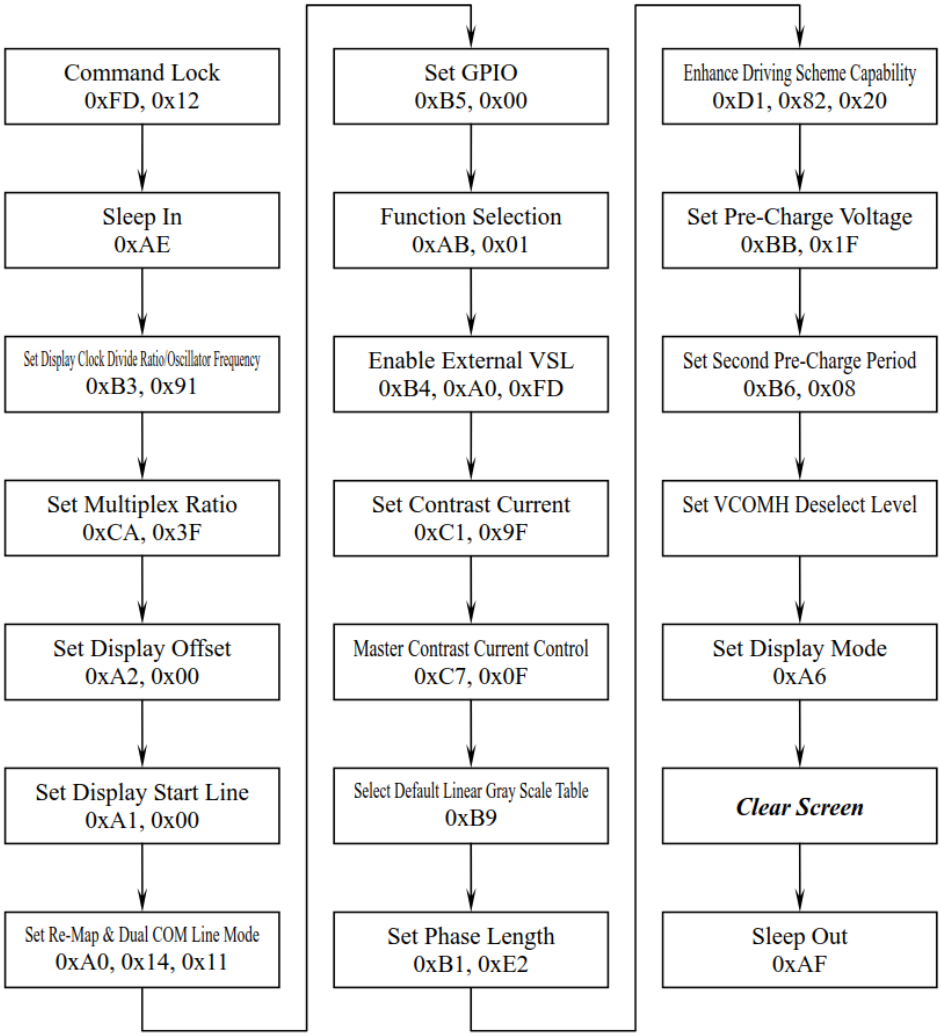
The Serial 4 Line SPI Reference Example



The Serial 3 Line SPI Reference Example



10 Initialization flow

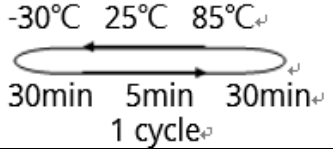


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

11 Example Initialization Code

```
void Write_Data(unsigned char dat)
{
        RS=1;
        CS=0;
         _RW=0;
        DATA_BUS=dat;
        Delayms(2);
         _RW=1;
        CS=1;
 }
 ----------------------------------------------------------------------------------------------------------------
 void Write_Instruction(unsigned char cmd)
 {
        RS=0;
        CS=0;
         _RW=0;
        DATA_BUS=cmd;
        Delayms(2);
        _RW=1;
        CS=1;
 }
 ----------------------------------------------------------------------------------------------------------------
void LCD_initialize(void)
{
      RES=1;  Delayms(200);
       RES=0;  Delayms(200);
       RES=1;  Delayms(200);
    Write_Instruction(0xFD);       /*SET COMMAND LOCK */
      Write_Data(0x12);               /* UNLOCK  */
      Write_Instruction(0xAE);       /*DISPLAY OFF*/
      Write_Instruction(0xB3);       /*DISPLAYDIVIDE CLOCKRADIO/OSCILLATAR FREQUANCY*/
      Write_Data(0x91);
    Write_Instruction(0xCA);   /*multiplex ratio*/
      Write_Data(0x3F);               /*duty = 1/64*/
      Write_Instruction(0xA2);       /*set offset*/
      Write_Data(0x00);
      Write_Instruction(0xA1);       /*start line*/
      Write_Data(0x00);
      Write_Instruction(0xA0);       /*set remap*/
      Write_Data(0x14);     Write_Data(0x11);
      Write_Instruction(0xAB);       /*funtion selection*/
      Write_Data(0x01);               /* selection external vdd */
      Write_Instruction(0xB4);
      Write_Data(0xA0);     Write_Data(0xFD);
      Write_Instruction(0xC1);        /*set contrast current */
      Write_Data(Contrast_level);
      Write_Instruction(0xC7);       /*master contrast current control*/
      Write_Data(0x0F);
      Wriite_Instruction(0xB1);       /*SET PHASE LENGTH*/
      Write_Data(0xE2);
      Write_Instruction(0xD1);
      Write_Data(0x82);     Write_Data(0x20);
      Write_Instruction(0xBB);       /*SET PRE-CHANGE VOLTAGE*/
      Write_Data(0x1F);
      Write_Instruction(0xB6);       /*SET SECOND PRE-CHARGE PERIOD*/
      Write_Data(0x08);
      Write_Instruction(0xBE);       /* SET VCOMH */
      Write_Data(0x07);
      Write_Instruction(0xA6);       /*normal display*/
      Clear_ram();
      Write_Instruction(0xAF);       /*display ON*/
}
```

12 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 ℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation  	-30℃/85℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: The packing have to including into the vibration testing.

13 Warranty and Conditions

http://www.displaymodule.com/pages/faq