DisplayModule

DM-OLED312-669

3.12" 256 x 64 Monochrome Graphic OLED - SPI

Contents

1 Revision History

Date	Changes
2022-08-18	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	3.12	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome with 16 Gray Scales (White)	Colors
Resolution	256 × 64	pixel
Controller IC	SSD1362	-
Interface	4-wire SPI	-
Active Area	76.78 × 19.18	mm
Module Dimension	100.0× 33.0 × 5.4	mm
Pixel Size	86.9 × 25.8 × 2.0	mm
Pixel Pitch	0.3 × 0.3	mm
Drive Duty	1/64 Duty	-
Weight	TBD± 10%	g

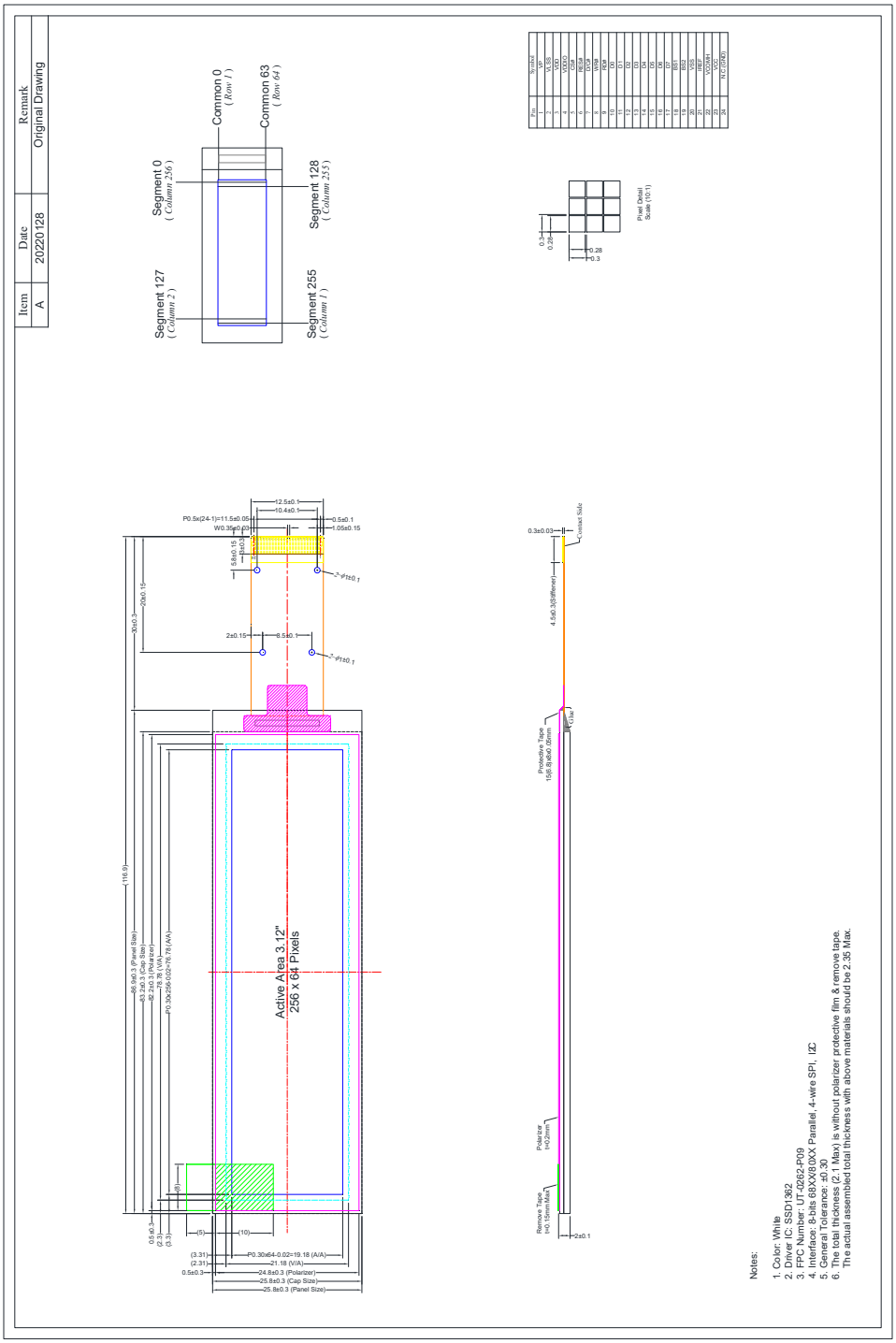
3 Pin Description

3.1 Panel Pin Description

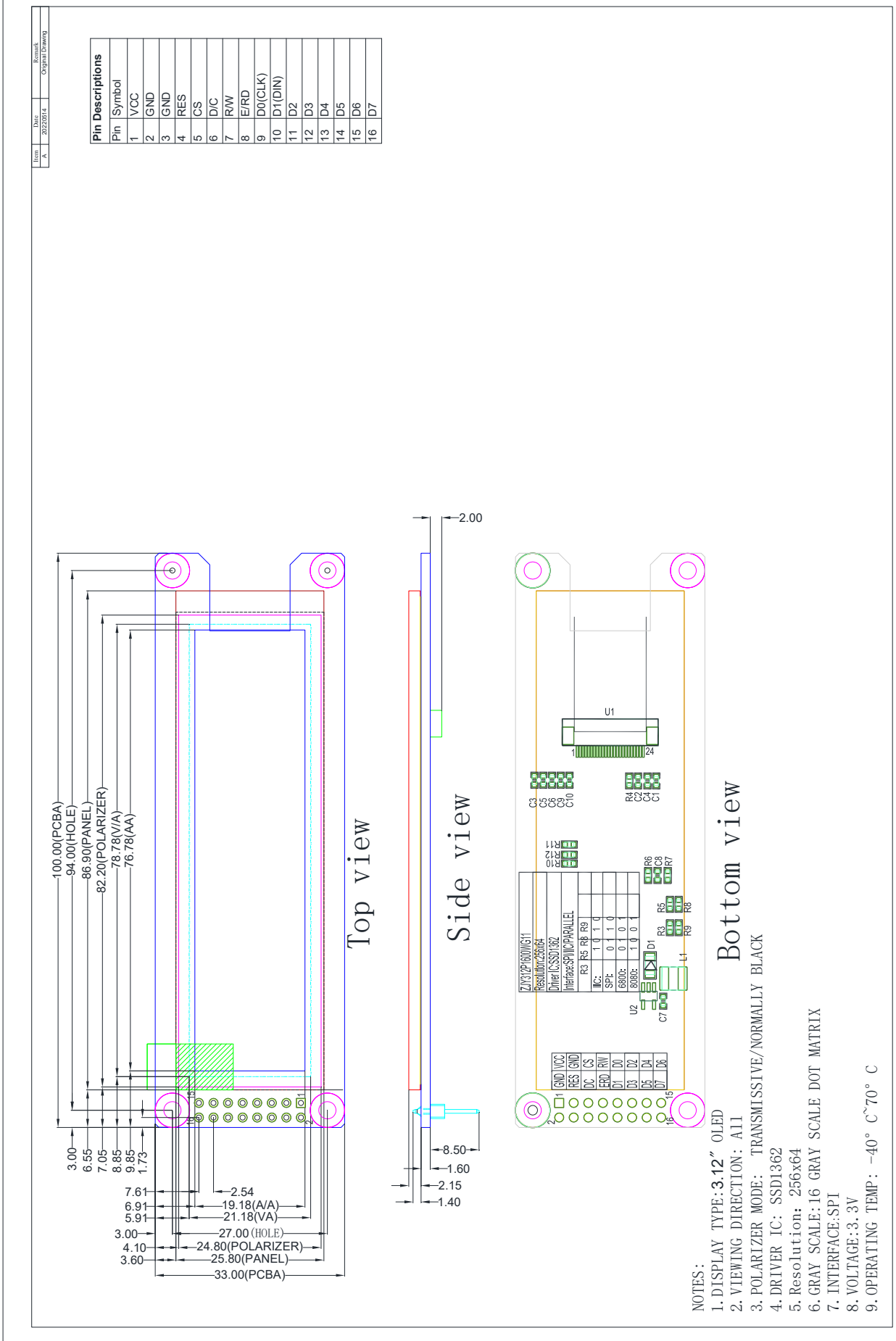
Pin No.	Symbol	Function Description
1,13	VCC	Power Supply for OLED This is a voltage supply pin. It must be connected to source
2	GND	Ground of Logic Circuit This is a ground pin. It must be connected to ground
3	GND	Ground of Logic Circuit This is a ground pin. It must be connected to ground
4	RES	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation
5	CS	Chip Select This pin is the chip select pin.Low enable, high disable.
6	DC	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at SDA is treated as display data. When the pin is pulled low, the input at SDA will be transferred to the command register.
7	R/W	Serves as a read signal and MCU read data at the rising edge.
8	E/RD	Serves as a write signal and MCU write data at the rising edge.
9-16	D0-D7	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Conditions
View Angles		-	Free	-	degree	-
C.I.E(White)	(x) (y)	0.25 0.29	0.29 0.33	0.33 0.37	-	CIE 1931
Brightness	L_{br}	80	100	-	cd/m²	Note 7
Dark Room Contrast	CR	-	>10000:1	-	-	

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Logic Supply Voltage	V_{DD}	3	3.5	V	Note1,2
Operating Temperature	TOP	-40	70	℃	Note3
Storage Temperature	TSTG	-40	85	℃	Note3
Life Time (100 cd/m^2)		TBD	-	hour	Note4

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the

module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

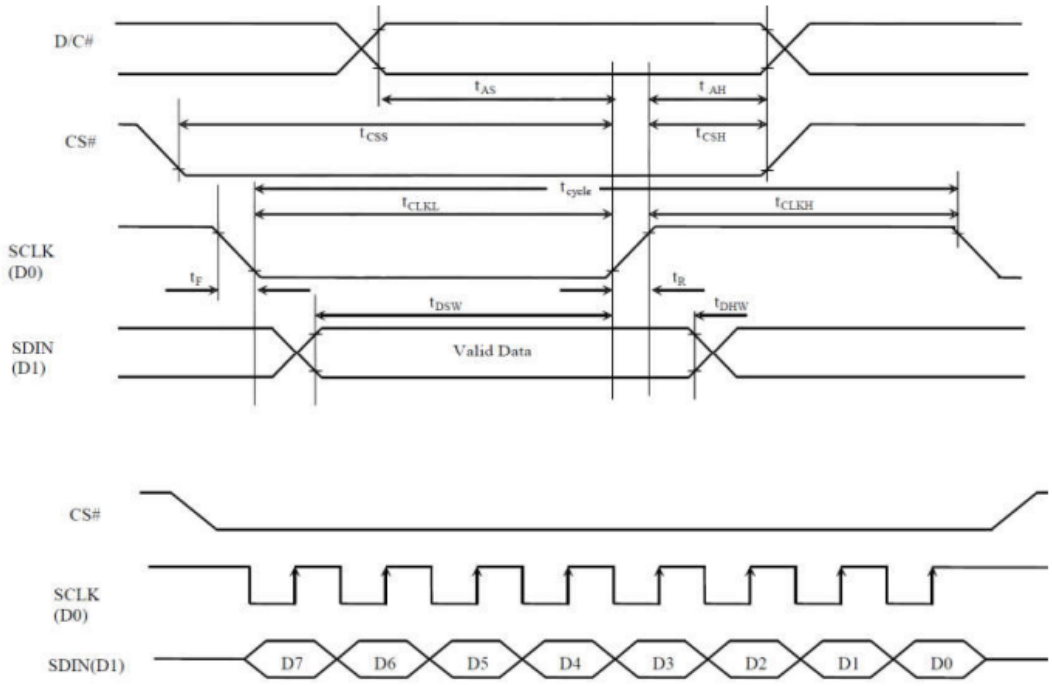
Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood

5.3 AC Characteristics

5.3.1 Serial Interface Timing Characteristics:4-wire SPI

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	40	-	ns
T_{DSW}	Write Data Setup Time	15	-	ns
T_{DHW}	Write Data Hold Time	30	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{CLKL}	Clock Low Time	25	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} -V_{SS} = 1.65V to 3.5V, T_A = 25℃)


D/C#
CS#
SCLK
(D0)
SDIN
(D1)
tAS
tAH
tCSS
tCSH
tcycle
tCLKL
tCLKH
tF
tR
tDSW
tDHW
Valid Data
CS#
SCLK
(D0)
SDIN(D1)
D7
D6
D5
D4
D3
D2
D1
D0

5.3.2 MCU I2C Interface

The I2 C communication interface consists of slave address bit SA0, I2 C-bus data signal SDA (SDAOUT/D2 for output and SDAIN/D1 for input) and I2 C-bus clock signal SCL (D0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

• Slave address bit (SA0) SSD1362 has to recognize the slave address before transmitting or receiving any information by the I2 C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

b7 b6 b5 b4 b3 b2 b1 b0

0 1 1 1 1 0 SA0 R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, can be selected as the slave address of SSD1362. D/C# pin acts as SA0 for slave address selection. “R/W#” bit is used to determine the operation mode of the I2 C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

• I2 C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.

“SDAIN” and “SDAOUT” are tied together and serve as SDA. The “SDAIN” pin must be connected to act as SDA. The “SDAOUT” pin may be disconnected. When “SDAOUT” pin is disconnected, the acknowledgement signal will be ignored in the I2 C-bus.

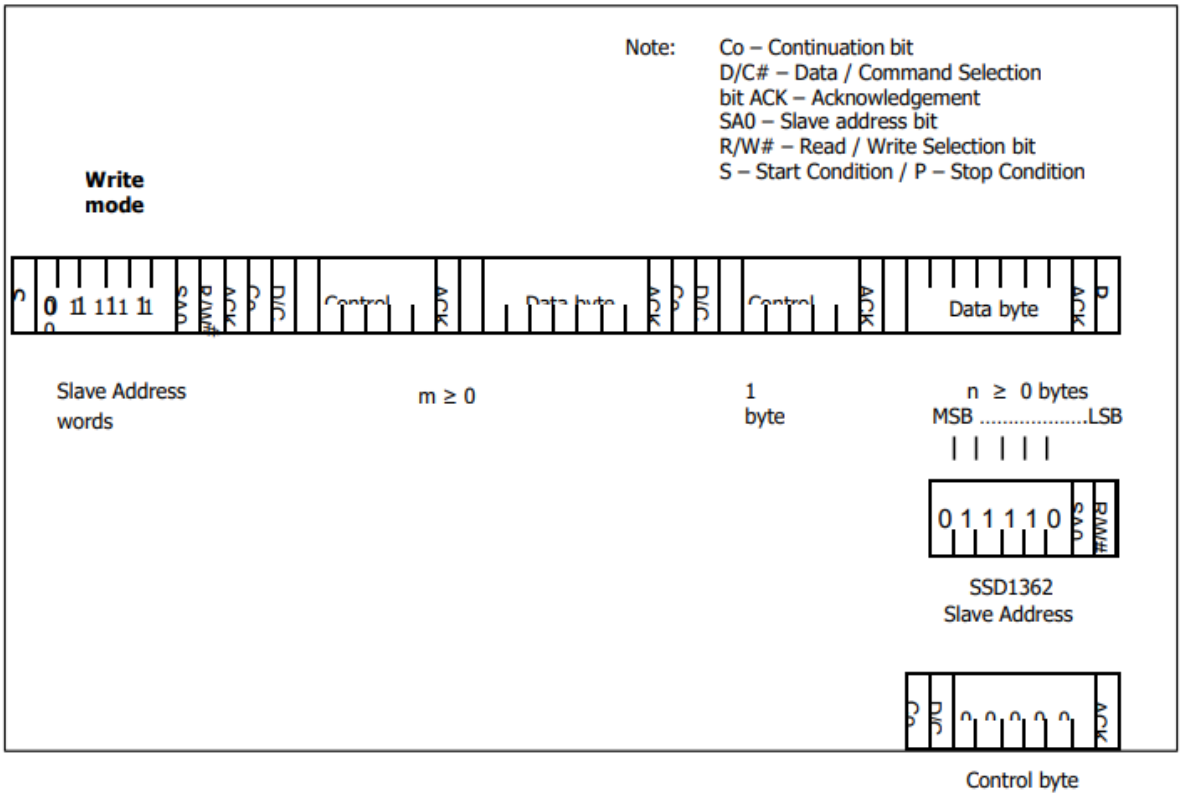
• I2 C-bus clock signal (SCL)

The transmission of information in the I2 C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

5.3.3 I2C-bus Write data

The I2 C-bus interface gives access to write data and command into the device. Please refer to Figure 7-7 for the write mode of I2 C-bus in chronological order.

Figure 7-7 : I2C-bus data format



• Write mode for I2C

• The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.

• The slave address is following the start condition for recognition use. For the SSD1362, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).

• The write mode is established by setting the R/W# bit to logic “0”.

• An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.

• After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0”’s.

• If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.

• The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.

• Acknowledge bit will be generated after receiving each control byte or data byte.

• The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure : Definition of the Start and Stop Condition

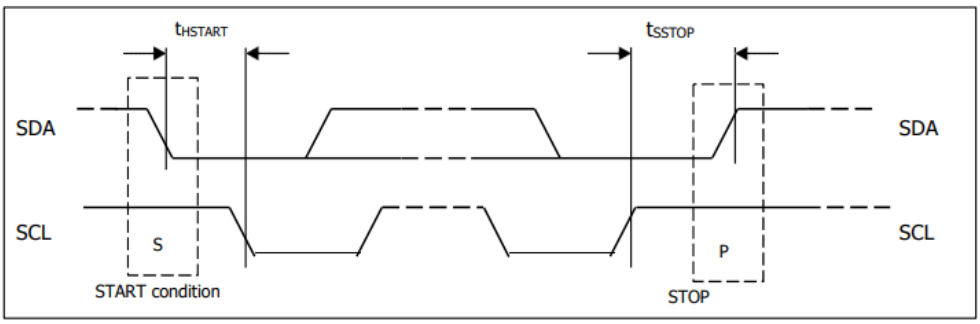
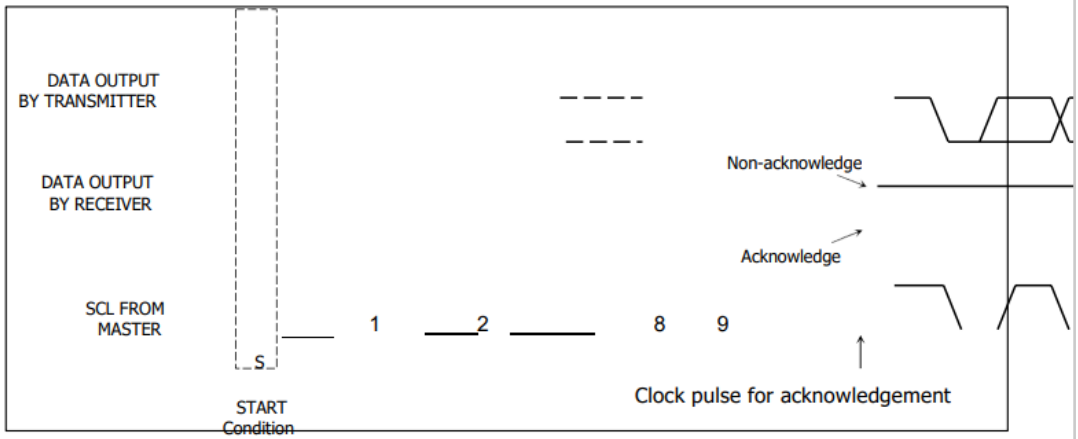


Figure 7-9 : Definition of the acknowledgement condition

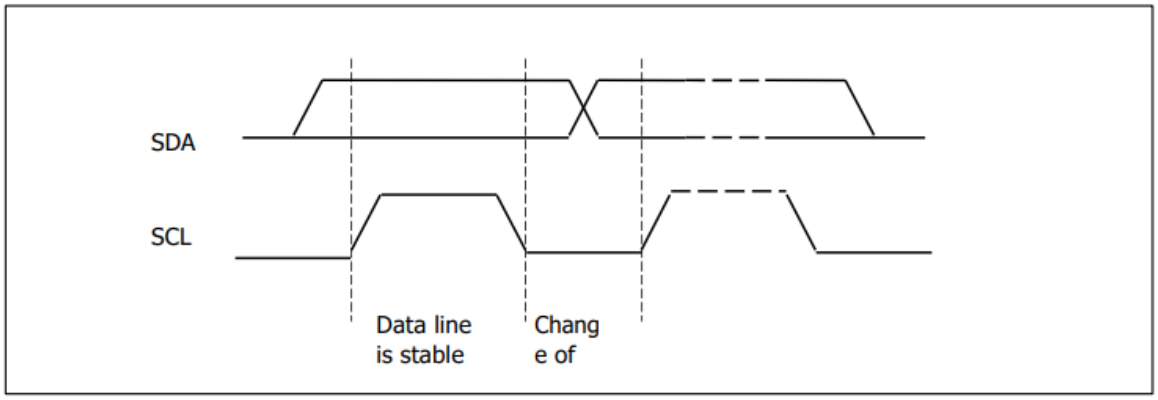


Please be noted that the transmission of the data bit has some limitations.

2. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “HIGH” period of the clock pulse. Please refer to the Figure 7-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.

3. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 7-10 : Definition of the data transfer condition

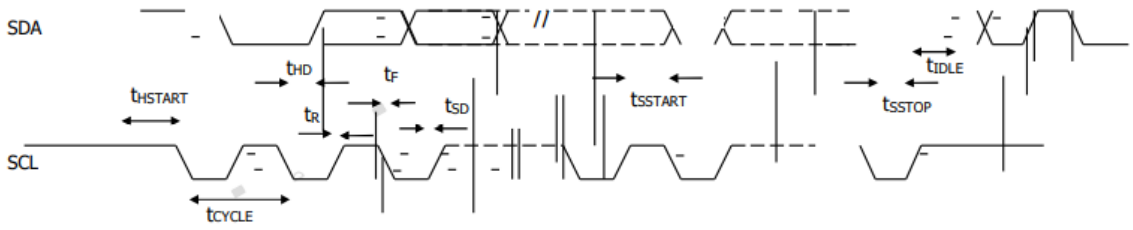


- **I2C Timing Characteristics**

(V_{CI} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Uni
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 12-5: I2C interface Timing



MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write. A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2 : Example of Write procedure in 8080 parallel interface mode

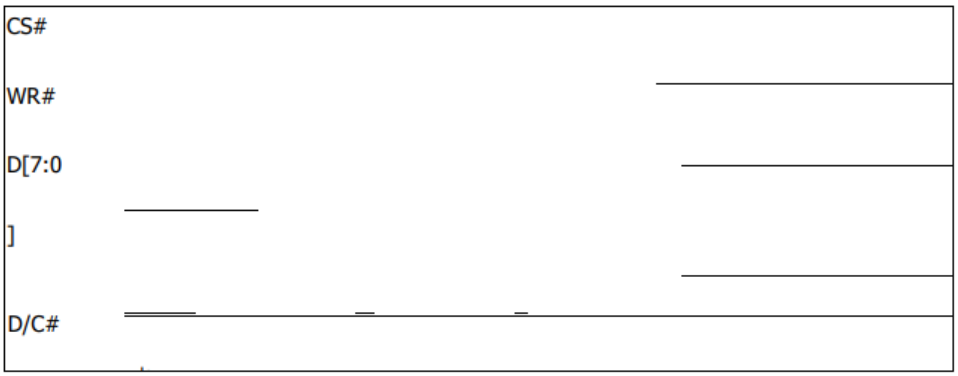


Figure 7-3 : Example of Read procedure in 8080 parallel interface mode

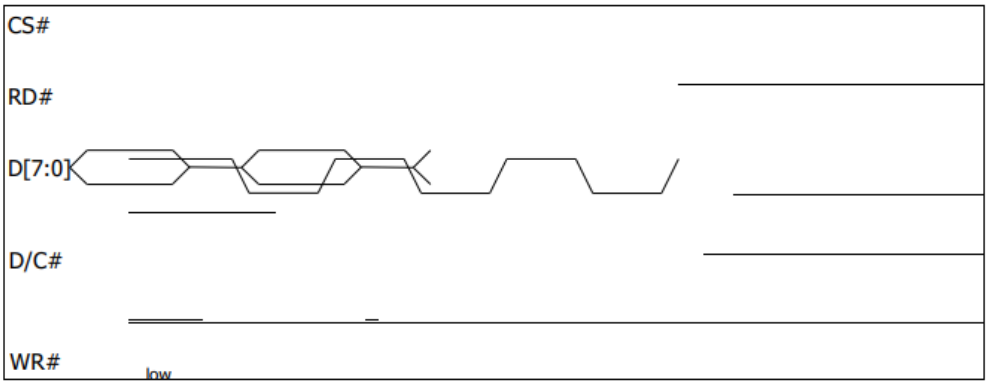


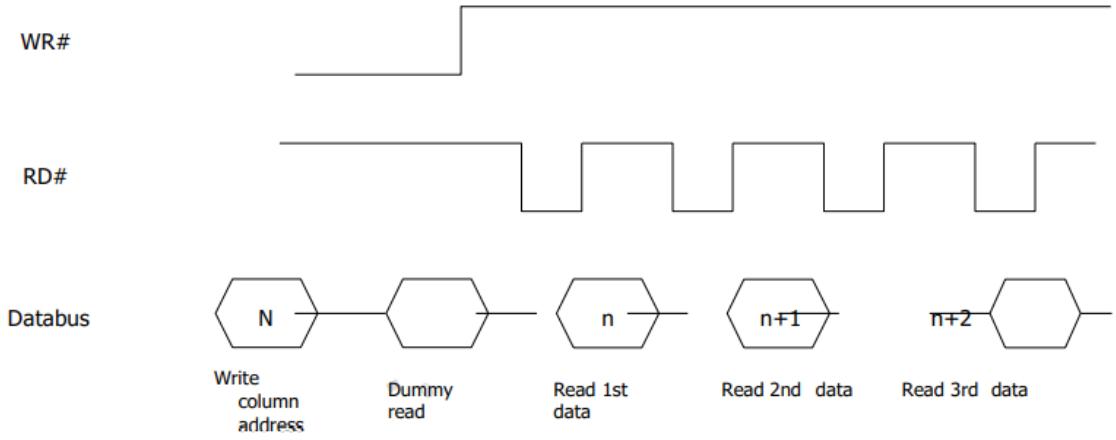
Table 7-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4 : Display data read back procedure - insertion of dummy read



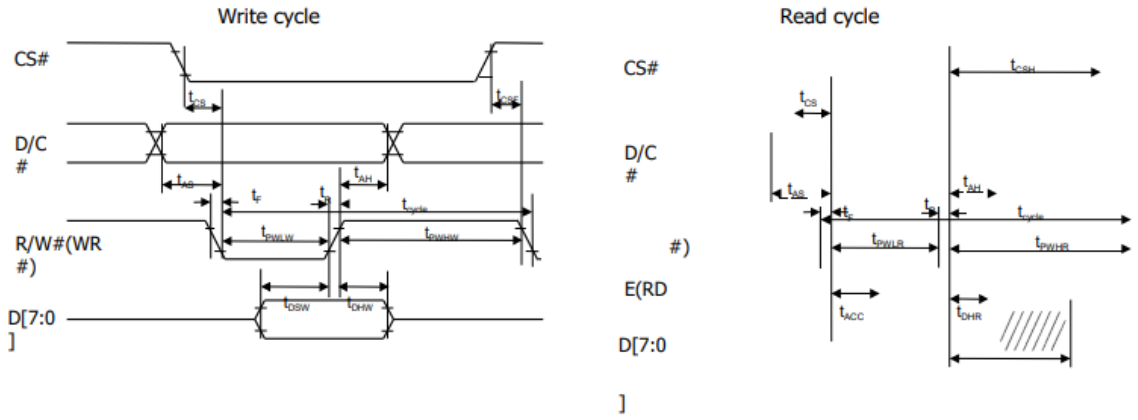
• 8080-Series MCU Parallel Interface Timing Characteristics

Table: 8080-Series MCU Parallel Interface Timing Characteristics

V_{CI} - V_{SS} = 1.65V to 3.5V (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Uni
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	30	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure : 8080-series MCU parallel interface characteristics



6 Functional Specification

6.1 Commands

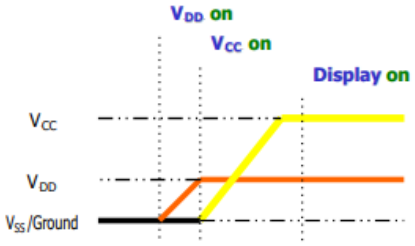
Refer to the Technical Manual for the SSD1362.

6.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

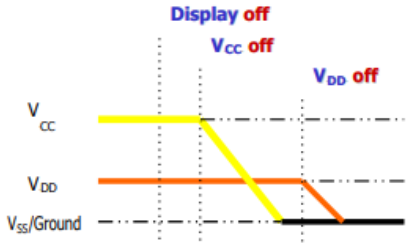
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 8:

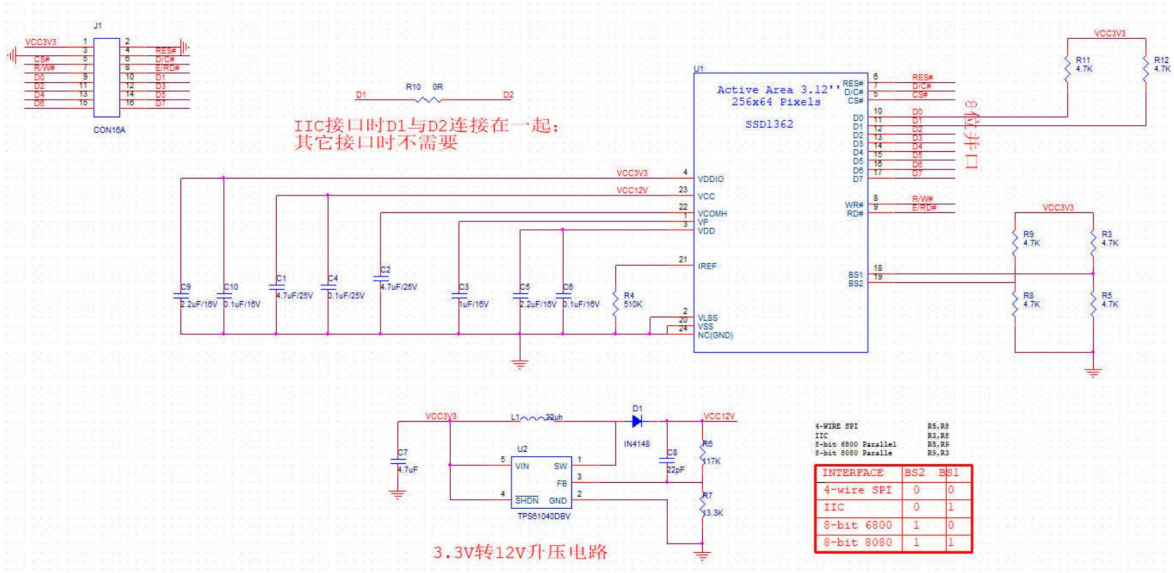
1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

6.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

2. Display is OFF
3. 256×64 Display Mode
4. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
5. Shift register data clear in serial interface
6. Display start line is set at display RAM address 0
7. Column address counter is set at 0
8. Normal scan direction of the COM outputs
9. Contrast control register is set at 7Fh
10. Normal display mode (Equivalent to A4h command)

6.4 Application circuit (VCC>3V)



Module Schematic

7 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	70℃ 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40℃ 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85℃ 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40℃ 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 120hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-40℃/85℃ 24cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

8 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"