DisplayModule

DM-OLED28-643

2.8" 256 × 64 MONOCHROME GRAPHIC OLED DISPLAY MOUDULE - SPI

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1 Revision History

Date	Changes
2019-05-29	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	2.8	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome (16 Gray Scale）	Colors
Resolution	256 x 64	pixel
Controller IC	SSD1322	-
Interface	4wire SPI	-
Active Area	69.10 x 17.26	mm
Module Dimension	84.00 x 45.80 x 2.00	mm
Pixel Pitch	0.27 x 0.27	mm
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

Pin No.	Symbol	Function Description
1	N.C. (GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins.These pins must be connected to external ground as the ESD protection circuit.
2	VSS	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3	VCC	Power Supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.
4	VCOMH	Voltage Output High Level for COM Signal This pin is the input for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to V_{SS} externally.
6-13	D7~D0	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to V_{SS} except for D2 in serial mode.
14	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to V_{SS}.
15	R/W#	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to V_{SS}.
16	BS0	Communicating Protocol Select These pins are MCU interface selection input. See the following table:
17	BS1	

	BS0	BS1
3-wire Serial	1	0
4-wire Serial	0	0
8-bit 68XX Parallel	1	1
8-bit 80XX Parallel	0	1

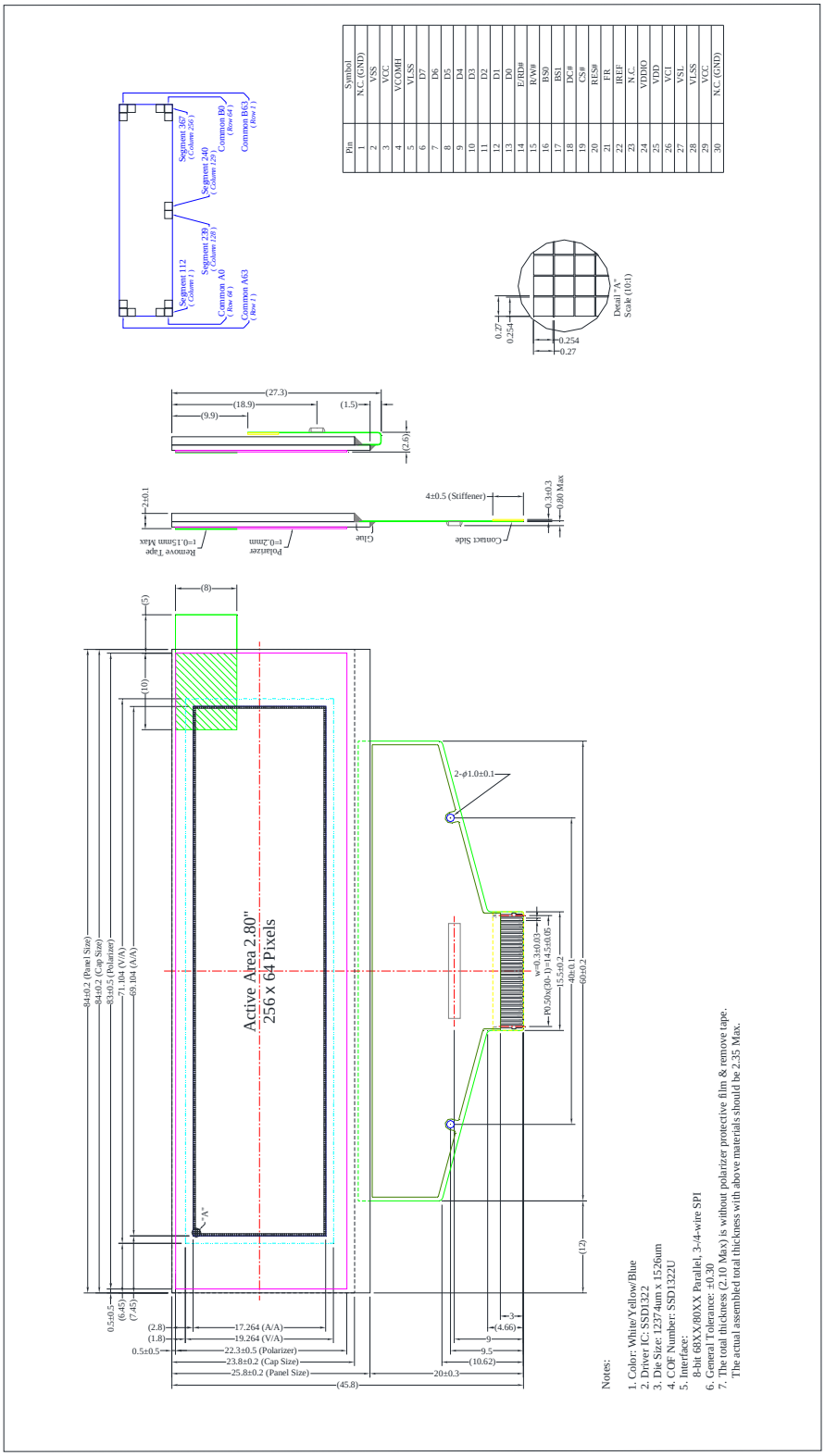
18	D/C#	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. When 3-wire serial mode is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
19	CS#	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
20	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
21	FR	Frame Frequency Triggering Signal This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.
22	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 10µA maximum.
23	N.C.	Reserved Pin The N.C. pin between function pins is reserved for compatible and flexible design.
24	VDDIO	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to V_{CI} or external source. All I/O signal should have V_{IH} reference to V_{DDIO}. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to V_{DDIO}.
25	VDD	Power Supply for Core Logic Circuit This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from V_{CI}. A capacitor should be connected between this pin & V_{SS} under all circumstances.
26	VCI	Power Supply for Operation This is a voltage supply pin. It must be connected to external source & always be equal to or higher than V_{DD} & V_{DDIO}.
27	VSL	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external V_{SL} is not used, this pin should be left open. When external V_{SL} is used, this pin should connect with resistor and diode to ground.
28	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to V_{SS} externally.
29	VCC	Power Supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.
30	N.C. (GND)	Reserved Pin (Sspporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

3.2 Module Pin Description

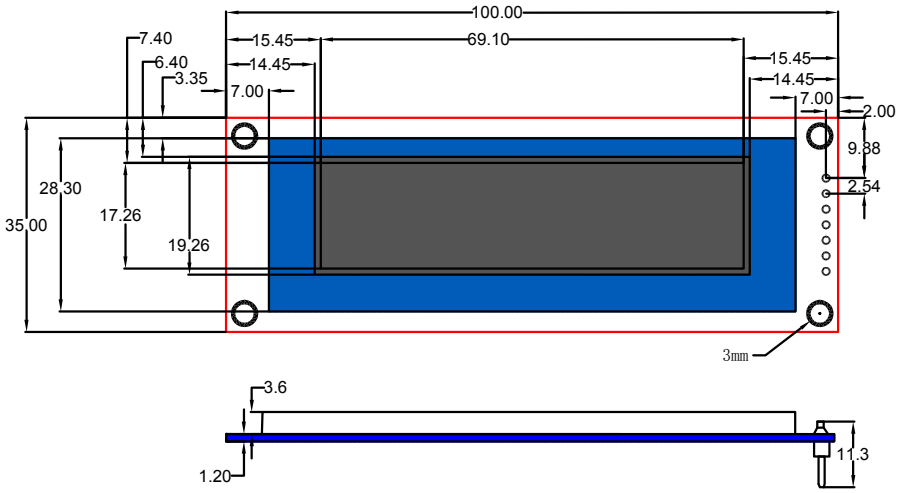
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC_M	Power Supply 3.3V
3	SCL	SPI Clock
4	SDA	SPI DATA
5	RES	OLED reset Pin.
6	D/C	Data/Command Control This pin is Data/Command control pin.
7	CS	Chip Select This pin is pulled low to active. Connect to ground if no used .

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



Resolution : 256*64
Controller IC:SSD1322
Display Colors : White/Yellow/Blue
Gray Scale : 16
Luminance : Supports 128-order adjustable brightness
Communication Interface : 4-wire SPI
Pin definition : From top to bottom is 1 to 7
1.GND
2.VCC_M(3.3V)
3.SCL(SPI Clock)
4.SDA(SPI Data)
5.RES(OLED reset)
6.DC(OLED Data/Commandcontrol pin)
7.CS(SPI Chip Select)

5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles		-	Free	-	°
C.I.E. (White)	(x) (y)	0.25 0.27	0.29 0.31	0.33 0.35	
Brightness	L_{br}	80	100	-	cd/m²
Dark room Contrast Ratio	CR	-	>10,000:1	-	

* Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 12.0V.

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Operation Supply Voltage for panel	V_{CI}	-0.3	4	V	1, 2
Logic Supply Voltage for panel	V_{DD}	-0.5	2.75	V	1, 2
I/O Pins Supply Voltage for panel	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Display Supply Voltage for panel	V_{CC}	-0.5	16	V	1, 2
Display Supply Voltage for module	V_{CC_M}	2.4	3.5	V	-
Operating Current for V_{CC}	I_{CC}	-	60	mA	1, 2
Operating Temperature	T_{OP}	-40	85	℃	3
Storage Temperature	T_{STG}	-40	90	℃	3
Life Time (100 cd/m^2)		15,000	-	hour	4
Life Time (80 cd/m^2)		25,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

Note 4: V_{CC} = 12.0V, Ta = 25℃, 50% Checkerboard.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 DC Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Operation Supply Voltage for panel	V_{CI}		2.4	2.8	3.5	V
Logic Supply Voltage for panel	V_{DD}		2.4	2.5	2.6	V
I/O Pins Supply Voltage for panel	V_{DDIO}		1.65	1.8	V_{CI}	V
Display Supply Voltage for panel	V_{CC}	Note5	11.5	12.0	12.5	V
Display Supply Voltage for module	V_{CC_M}		2.4	3.3	3.5	V
Operating Current V_{CI}	I_{CI}		-	180	300	µA
Operating Current V_{CC}	I_{CC}	Note6	-	15.6	19.5	mA
		Note7	-	26.1	32.7	mA
		Note8	-	44.7	55.9	mA
Sleep Mode Current V_{CI}	$I_{CI,SLEEP}$		-	20	100	µA
Sleep Mode Current V_{DDIO}	$I_{DDIO,SLEEP}$		-	2	10	µA
Low Level Input Voltage	V_{IL}		0	-	0.2 x V_{DDIO}	V
High Level Input Voltage	V_{IH}		0.8 x V_{DDIO}	-	V_{DDIO}	V
Low Level Output Voltage	V_{OL}	I_{out} =100µA	0	-	0.1 x V_{DDIO}	V
High Level Output Voltage	V_{OH}	I_{out} =100µA	0.9 x V_{DDIO}	-	V_{DDIO}	V

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 6: V_{CI} = 2.8V, V_{CC} = 12.0V, 30% Display Area Turn on.

Note 7: V_{CI} = 2.8V, V_{CC} = 12.0V, 50% Display Area Turn on.

Note 8: V_{CI} = 2.8V, V_{CC} = 12.0V, 100% Display Area Turn on.

5.4 AC Characteristics

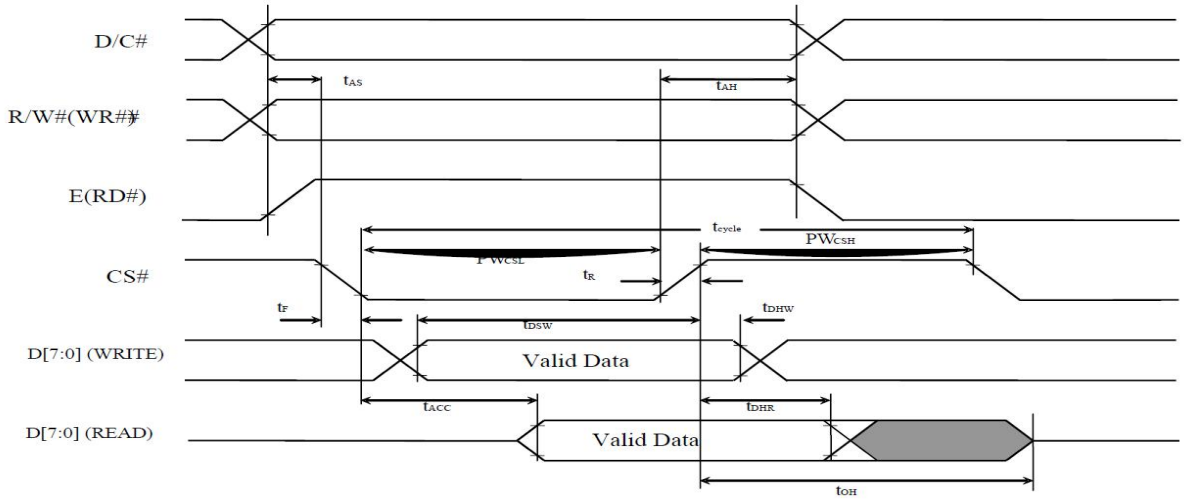
5.4.1 6800-Series MCU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	200	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	450 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	200	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	450 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 2.1V-V_{CI}, V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)



5.4.2 8080-Series MCU Parallel Interface Timing Characteristics:

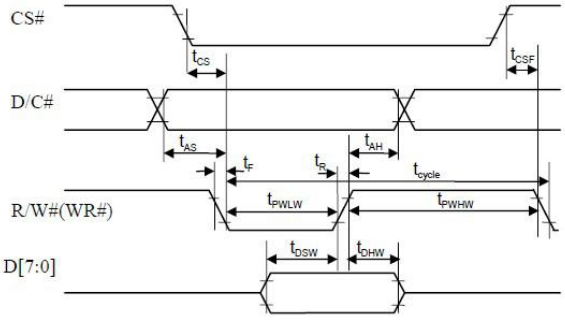
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	200	ns
t_{PWLR}	Read Low Time	200	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)

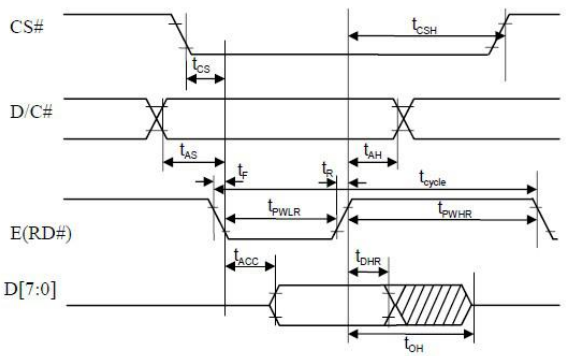
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	10	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	200	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 2.1V-V_{CI}, V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)

Write cycle



Read cycle



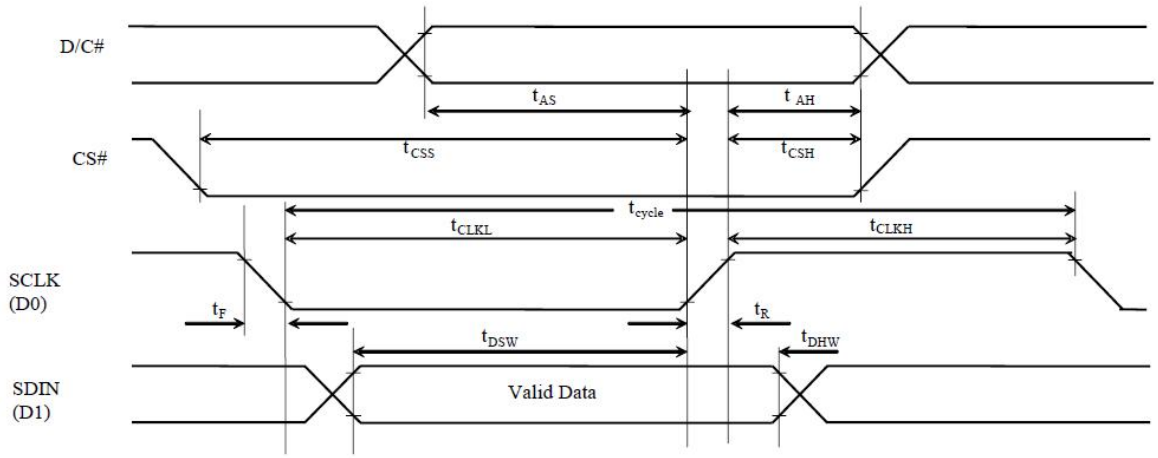
5.4.3 4-wire Serial Interface Timing Characteristics: (default)

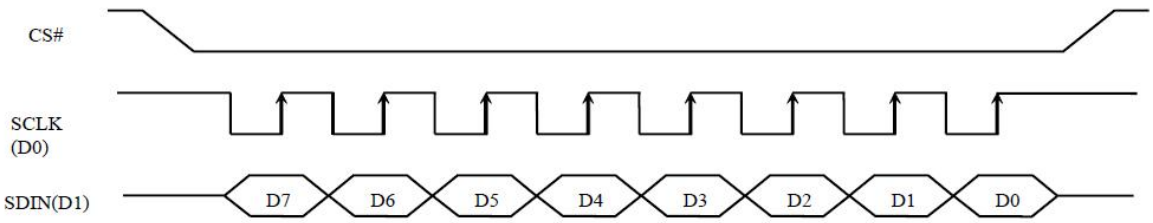
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	35	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	40	-	ns
t_{CLKH}	Clock High Time	40	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	35	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	40	-	ns
t_{CLKH}	Clock High Time	40	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 2.1V-V_{CI} , V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)





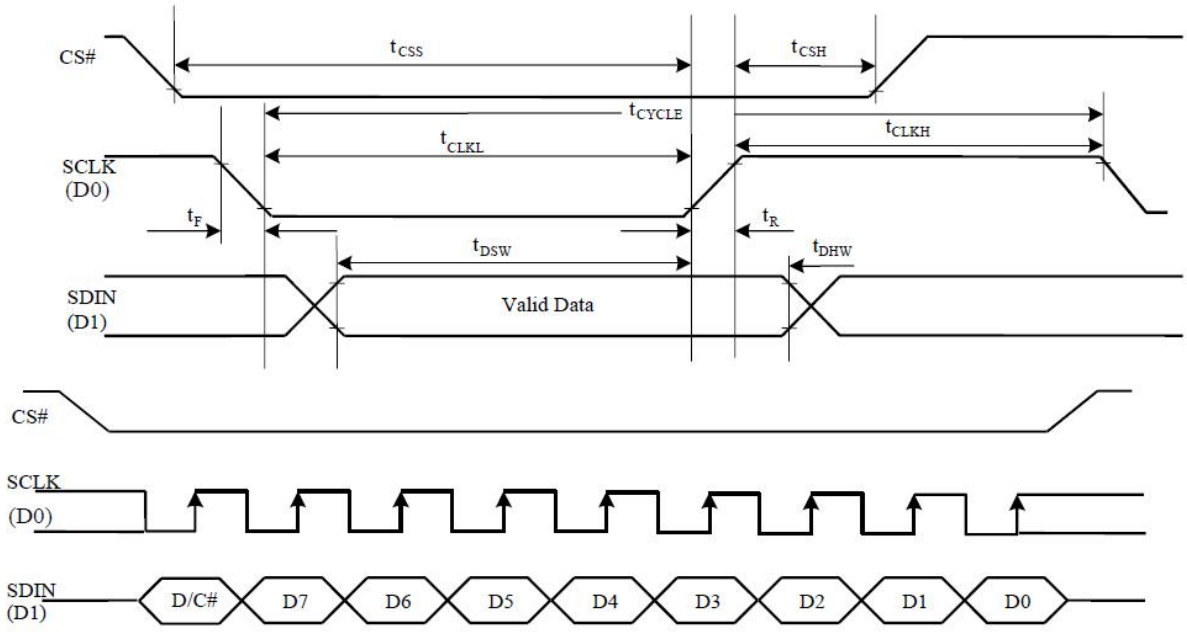
5.4.4 3-wire Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	35	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	40	-	ns
t_{CLKH}	Clock High Time	25	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	25	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	25	-	ns
t_{CLKH}	Clock High Time	25	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} -V_{SS} = 2.1V-V_{CI} , V_{CI} - V_{SS} = 2.4V-3.5V, Ta = 25°C)



6 Functional Specification

6.1 Commands

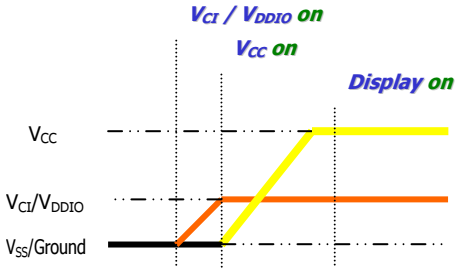
Refer to the Technical Manual for the SSD1322

6.2 Power down and Power up Sequence

To protect OEL paneland extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

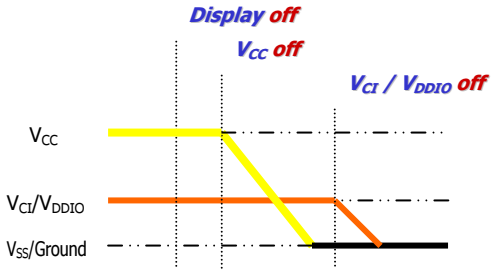
6.2.1 Power up Sequence:

1. Power up V_{CI} / V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 200ms (When V_{CC} is stable)
7. Send Display on command



6.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
4. (When V_{CC} is reach 0 and panel is completely discharges)
5. Power down V_{CI} / V_{DDIO}



Note 9:

1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{CI} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{CI}, V_{DDIO} should not be power down before V_{CC} power down.

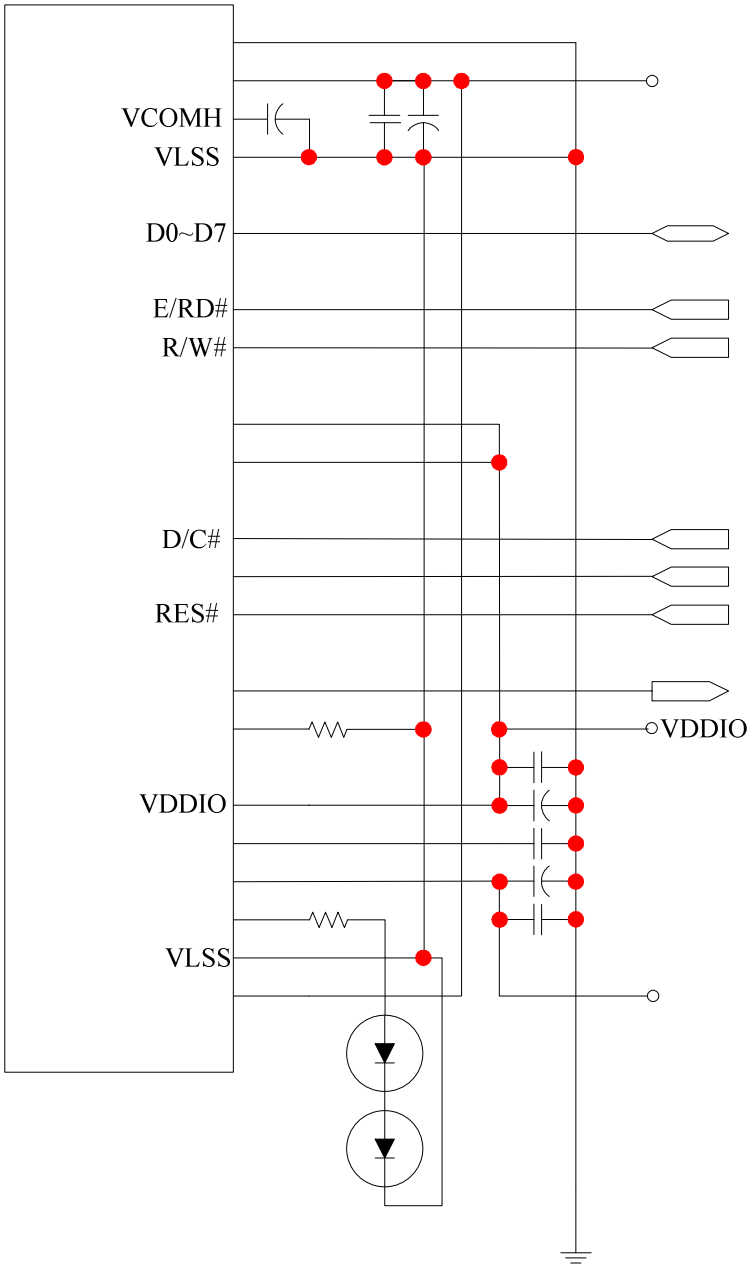
6.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 480 x 128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 7Fh

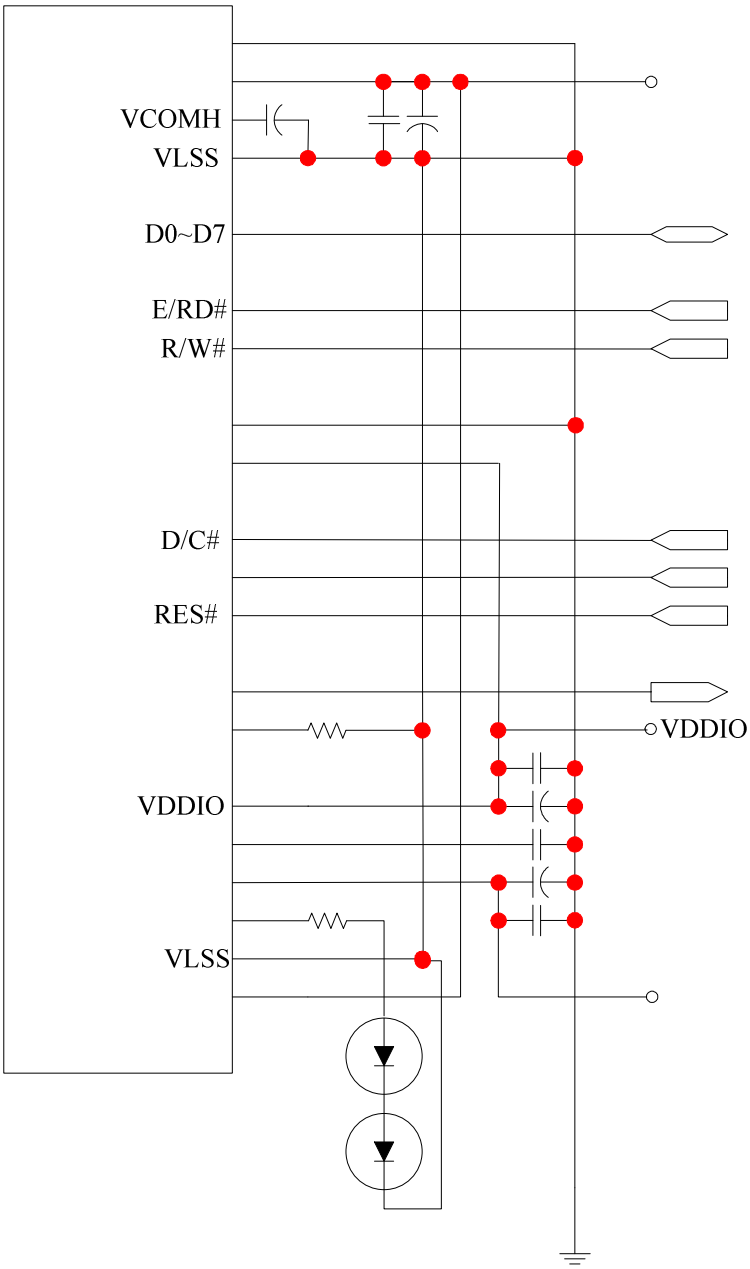
6.4 Application circuit reference

6.4.1 6800-Series MCU Parallel Interface and VCC Supplied Externally



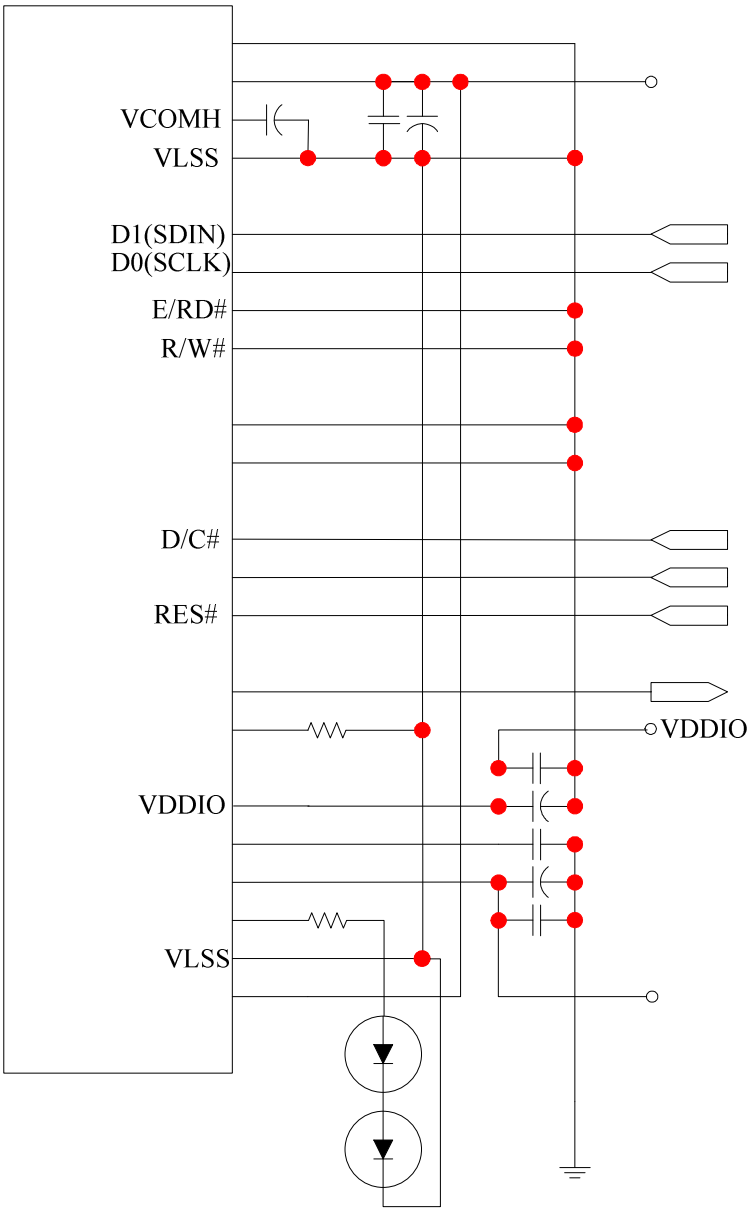
C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680k
R2: 50 , 1/4W
D1,D2: = 0.7V, 1N4148

6.4.2 8080-Series MCU Parallel Interface and VCC Supplied Externally



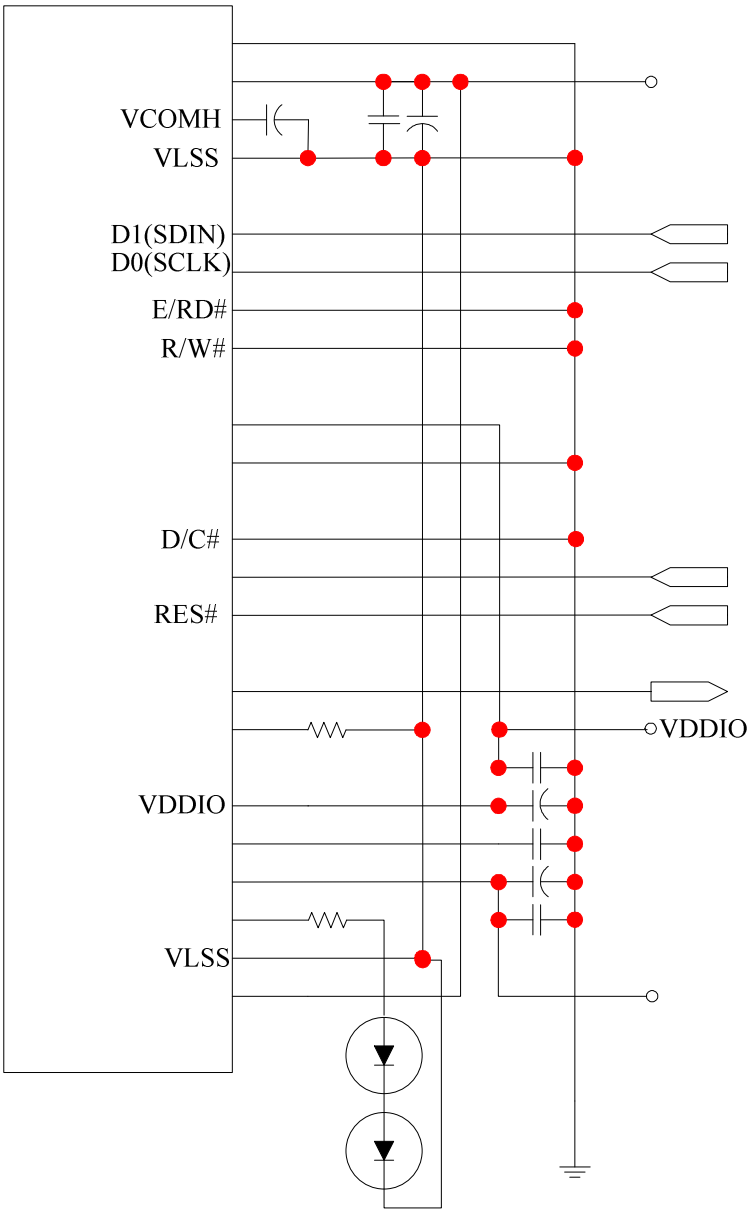
C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680k
R2: 50 , 1/4W
D1,D2: Vth = 0.7V, 1N4148

6.4.3 4wire SPI and VCC Supplied Externally



C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680k
R2: 50 , 1/4W
D1,D2: Vth = 0.7V, 1N4148

6.4.4 3wire SPI and VCC Supplied Externally



C1,C3,C5:0.1uF
C2,C4: 4.7uF
C6: 10uF
C7: 1uF
C8: 4.7uF/25V Tantalum Capacitor
R1: 680k
R2: 50 , 1/4W
D1,D2: Vth = 0.7V, 1N4148

7 Power ON/OFF Timing Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1322 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

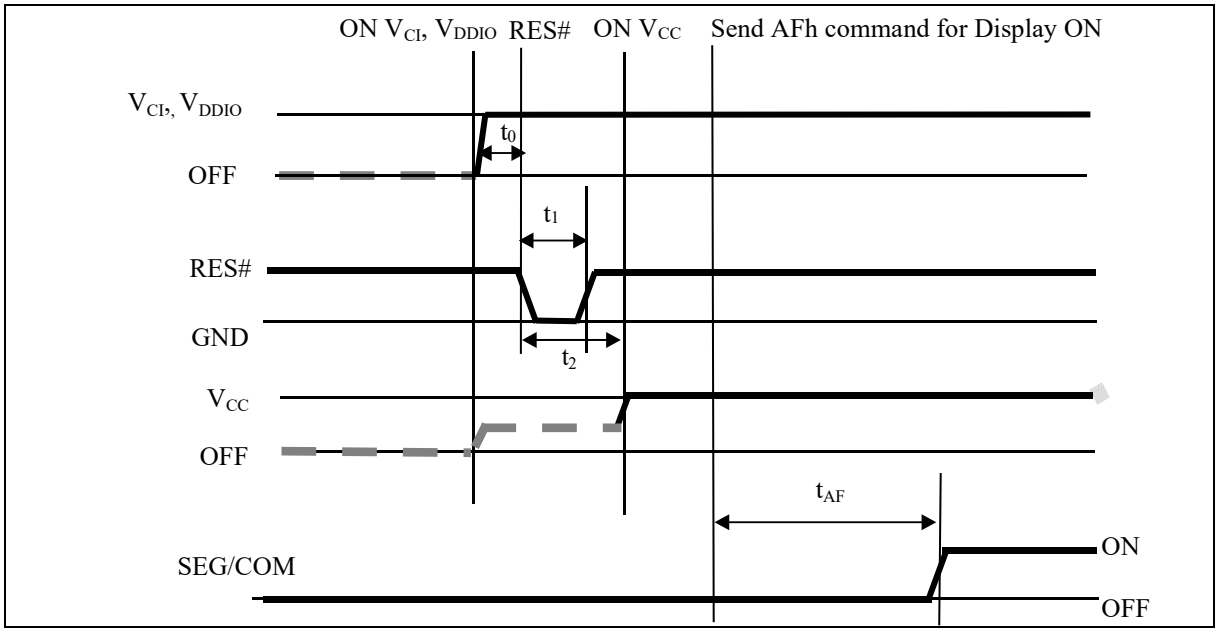
1. Power ON V_{CI},V_{DDIO}.

2. After V_{CI},V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1)(4) and then HIGH (logic high).

3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}. (1)

4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

Figure 7-1 : The Power ON sequence



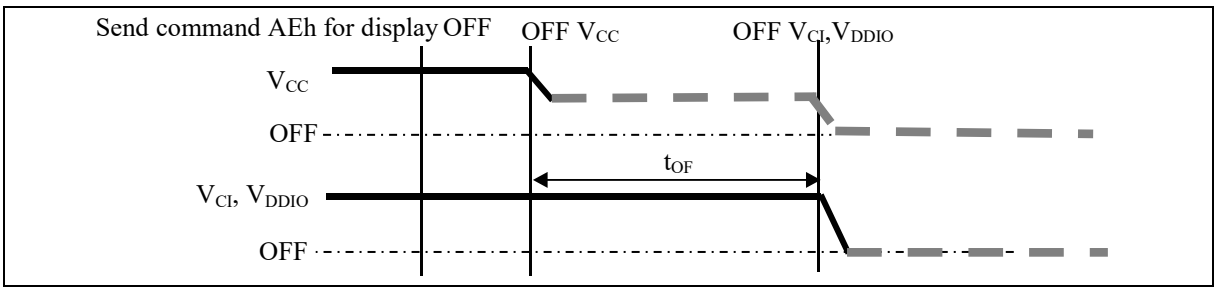
Power OFF sequence:

1. Send command AEh for display OFF.

2. Power OFF V_{CC}.(1), (2)

3. Wait for t_{OFF}. Power OFF V_{CI}, V_{DDIO}. (where Minimum t_{OFF}=0ms(3), Typical t_{OFF}=100ms)

Figure 7-2 : The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-1 and Figure 7-2.

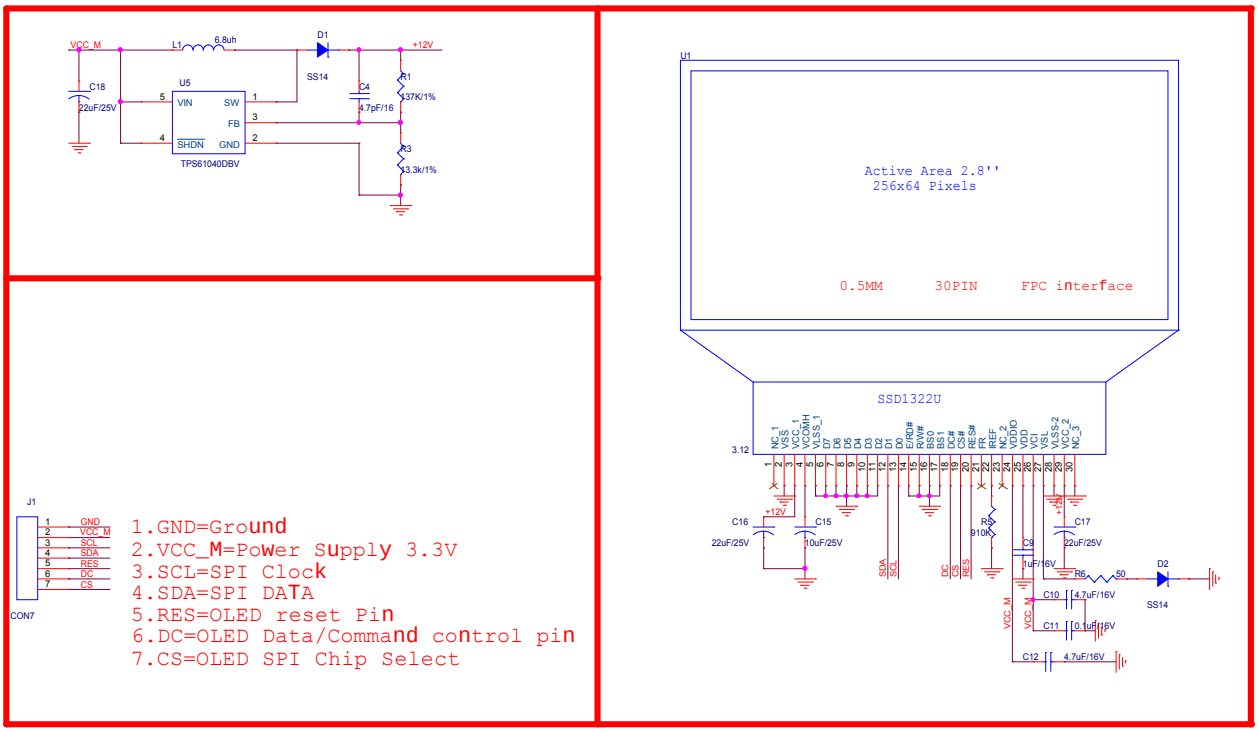
(2) V_{CC} should be kept float (disable) when it is OFF.

(3) V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.

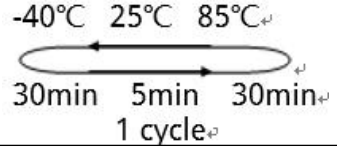
(4) The register values are reset after t1.

(5) Power pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

8 Module Schematic



9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	90°C 500hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 500hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85°C 500hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 °C 500hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 240hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40°C/85°C 100 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"