DisplayModule

DM-OLED223-644

2.8" 128 × 32 MONOCHROME GRAPHIC OLED DISPLAY MOUDULE - SPI

Contents

1 Revision History

Date	Changes
2019-06-03	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	2.23	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome (Blue,Yellow,White)	Colors
Resolution	128 x 32	pixel
Controller IC	SSD1305	-
Interface	4-wire SPI	-
Active Area	55.02 x 13.1	mm
Module Dimension	62.0 x 24.0 x 2.00	mm
Pixel Pitch	0.43 x 0.41	mm
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1</td><td>N.C. (GND)</td><td>Reserved Pin (Sspporting Pin)
The supporting pins can reduce the influences from stresses on the function pins.These pins must be connected to external ground as the ESD protection circuit.</td></tr>
<tr><td>2</td><td>VLSS</td><td>Positive Terminal of the Flying Inverting Capacitor Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>3</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>N.C.</td><td>Reserved Pin
The N.C. pin between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>5</td><td>VDD</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>6</td><td>BS1</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th></tr>
<tr><td>I²C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire Serial</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>8</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>9</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>10</td><td>D/C#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>11</td><td>R/W#</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and</td></tr>
</table>

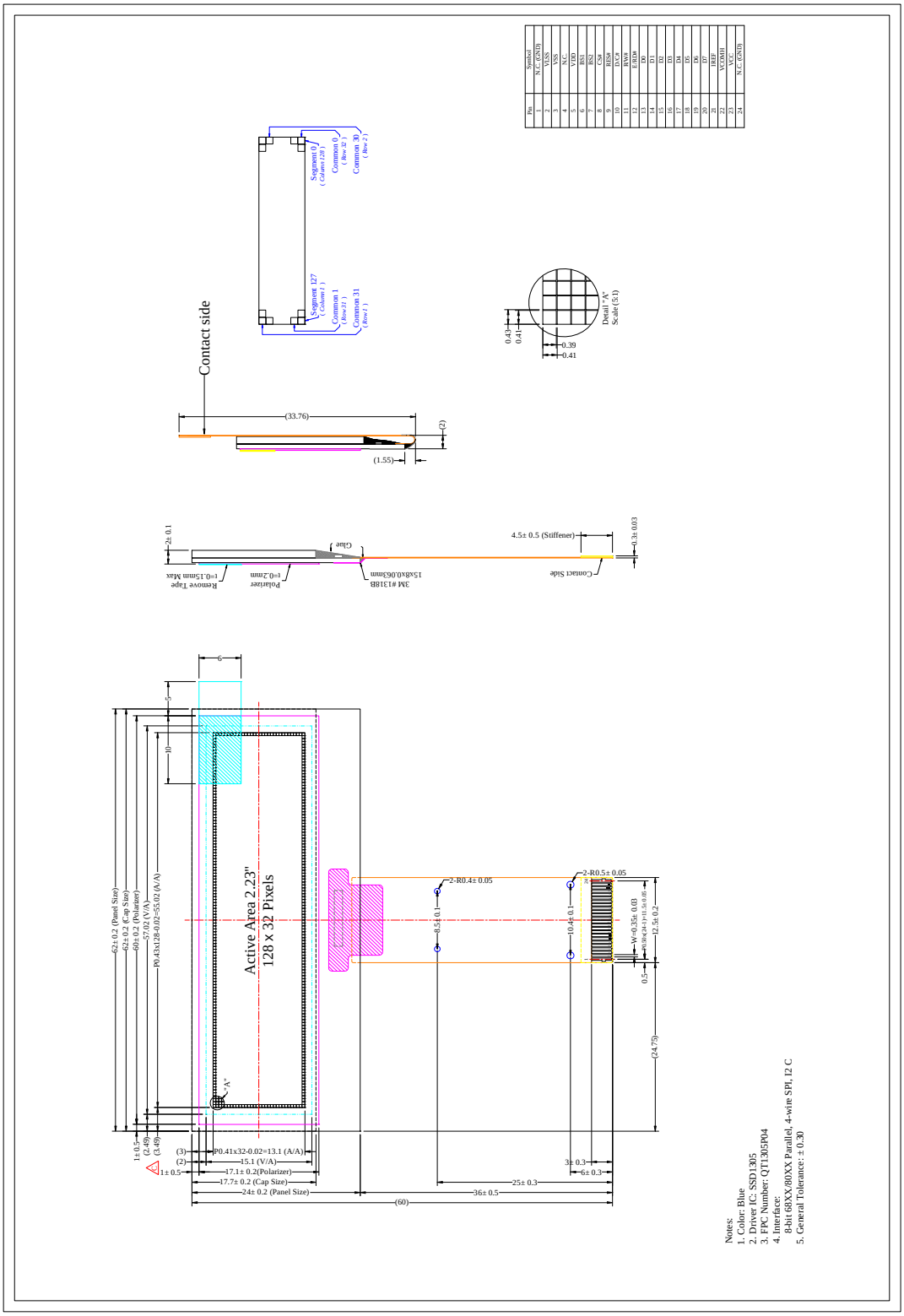
		the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
12	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
13-20	D0~D7	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.
21	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5 A maximum.
22	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
23	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
24	N.C. (GND)	Reserved Pin (Sspporting Pin) The supporting pins can reduce the influences from stresses on the function pins.These pins must be connected to external ground as the ESD protection circuit.

3.2 Module Pin Description

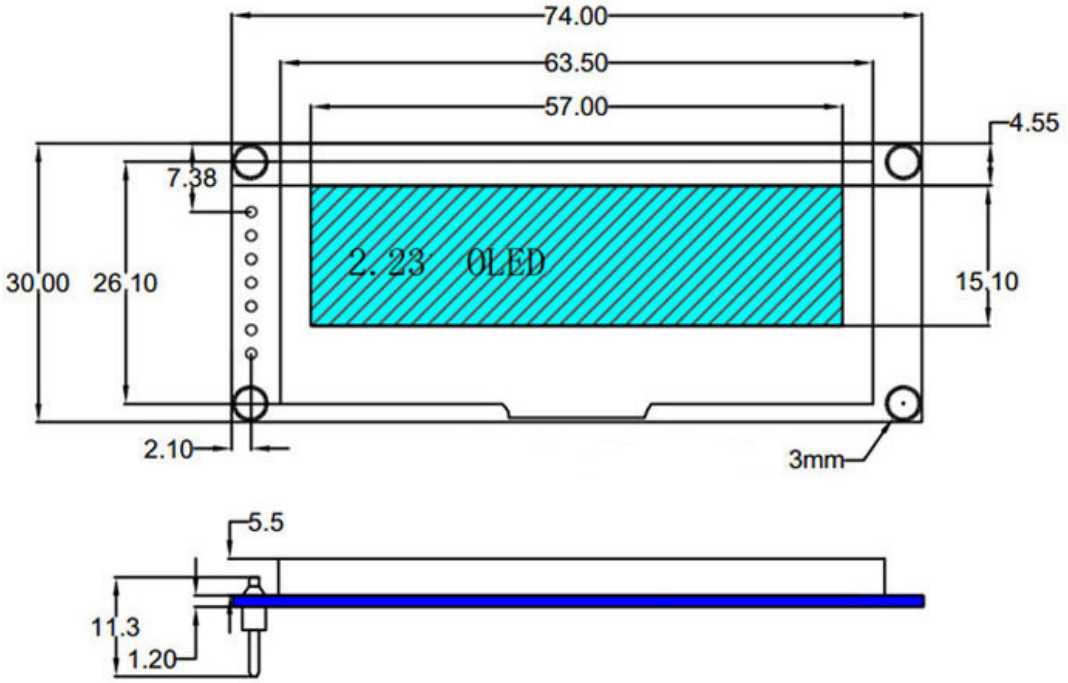
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC_IN	Power Supply 3.3V
3	CLK	This pin is used serial interface in 4-wire 8-bit serial data interface.
4	DIN	Serial input signal. The data is applied on the rising edge of the SCL signal.
5	RES	OLED reset pin. Signal is active low.
6	D/C	Data/Command Control This pin is Data/Command control pin.
7	CS	Chip Select This pin is pulled low to active. Connect to ground if no used .

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
View Angles		-	Free	-	°	
C.I.E.	(x) (y)	0.12 0.22	0.16 0.26	0.20 0.30		C.I.E. 1931
Brightness	L_{br}	100	120	-	cd/m²	5
Dark room Contrast Ratio	CR	-	2000:1	-		

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.0V.

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Logic Supply Voltage for panel	V_{DD}	-0.3	4	V	1, 2
Display Supply Voltage for panel	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	85	℃	
Storage Temperature	T_{STG}	-40	85	℃	3
Life Time (120 cd/m^2)		10,000	-	hour	4
Life Time (80 cd/m^2)		30,000	-	hour	4
Life Time (60 cd/m^2)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

Note 4: V_{CC} = 12.0V, Ta = 25℃, 50% Checkerboard.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 DC Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Logic Supply Voltage for panel	V_{DD}		1.65	2.8	3.3	V
Display Supply Voltage for panel	V_{CC}	Note5	-	12.0	-	V
Display Supply Voltage for module	V_{CC_IN}		-	3.3	-	V
Operating Current V_{DD}	I_{DD}		-	180	300	µA
Operating Current V_{CC}	I_{CC}	Note6	-	18	25	mA
Sleep Mode Current V_{DD}	$I_{DD,SLEEP}$		-	1	5	µA
Sleep Mode Current V_{CC}	$I_{CC,SLEEP}$		-	2	10	µA
Low Level Input Voltage	V_{IL}	I_{out}=100µA, 3.3MHz	0	-	0.2 x V_{DD}	V
High Level Input Voltage	V_{IH}	I_{out}=100µA, 3.3MHz	0.8 x V_{DD}	-	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{out}=100µA, 3.3MHz	0	-	0.1 x V_{DD}	V
High Level Output Voltage	V_{OH}	I_{out}=100µA, 3.3MHz	0.9 x V_{DD}	-	V_{DD}	V

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

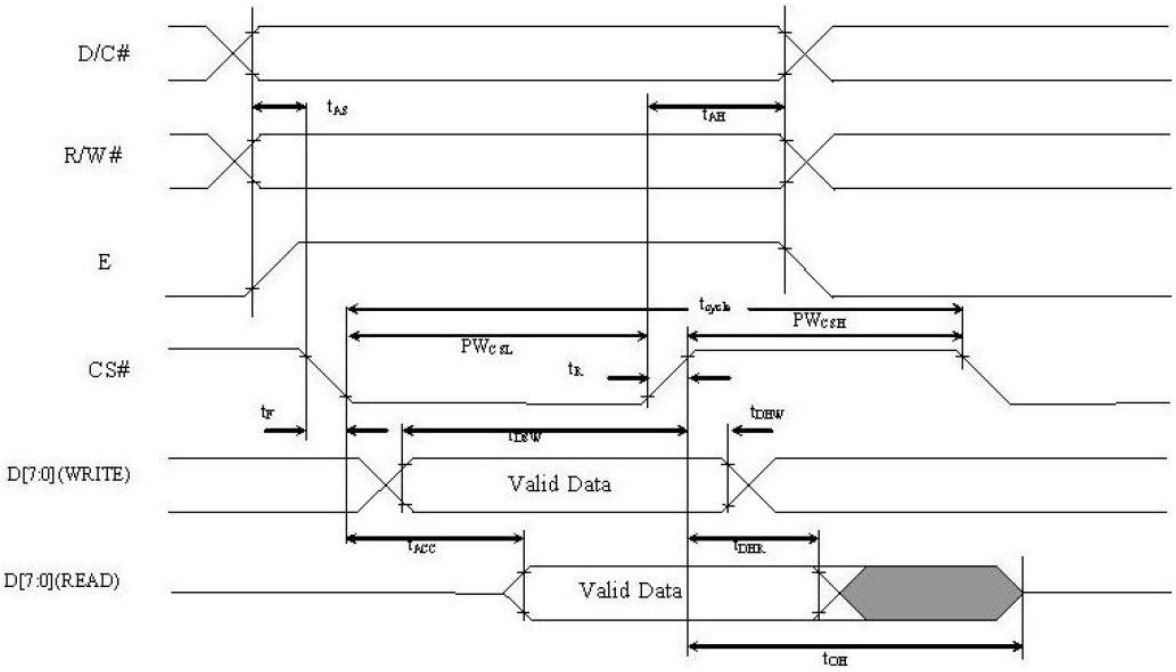
Note 6: V_{DD} = 2.8V, V_{CC} = 12.0V, 100% Display Area Turn on.

5.4 AC Characteristics

5.4.1 68XX-Series MCU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} -V_{SS} = 1.65V to 3.3V, Ta = 25°C)

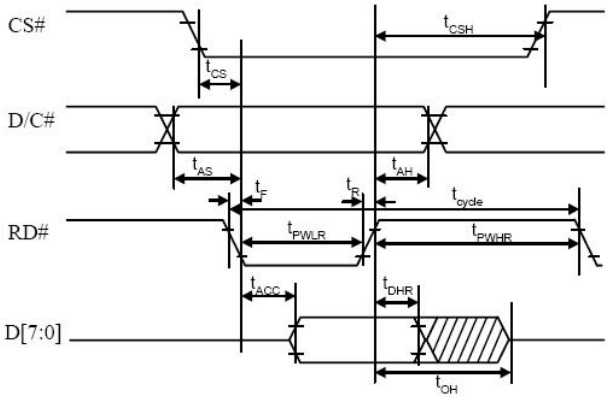


5.4.2 80XX-Series MCU Parallel Interface Timing Characteristics:

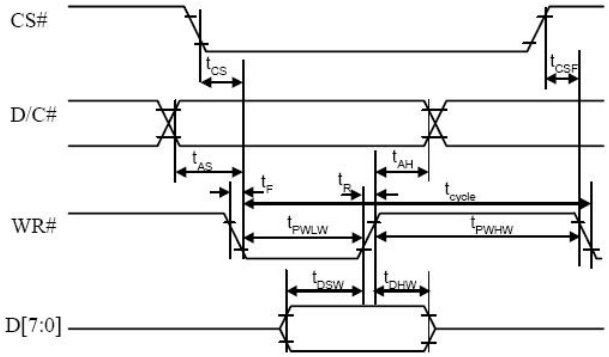
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} -V_{SS} = 1.65 to 3.3V, Ta = 25°C)

(Read Timing)



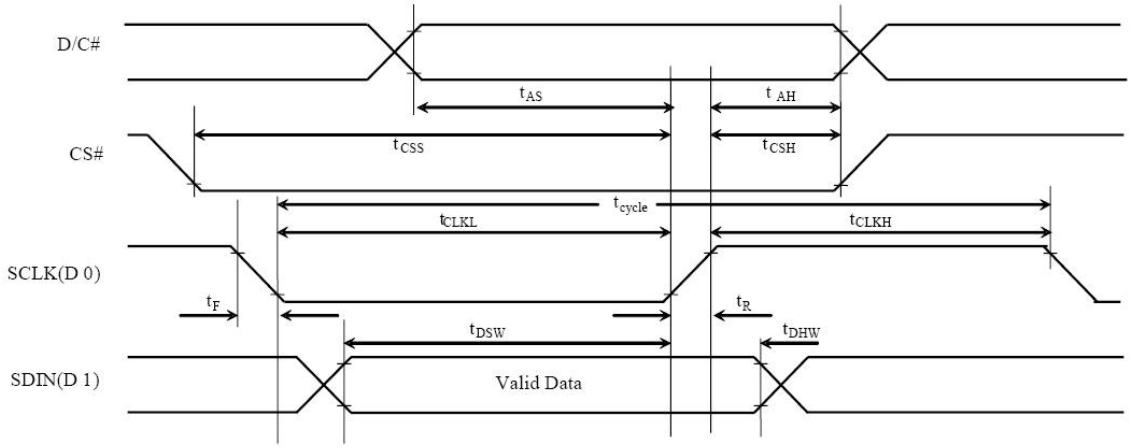
(Write Timing)

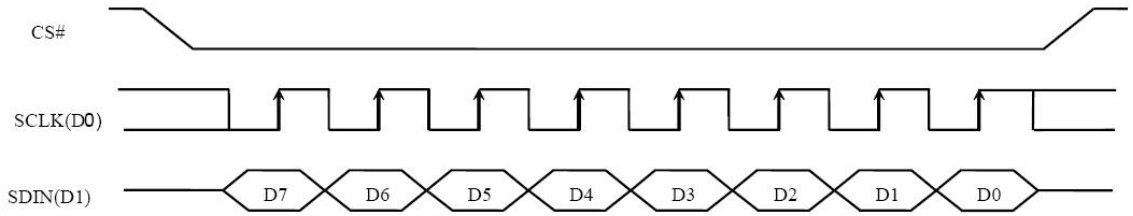


5.4.3 4-wire Serial Interface Timing Characteristics:(default)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	50	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} -V_{SS} = 1.65V to 3.3V, Ta = 25°C)

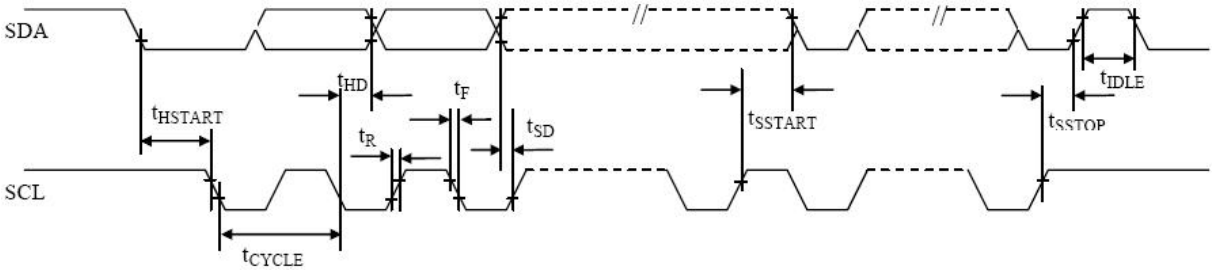




5.4.4 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	35	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	40	-	ns
t_{CLKH}	Clock High Time	25	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDD -VSS = 1.65V to 3.3V, Ta = 25℃)



6 Functional Specification

6.1 Commands

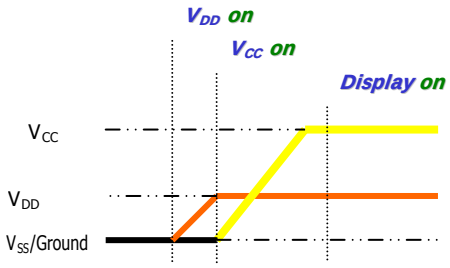
Refer to the Technical Manual for the SSD1305

6.2 Power down and Power up Sequence

To protect OEL paneland extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after theoperation.

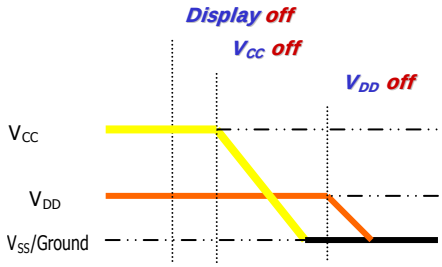
6.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms (When V_{CC} is stable)
7. Send Display on command



6.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
4. (When V_{CC} is reach 0 and panel is completely discharges)
5. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

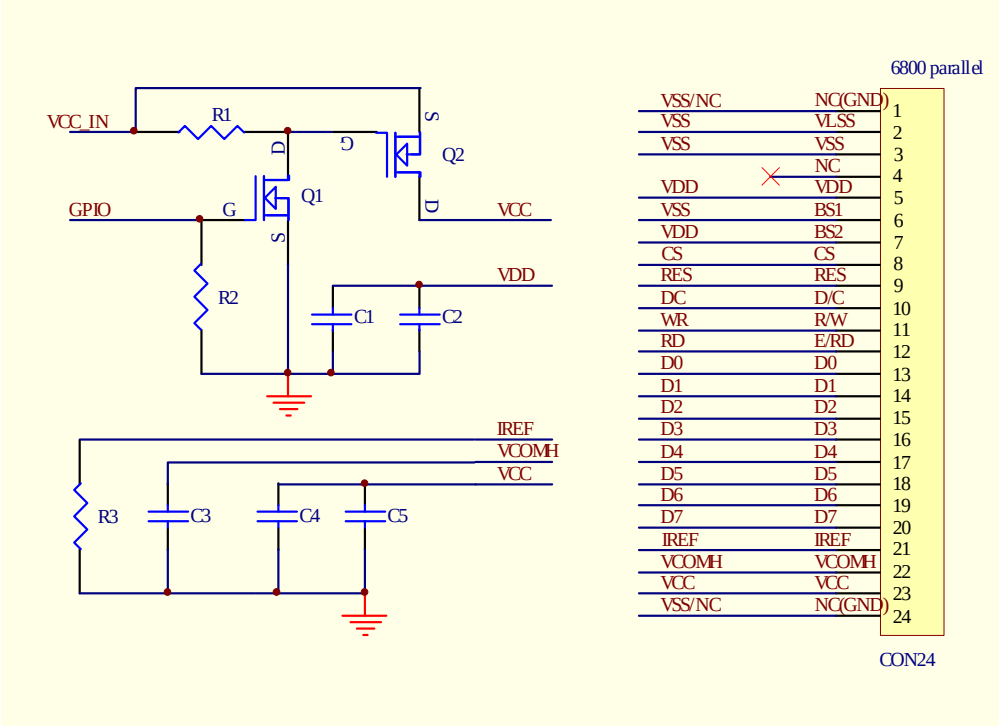
6.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 32 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

6.4 Application circuit reference

6.4.1 68XX-Series MCU Parallel Interface



Recommended Components:

C1: 0.1 µ F / 6.3V, X5R

C2: 4.7 µ F / 6.3V, X5R

C3: 2.2 µ F /25V

C4: 4.7 µ F / 25V, X7R

C5: 0.1 µ F / 25V, X7R

R3: 910kΩ , R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ

Q1: FDN338P

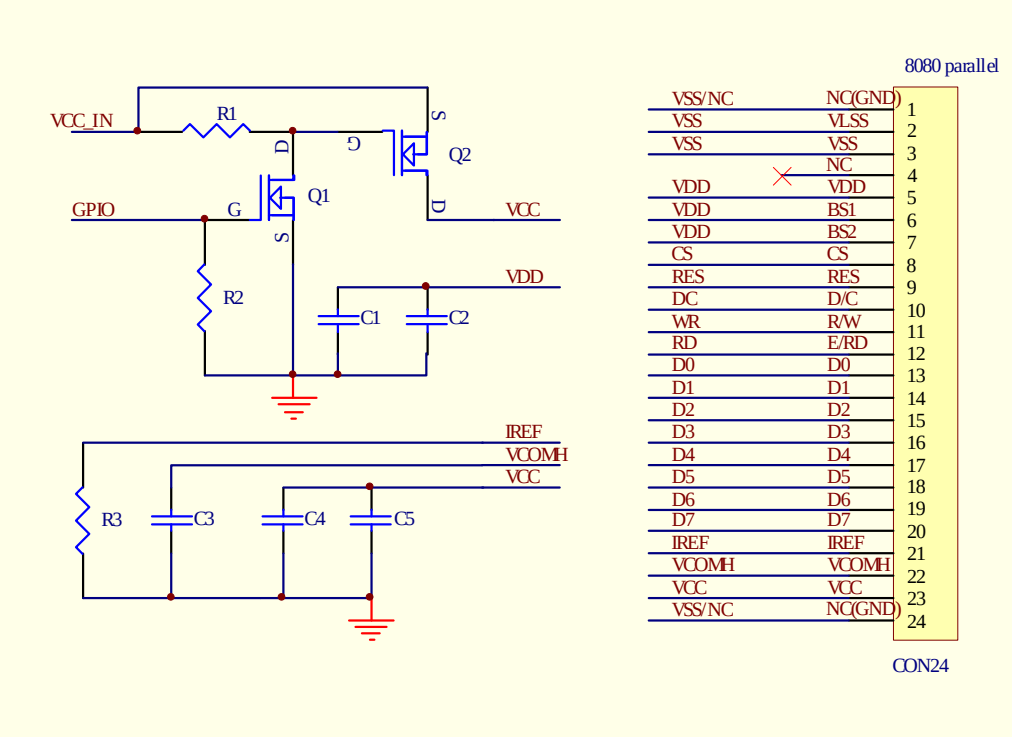
Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MCU I/O voltage.

V_{CC_IN}: 7~15V

6.4.2 80XX-Series MCU Parallel Interface



Recommended Components:

C1: 0.1 µ F / 6.3V, X5R

C2: 4.7 µ F / 6.3V, X5R

C3: 2.2 µ F /25V

C4: 4.7 µ F / 25V, X7R

C5: 0.1 µ F / 25V, X7R

R3: 910kΩ , R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ

Q1: FDN338P

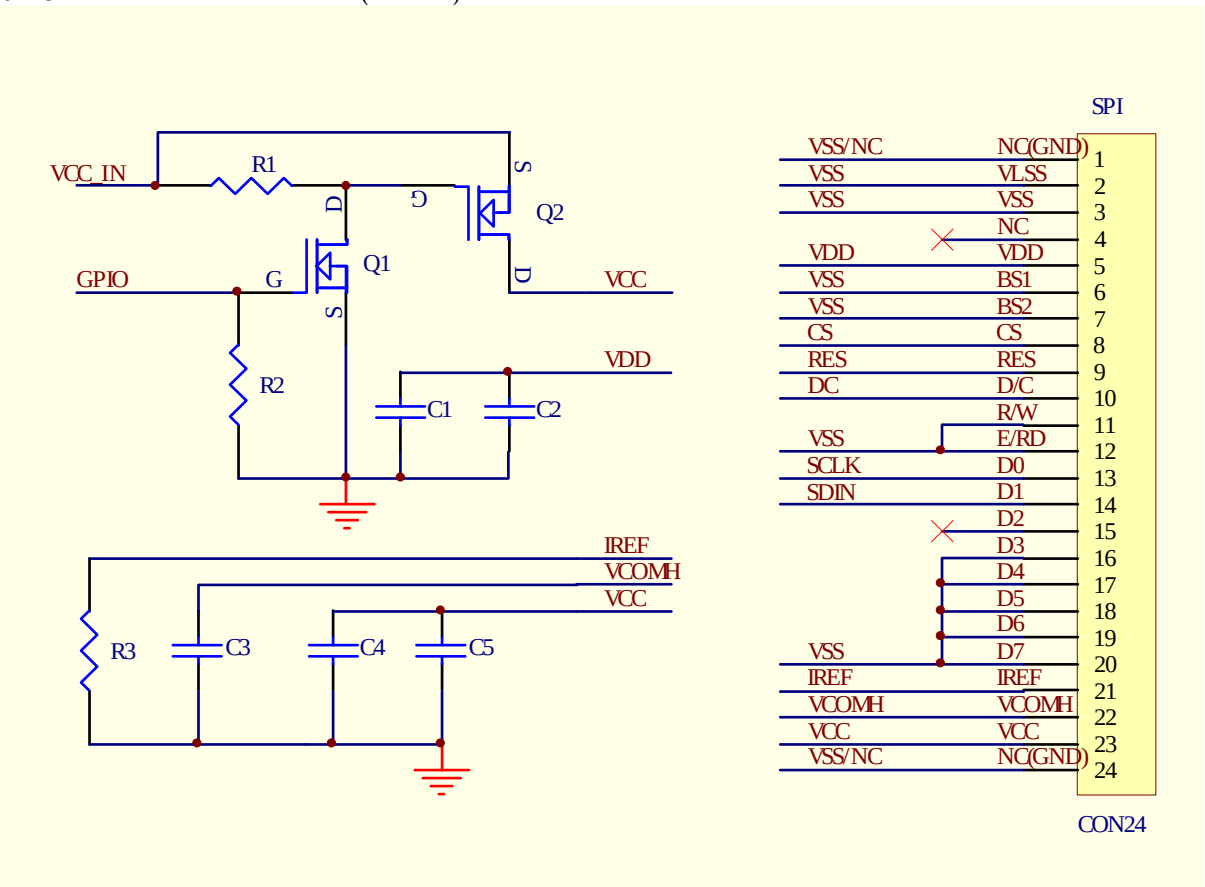
Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MCU I/O voltage.

V_{CC_IN}: 7~15V

6.4.3 4-wire Serial Interface(default)



Recommended Components:

C1: 0.1 µ F / 6.3V, X5R

C2: 4.7 µ F / 6.3V, X5R

C3: 2.2 µ F /25V

C4: 4.7 µ F / 25V, X7R

C5: 0.1 µ F / 25V, X7R

R3: 910kΩ , R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ

Q1: FDN338P

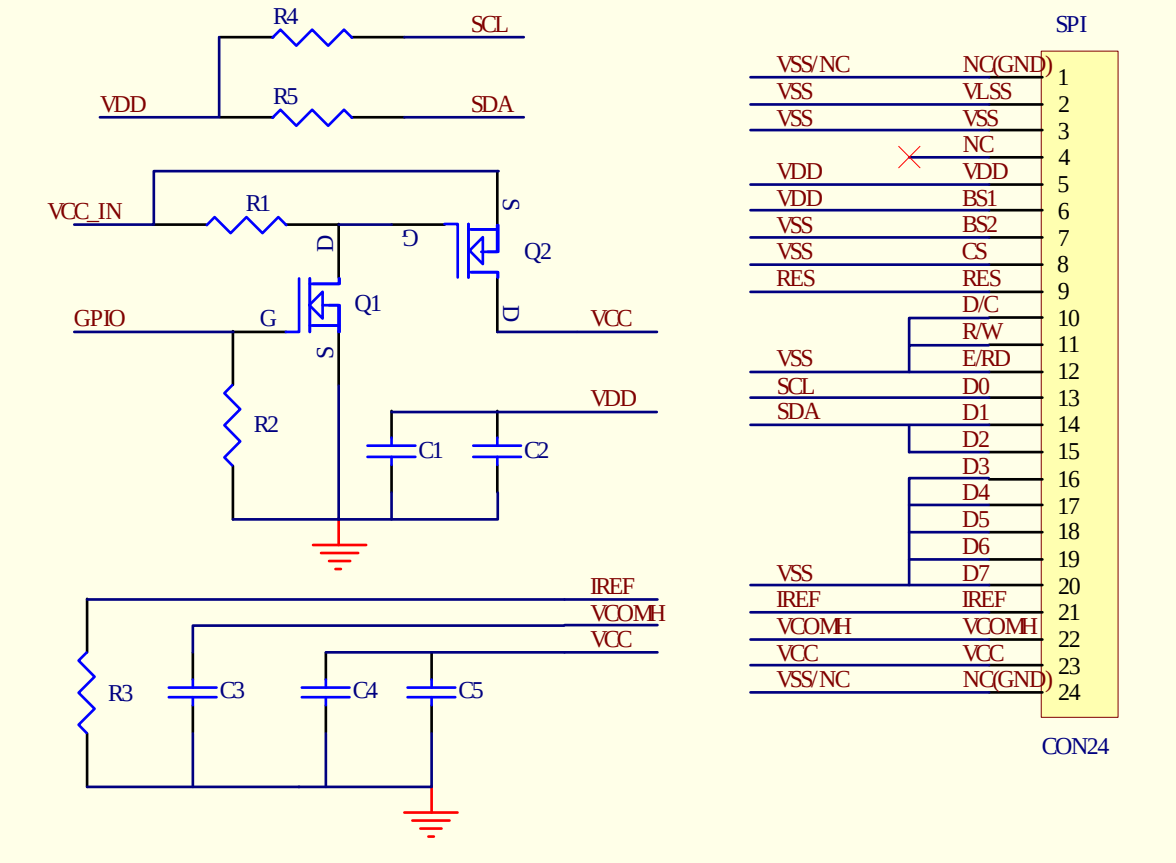
Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MCU I/O voltage.

V_{CC_IN}: 7~15V

6.4.4 I_2C Interface



Recommended Components:

C1: 0.1 µ F / 6.3V, X5R

C2: 4.7 µ F / 6.3V, X5R

C3: 2.2 µ F /25V

C4: 4.7 µ F / 25V, X7R

C5: 0.1 µ F / 25V, X7R

R3: 910kΩ , R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ

R4, R5: 4.7kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MCU I/O voltage.

V_{CC_IN}: 7~15V

7 Power ON/OFF Timing Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1305 (assume V_{DD} and V_{DDIO} are at the same voltage level).

Power ON sequence:

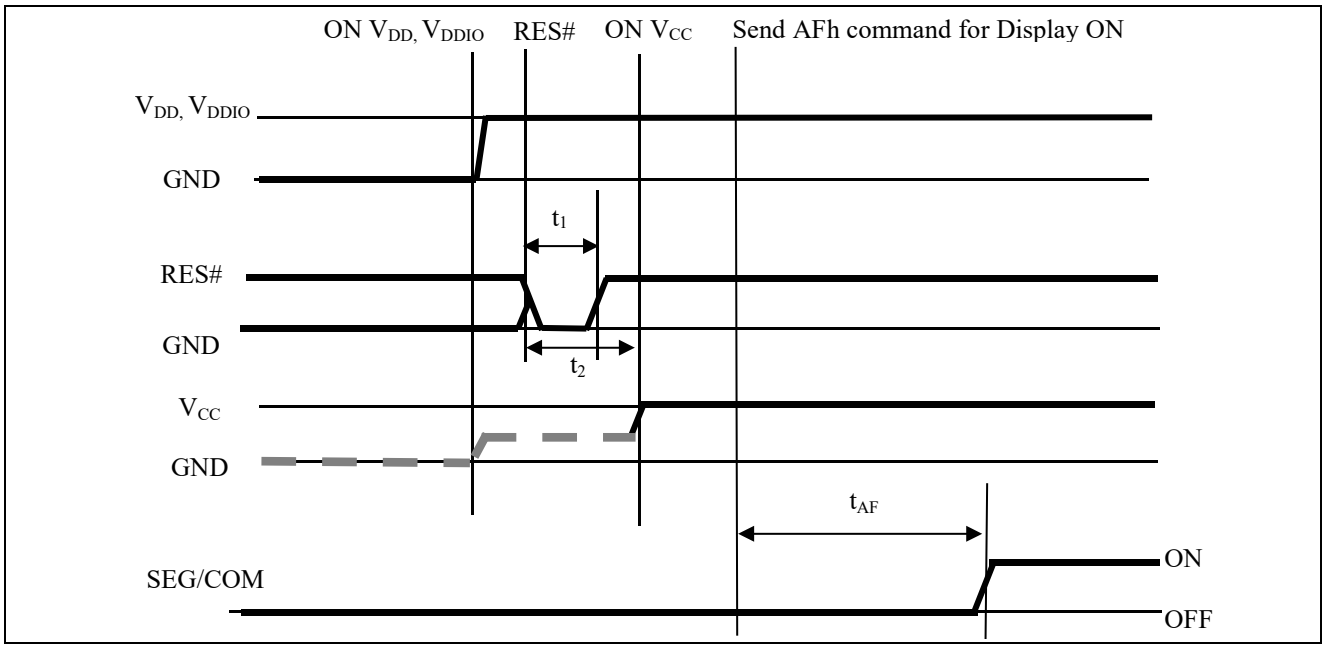
1. Power ON V_{DD},V_{DDIO}.

2. After V_{DD},V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) and then HIGH (logic high).

3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. (1)

4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).

Figure 7-1 : The Power ON sequence



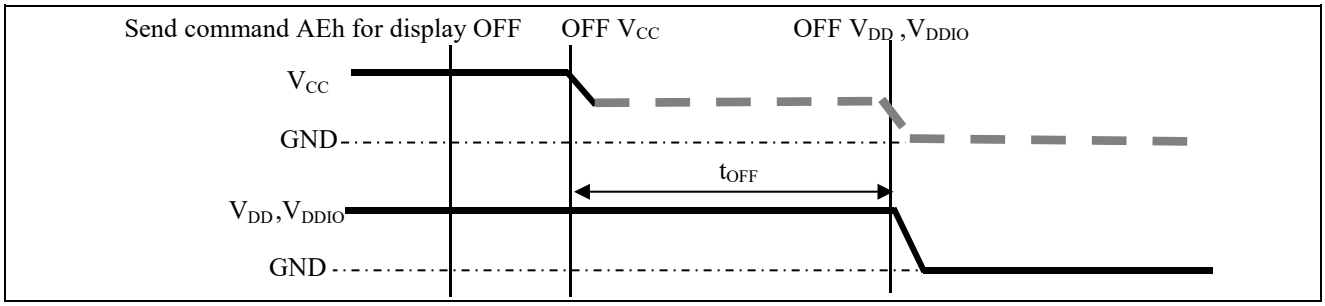
Power OFF sequence:

1. Send command AEh for display OFF.

2. Power OFF V_{CC}.(1), (2)

3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=0ms(3), Typical t_{OFF}=100ms)

Figure 7-2 : The Power OFF sequence

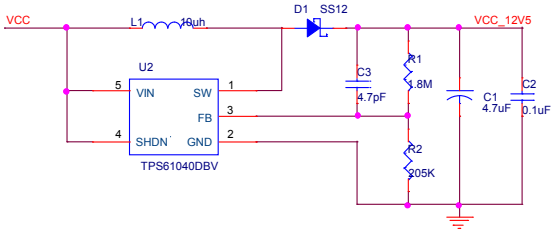


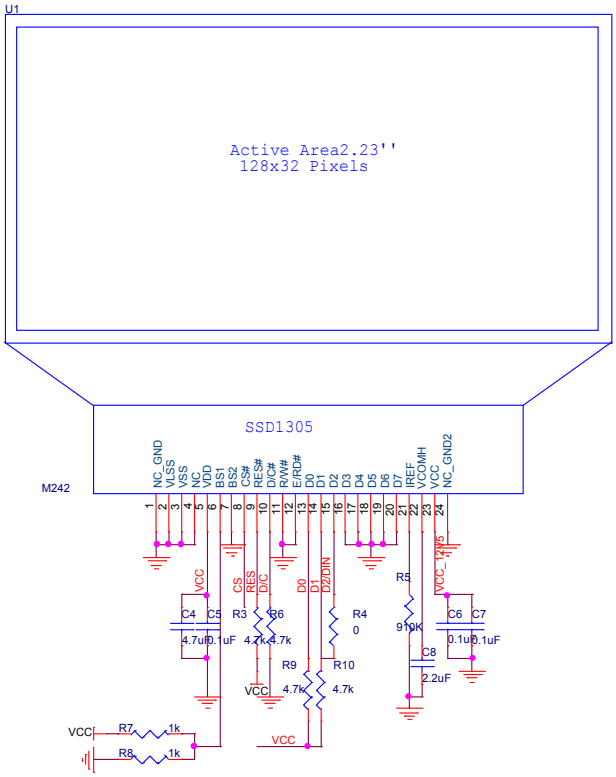
Note:

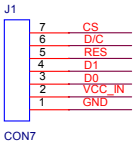
(1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-1 and Figure 7-2.
(2) V_{CC} should be kept float (disable) when it is OFF.

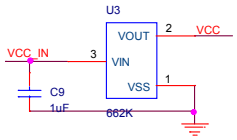
8 Module Schematic

2.23'' 128*32 homochromy OLED

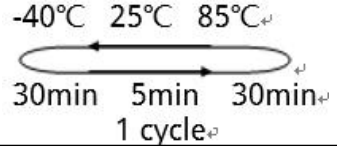








9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85℃ 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40℃ 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 ℃ 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 120hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40℃/85℃ 24 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"