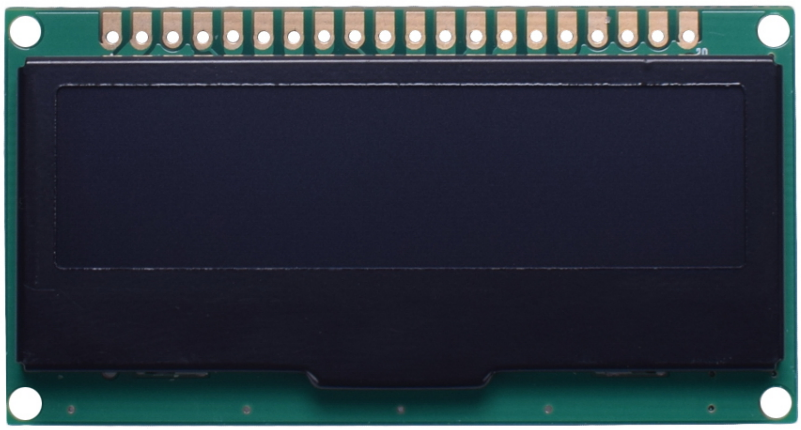
DisplayModule



DM-OLED22-612

BLUE GRAPHIC OLED DISPLAY WITH 8-BIT PARALLEL, I²C OR 4-WIRE SPI MPU INTERFACE

Contents

1 Revision History

Date	Changes
2015-03-13	First release

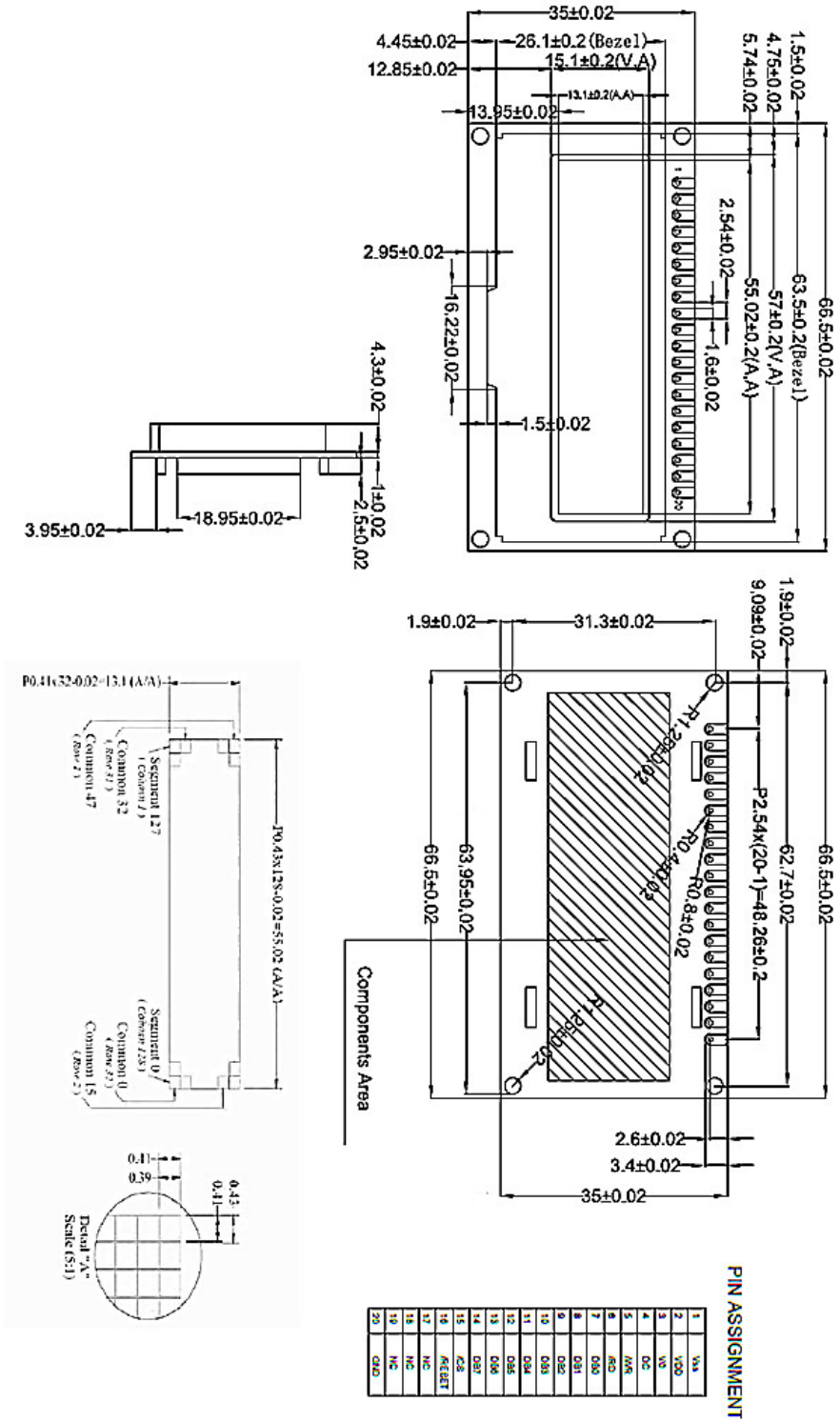
2 Main Features

Item	Specification	Unit
Diagonal Size	2.23	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Blue	
Resolution	128 x 32	pixel
Controller IC	SSD1305	-
Duty	1/32	
Interface	8-Bit 68XX/80XX Parallel、4-Wire SPI、I2C	-
Power Supply	3.3V	V
Viewing Area	57.0 x 15.1	mm
Weight	18.1	g

3 Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>2</td><td>VDD</td><td>Power Supply for Display Module Circuit
This is a voltage supply pin. It connected to external source.</td></tr>
<tr><td>3</td><td>V0</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip.
Please let it Float.</td></tr>
<tr><td>4</td><td>/DC</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>5</td><td>/WR</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin while used as Read/Write (R/W) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR) input. Data write operation is initiated when this pin is pulled low and the CS is pulled low.</td></tr>
<tr><td>6</td><td>/RD</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to an 68XX-series microprocessor, this pin will be used as the Enable(E) signal. Read/Write operation is initiated when this pin is pulled high and the CS is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read(RD) signal. Data read operation is initiated when this pin is pulled low CS is pulled low.</td></tr>
<tr><td>7-14</td><td>DB0-DB7</td><td>Host Data Input/output Bus
These pins are 8-bits bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.</td></tr>
<tr><td>15</td><td>CS</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>16</td><td>Reset</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>17
18</td><td>BS1
BS2</td><td>Communicating Protocol Select
These pins MCU interface selection input. See the following table:
<table>
<tr><td></td><td>68XX-parallel</td><td>80XX-parallel</td><td>I2C</td><td>Serial</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>19</td><td>NC</td><td colspan="2">Float or connect to VSS</td></tr>
<tr><td>20</td><td>FG</td><td colspan="2">It connected to external ground</td></tr>
</table>

4 Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD		2.8		3.5	V
Digital Operation Current	IDD	Ta=25℃		38	-	mA
Low Level Input Voltage	V_{IL}		0	-	0.2VDD	V
High Level Input Voltage	V_{IH}		0.8VDD	-	VDD	V
Low Level Output Voltage	V_{OL}		0		0.1VDD	V
High Level Output Voltage	V_{OH}		0.9VDD		VDD	V
Operating Temperature	TOP	Absolute Max	-40		85	℃
Storage Temperature	TST	Absolute Max	-45		90	℃

6 Optical Characteristics

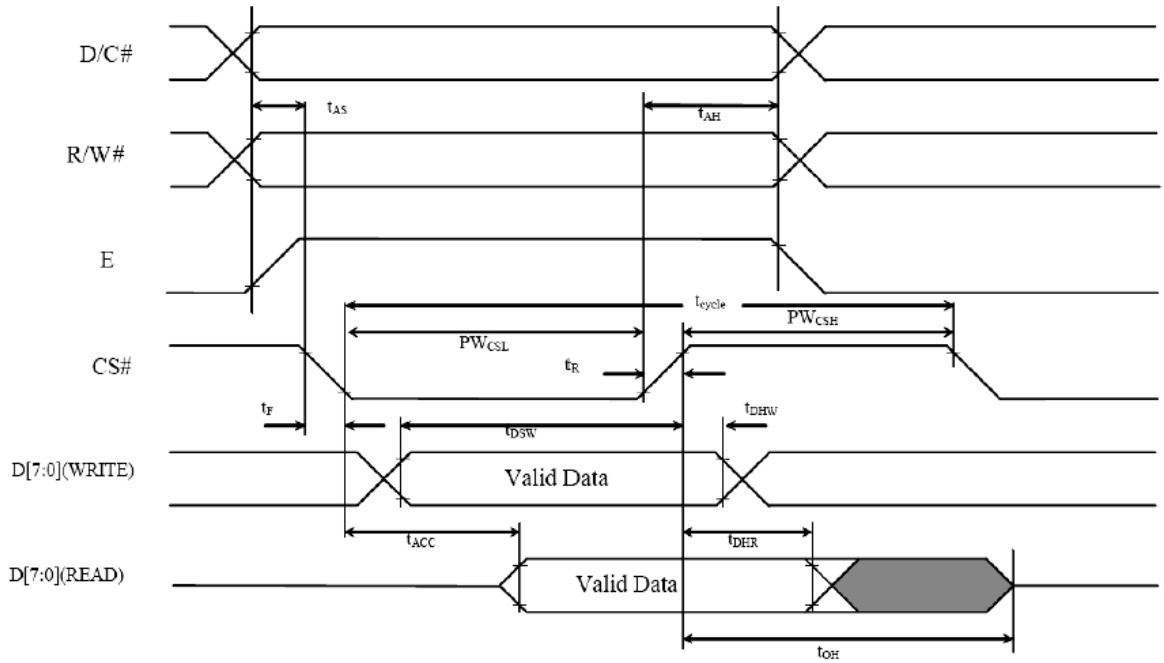
Item	Symbol	Min	Typ	Max	Unit
View Angles Left	AH		80		°
View Angles Right	AH		80		°
View Angles Top	AV		80		°
View Angles Bottom	AV		80		°
Response Time (25°C)	Tr + Tf		20		us
Contrast Ratio	CR	2000:1			
Brightness	L_V	120	150		cd/m²
Lifetime		20,000			Hrs

7 Timing Characteristics

7.1 68XX-Series MPU Parallel Interface Timing Characteristics:

TA=25℃,VDD-VSS=2.4V to 3.5V

Symbol	Item	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time(write cycle)	300	-	-	ns
P_{WCSL}	Control Pulse Low Width(write cycle)	60			
P_{WCSH}	Control Pulse High Width(write cycle)	60			
t_{CYCLE}	Clock Cycle Time(read cycle)	200			
PW_{CSL}	Control Pulse Low Width(read cycle)	120	-		ns
PW_{CSH}	Control Pulse High Width(read cycle)	60	-		ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	40	-	-	ns
t_{DHW}	Data Hold Time	7	-	-	ns
t_{ACC}	Access Time	-		140	
t_{OH}	Output Disable Time	-	-	70	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

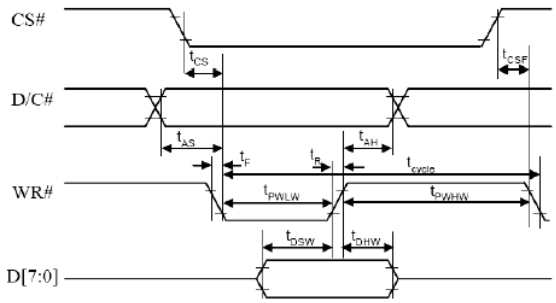


7.2 80XX-Series MPU Parallel Interface Timing Characteristics

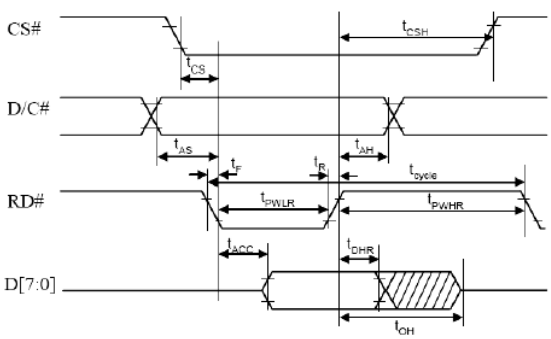
TA=25℃,VDD-VSS=2.4V to 3.5V

Symbol	Item	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width(Read) Chip Select Low Pulse Width(Write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width(Read) Chip Select High Pulse Width(Write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip Select Time	0			
t_{CSH}	Chip Select Hold Time to Read signal	0			
t_{CSF}	Chip Select Hold Time	20			

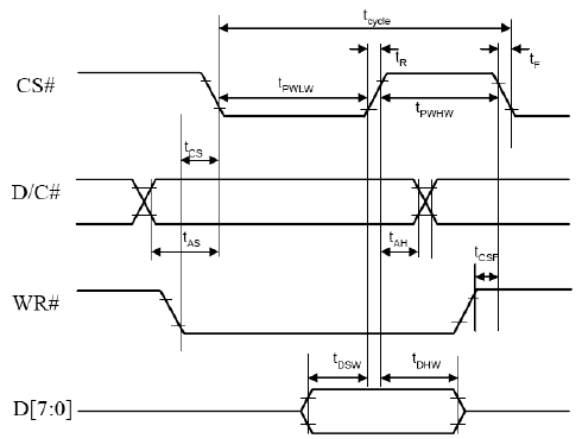
Write cycle (Form 1)



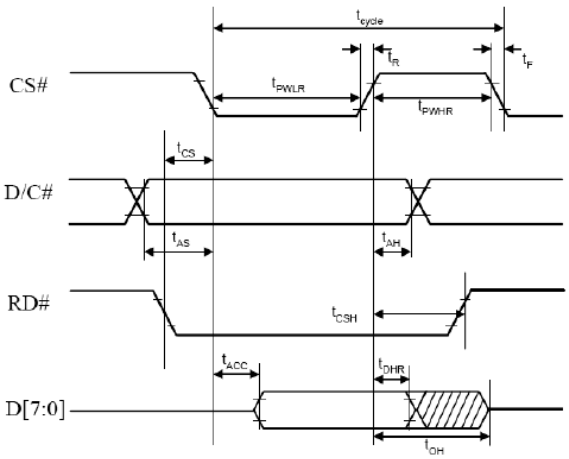
Read cycle (Form 1)



Write cycle (Form 2)

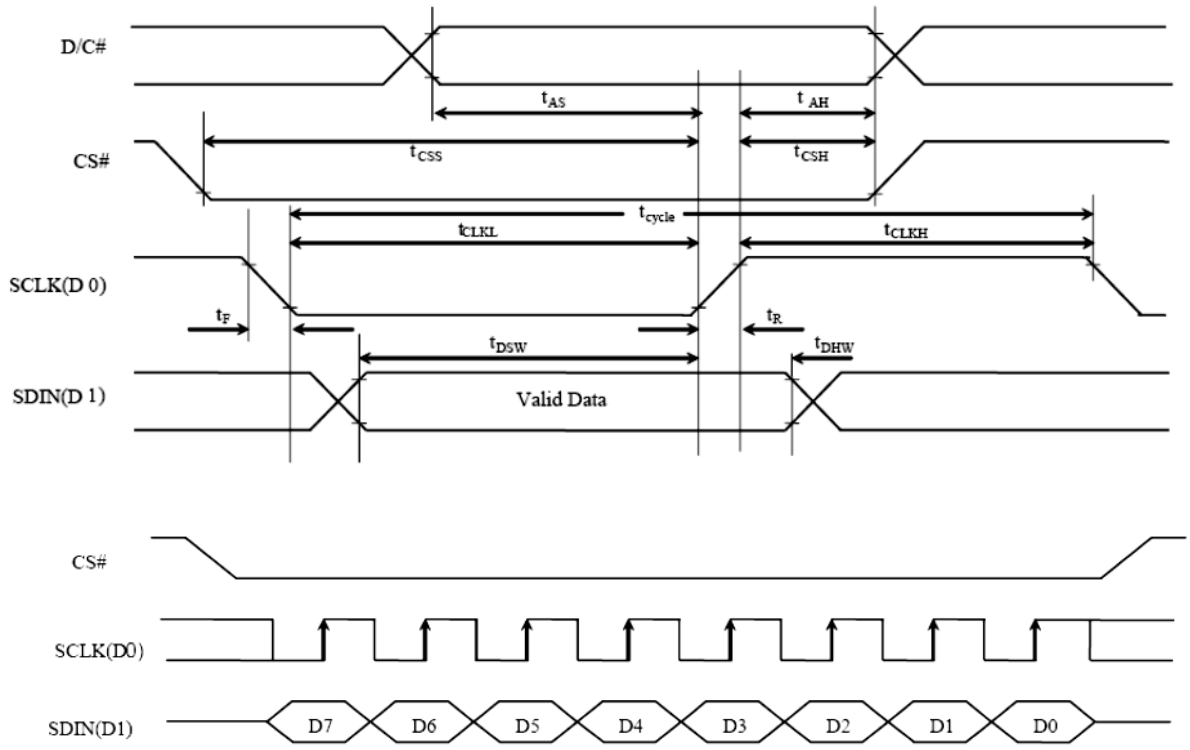


Read cycle (Form 2)



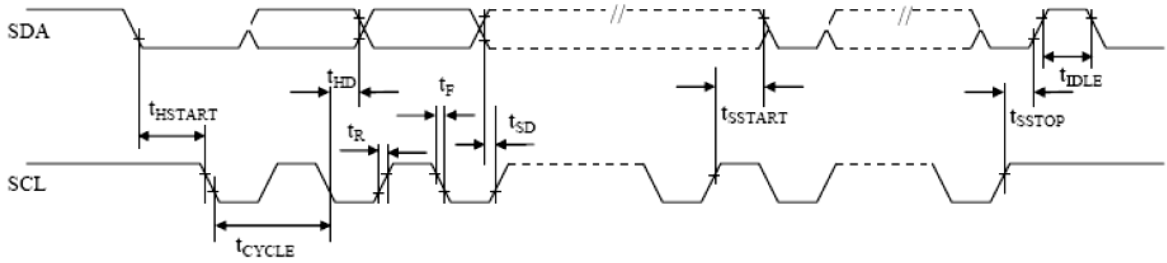
7.3 Serial Interface Timing Characteristics

Symbol	Item	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CS}	Chip Select Setup Time	120			
t_{CSH}	Chip Select Hold Time	60			
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



7.4 I2C Interface Timing Characteristics

Symbol	Item	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time(for "SDAOUT" pin) Data Hold Time(for "SDIN" pin)	0 300	-	-	ns ns
t_{SD}	Data Setup Time	100			ns
t_{SSTART}	Start Condition Setup Time(Only relecant for a repeated Start condition)	0.6			us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



8 MCU Interface selection

MCU Interface assignment under different bus interface mode:

Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
SPI	Tie LOW					NC	SDI	SCLK	Tie LOW		/CS	D/C	/RES
I2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	/RES

8.1 MCU parallel 6800-series interface

The parallel interface consists of 8 bi-directional data pins (DB[7:0}), R/W, D/C,E and /CS. A LOW in R/W indicates WRITE operation and HIGH in R/W indicates READ operation. A LOW in D/C indicates COMMAND read/write and HIGH in D/C indicates DATA read/write. The E input serves as data latch signal while /CS is LOW. Data is latched at the falling edge of E signal.

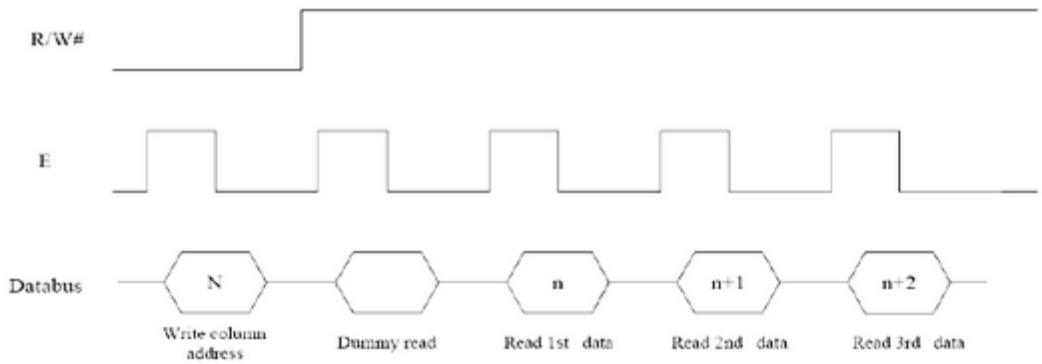
Control pins of 6800 interface

Function	E	R/W	/CS	D/C
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note: ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown as follows.

Data read back procedure-insertion of dummy read



8.2 MCU parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (DB[7:0]), /RD, /WR, D/C and /CS. A LOW in A0 indicates COMMAND read/write and HIGH in D/C indicates DATA read/write. A rising edge of /ER input serves as a data/command WRITE latch signal while /CS is kept LOW.

Control pins of 8080 interface (Form 1)

Function	/RD	/WR	/CS	D/C
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note: (1) ↓ stands for falling edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics.

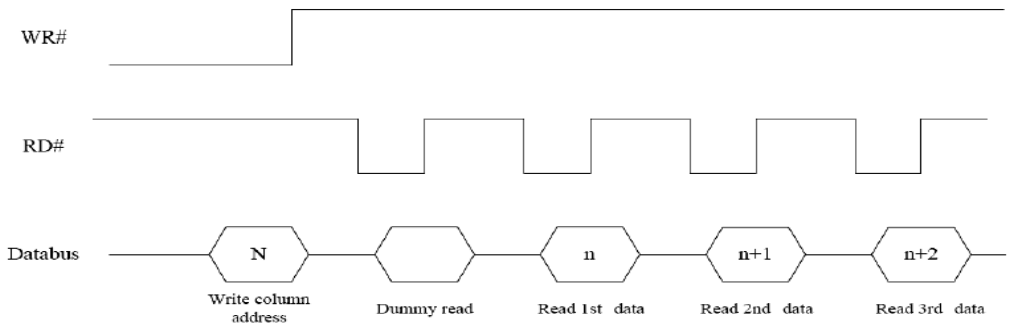
Alternatively, /RD and /WR can be keep stable while /CS serves as the data/command latch signal.

Control pins of 8080 interface (Form 1)

Function	/RD	/WR	/CS	D/C
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note: (1) ↓ stands for falling edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 13-3 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is performed which requires the insertion of a dummy read before the first actual display data read. This is shown as follows.



8.3 MCU Serial Interface

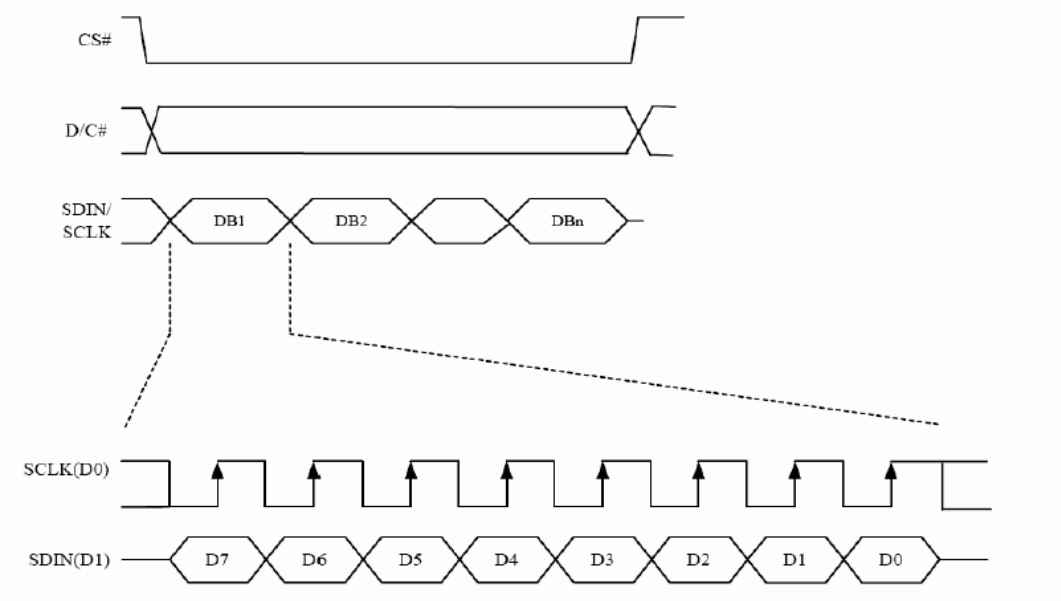
The serial interface consists of serial clock SCLK, serial data SDIN , D/C ,/CS. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W can be connected to an external ground.

Control pins of Serial interface

Function	E	R/W	/CS	D/C
Write command	Tie Low	Tie Low	L	L
Write data	Tie Low	Tie Low	L	H

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6,...D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Write procedure in SPI mode



8.4 MCU I2C Interface

The I2C communication interface consists of slave address bit SA0, I2C-bus data signal SDA(SDAOUT/D2 for output and SDAIN/D1 for input) and I2C-bus clock signal SCL (D0). Both the data and clock signals must be connected to pull-up resistors. /RES is used for the initialization of device.

a) Slave address bit (SA0)

SSD1305 has to recognize the slave address before transmitting or receiving any information by the I2C-bus. The device will respond to the slave address following by the slave address bit("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format.

b7	b6	b5	b4	b3	b2	b1	b0
0	1	1	1	1	0	SA0	R/W

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1305. DC pin acts as SA0 for slave address selection. "R/W" bit is used to determine the operation mode of the I2C-bus interface. R/W=1, it is in read mode. R/W=0, it is in write mode.

b) I2C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgment would not be possible to attain a valid logic 0 level in "SDA". "SDAIN" and "SDAOUT" are tied together and serve as SDA. The "SDAIN" pin must be connected to act as SDA. The "SDAOUT" pin is disconnected, the acknowledgement signal will be ignored in the I2C-bus.

c) I2C-bus clock signal (SCL)

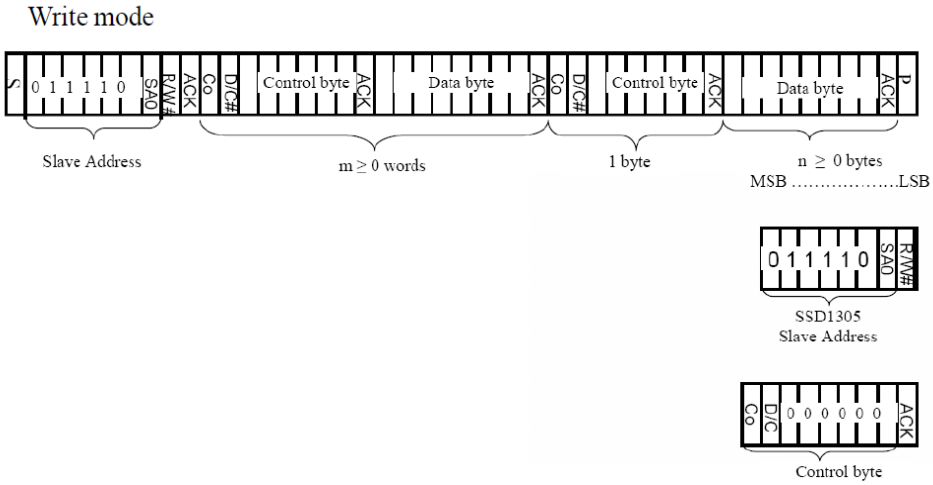
The transmission of information in the I2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.4.1 I2C-bus Write data

The I2C-bus interface gives access to write data and command into the device. Please refer to the following Figure for the write mode of I2C-bus in chronological order.

I2C-bus data format

Note: Co – Continuation bit
D/C# - Data / Command Selection bit
ACK – Acknowledgement
SA0 – Slave address bit
R/W# - Read/Write Selection bit
S – Start Condition / P – Stop Condition



8.4.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in the following Figure(1). The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1305, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (DC pin acts as SA0).
3) The write mode is established by setting the R/W bit to logic “0”
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W bit. Please refer to the following Figure (2) for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of C0 and A0 bits following by six “0” ‘s.
    a) If the Co bit is set as logic “0”, the transmission of following information will contain data bytes only.
    b) The A0 bit determines the next data byte is acted as a command or a data. If the A0 bit is set to logic “0”, it defines the following data byte as a command. If the A0 bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.

6) Acknowledge bit will be generated after receiving each control byte or data byte.

7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure (1). The stop condition is established by pulling the "SDA in " from LOW to HIGH while the "SCL" stays HIGH.

Figure (1): Definition of the Start and Stop Condition

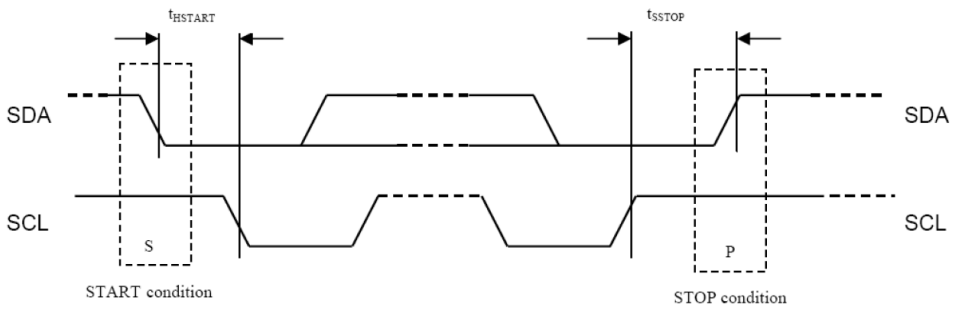
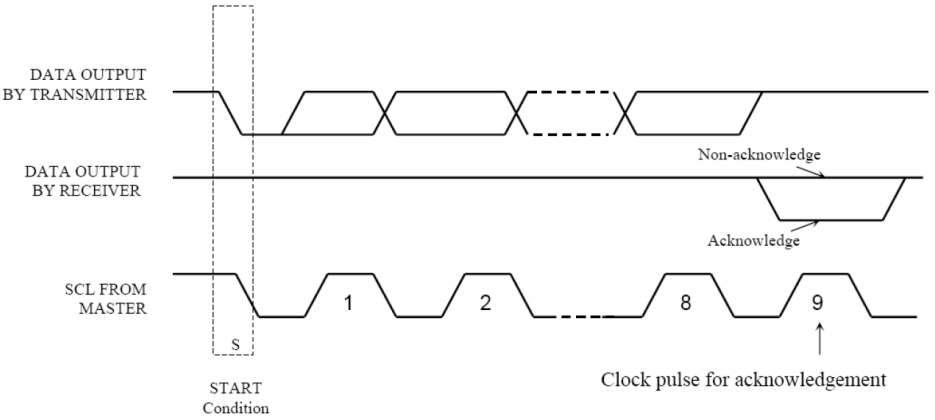


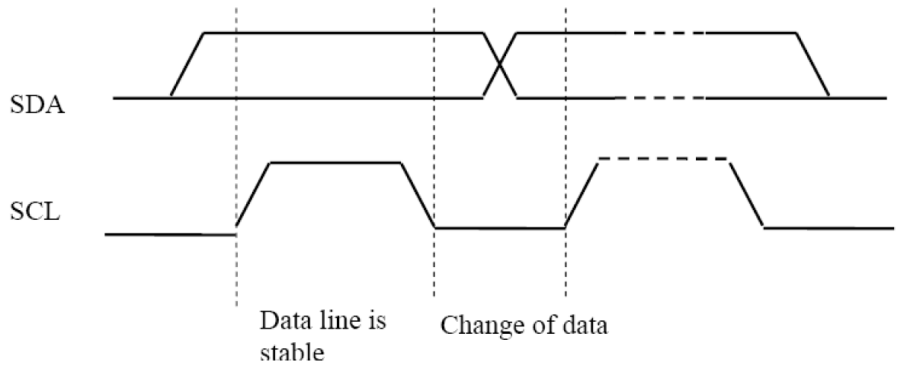
Figure (2): Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

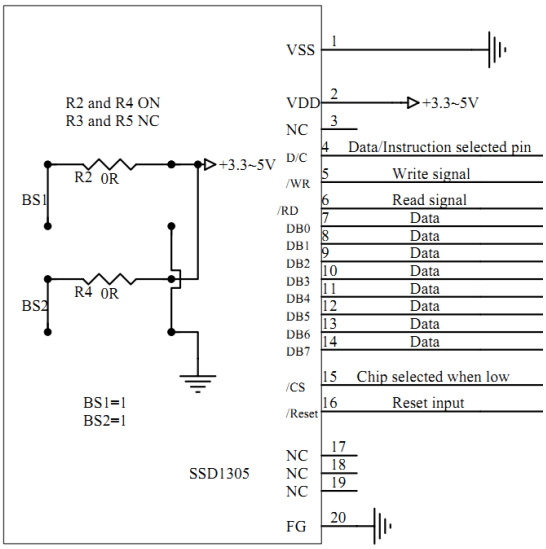
1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure (3) for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure (3): Definition of the data transfer condition



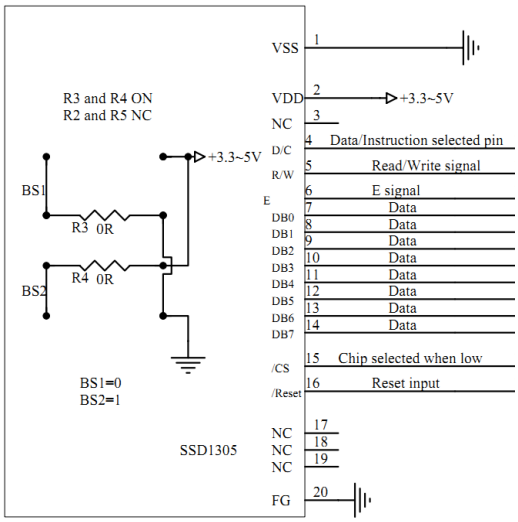
9 Application Reference

The Parallel (8080 Series MCU)Reference Example



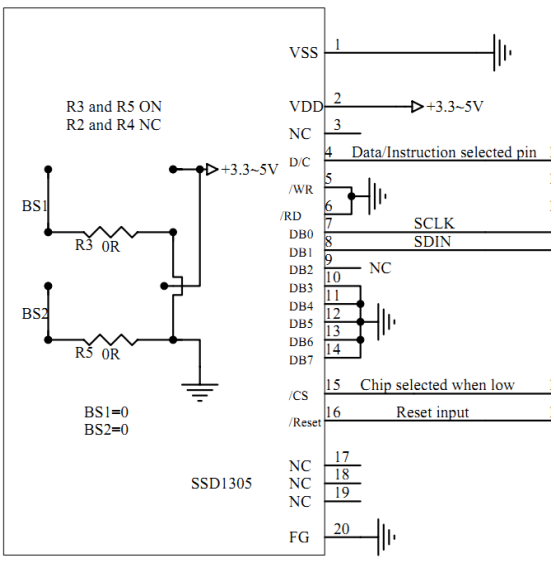
DM-OLED22-612

The Parallel (6800 Series MCU)Reference Example



DM-OLED22-612

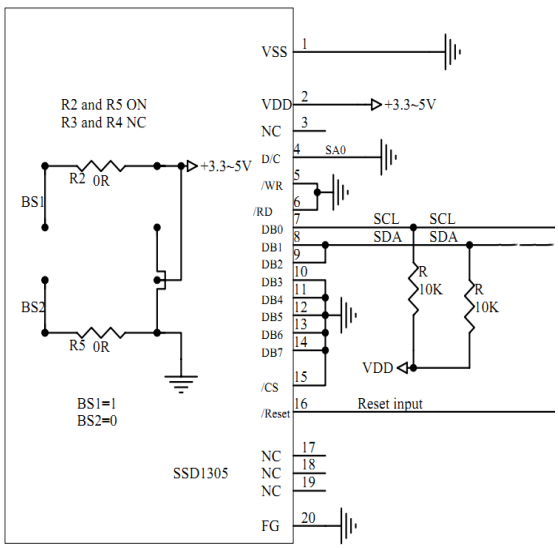
The Serial 4 Line SPI Reference Example



DM-OLED22-612

The Serial I2C Reference Example

If SA0(PIN4)Connected to the ground
Write Slave Address :0x78
Read Slave Address:0x79



DM-OLED22-612

10 Driver/Controller Information

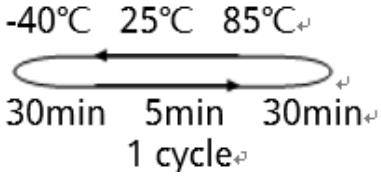
Built-in SSD1305 Controller:

https://drive.google.com/file/d/0Bxu0OURUiyL5RUE0R2VCVXl1ZnM/view?usp=sharing

11 Example Initialization Code

```
void Write_Data(unsigned char dat)
{
        RS=1;
        CS=0;
          _RW=0;
         DATA_BUS=dat;
         Delayms(2);
          _RW=1;
         CS=1;
 }
 ---------------------------------------------------------------------------------------------------------------------
 void Write_Instruction(unsigned char cmd)
 {
          RS=0;
          CS=0;
          _RW=0;
         DATA_BUS=cmd;
         Delayms(2);
         _RW=1;
         CS=1;
 }
 ---------------------------------------------------------------------------------------------------------------------
 void LCD_initialize(void)
{
       RES=0;
       Delayms(200);
       RES=1;
       Delayms(200);
       Write_Instruction(0xae);  //--turn off oled panel
       Write_Instruction(0xd5);  //--set display clock divide ratio/oscillator frequency
       Write_Instruction(0xa0);  //--set divide ratio
       Write_Instruction(0xa8);  //--set multiplex ratio(1 to 64)
       Write_Instruction(0x1f);  //--1/32 duty
       Write_Instruction(0xd3);  //-set display offset
       Write_Instruction(0x00);  //-not offset
       Write_Instruction(0xad);  //--Set Master Configuration
       Write_Instruction(0x8e);  //--
       Write_Instruction(0xd8);  //--Set Area Color Mode On/Off & Low Power Display Mode
       Write_Instruction(0x05);  //
       Write_Instruction(0xa1);  //--set segment re-map 132 to 0
       Write_Instruction(0xC8);  //--Set COM Output Scan Direction 64 to 1
       Write_Instruction(0xda);  //--Set COM Pins Hardware Configuration
       Write_Instruction(0x12);
       Write_Instruction(0x91);  //--Set current drive pulse width of BANK0, Color A, Band C.
       Write_Instruction(0x3f);
       Write_Instruction(0x3f);
       Write_Instruction(0x3f);
       Write_Instruction(0x3f);
       Write_Instruction(0x81);  //--set contrast control register
       Write_Instruction(Contrast_level);
       Write_Instruction(0xd9);  //--set pre-charge period
       Write_Instruction(0xd2);
       Write_Instruction(0xdb);  //--set vcomh
       Write_Instruction(0x34);
       Write_Instruction(0xa6);  //--set normal display
       Write_Instruction(0xa4);  //Disable Entire Display On
       Write_Instruction(0xaf);  //--turn on oled panel
    }
```

12 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	90℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-45℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85℃ 200hrs	2
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 ℃ 200hrs	1,2
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40℃/85℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.
Note3: Test performed on product itself, not inside a container.

13 Warranty and Conditions

http://www.displaymodule.com/pages/faq