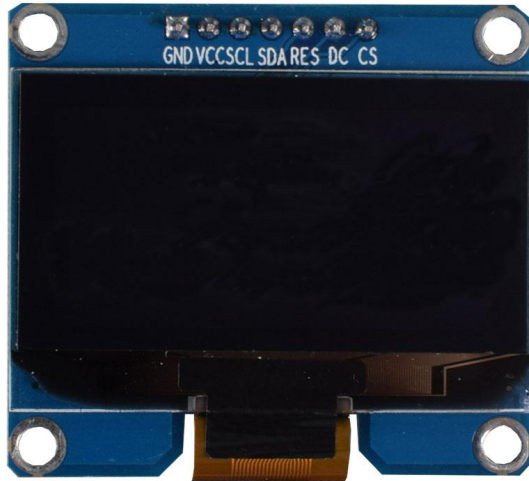


# DisplayModule



DM-OLED154-639

1.54" 128 x 64 MONOCHROME GRAPHIC  
OLED DISPLAY MODULE-SPI

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## 1 Revision History

Date	Changes
2018-09-28	First release

## 2 Main Features

Item	Specification	Unit
Diagonal Size	1.54	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome	Colors
Resolution	128 x 64	pixel
Controller IC	SPD0301	-
Interface	4wire SPI	-
Active Area	35.052 x 17.516	mm
Module Dimension	38.00 x 42.4	mm
Weight	TBD	g

## 3 Pin Description

### 3.1 Panel Pin Description

Pin No.	Symbol	Function Description															
1	N.C. (GND)	Reserved Pin(Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.															
2	VLSS	Ground of Analog Circuit This is an analog ground pin. It should be connected to VSS externally.															
3	VSS	Ground of Logic Circuit This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.															
4	N.C. (GND)	Reserved Pin(Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.															
5	VDD	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.															
6	BS1 BS2	Communicating Protocol Select This pins are MCU interface selection input. See the following table:															
7		<table border="1"> <thead> <tr> <th></th> <th>BS1</th> <th>BS2</th> </tr> </thead> <tbody> <tr> <td>IIC</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-Wire SPI</td> <td>0</td> <td>0</td> </tr> <tr> <td>8-bit 80XX parallel</td> <td>1</td> <td>1</td> </tr> <tr> <td>8-bit 68XX parallel</td> <td>0</td> <td>1</td> </tr> </tbody> </table>		BS1	BS2	IIC	1	0	4-Wire SPI	0	0	8-bit 80XX parallel	1	1	8-bit 68XX parallel	0	1
		BS1	BS2														
IIC		1	0														
4-Wire SPI		0	0														
8-bit 80XX parallel	1	1															
8-bit 68XX parallel	0	1															
8	CS#	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.															
9	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.															
10	D/C#	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
11	R/W#	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.															

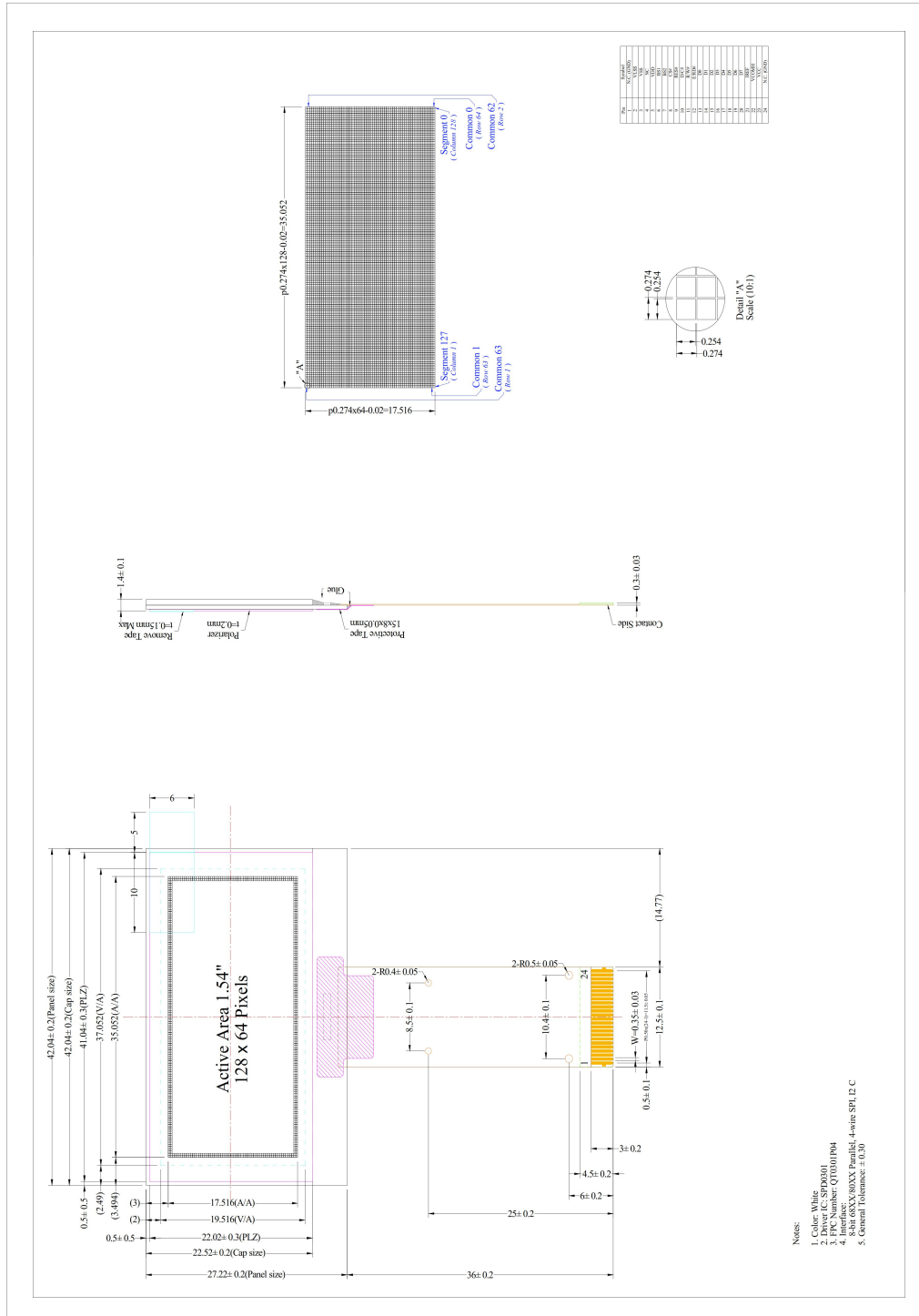
12	E/RD#	<p>Read/Write Enable or Read</p> <p>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.</p> <p>When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.</p> <p>When serial or I2C mode is selected, this pin must be connected to VSS.</p>
13-20	D0-D7	<p>Host Data Input/ Output Bus</p> <p>These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 &amp; D1 should be tied together and serve as SDAout &amp; SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.</p>
21	IREF	<p>Current Reference for Brightness Adjustment</p> <p>This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5 <math>\mu</math> A maximum.</p>
22	VCOMH	<p>Voltage Output High Level for COM Signal</p> <p>This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</p>
23	VCC	<p>Power Supply for OEL Panel</p> <p>This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.</p>
24	N.C. (GND)	<p>Reserved Pin(Supporting Pin)</p> <p>The supporting pins can reduce the influences from stresses on the function pins.</p> <p>These pins must be connected to external ground as the ESD protection circuit.</p>

### 3.2 Module Pin Description

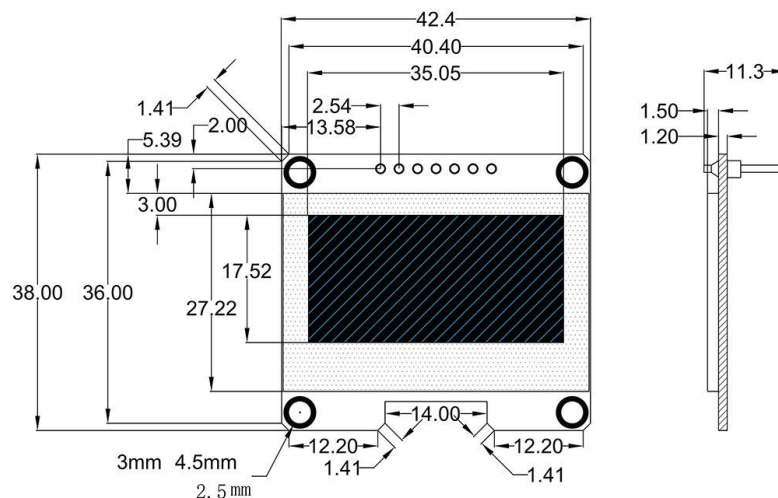
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC	Power Supply 3.3V
3	SCL	SPI Clock
4	SDA	SPI DATA
5	RES	OLED reset Pin.
6	D/C	Data/Command Control This pin is Data/Command control pin.
7	CS	Chip Select This pin is pulled low to active. Connect to ground .

## 4 Mechanical Drawing

### 4.1 Panel Mechanical Drawing



## 4.2 Module Mechanical Drawing



## 5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Power supply	VDD		2.6	3.3	3.5	V
Input Power	VCC IN		4.5		6.5	V
Supply Voltage for Display(for OLED Panel)	Vcc		11.5	12	12.5	V
Segment Output current consumption in Vcc	ISEG	Contrast max	280	310	340	uA
Operating Maximum Temperature	TOP		-40		70	°C
Storage Maximum Temperature	TST		-40		85	°C

## 6 Optical Characteristics

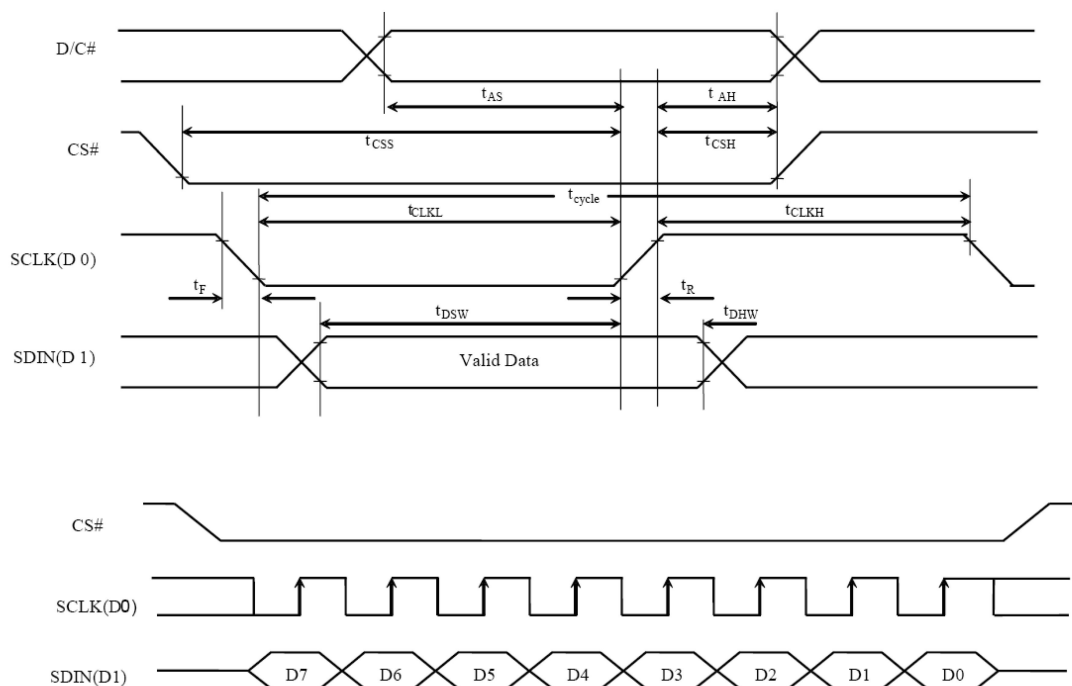
Item	Symbol	Min	Typ	Max	Unit
View Angles		160		-	°
Response Time (25°C)	Tr + Tf		30		ns
Brightness	Lbr	90	110	-	cd/m <sup>2</sup>
Dark room Contrast Ratio	CR	2000:1	-	-	

## 7 AC characteristics

### 7.1 Serial Interface Timing Characteristics (4-wire SPI)

Symbol	Description	Min	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	250	-	ns
$t_{\text{AS}}$	Address Setup Time	150	-	ns
$t_{\text{AH}}$	Address Hold Time	150	-	ns
$t_{\text{CSS}}$	Chip Select Setup Time	120	-	ns
$t_{\text{CSH}}$	Chip Select Hold Time	60	-	ns
$t_{\text{DSW}}$	Write Data Setup Time	50	-	ns
$t_{\text{DHW}}$	Write Data Hold Time	15	-	ns
$t_{\text{CLKL}}$	Clock Low Time	100	-	ns
$t_{\text{CLKH}}$	Clock High Time	100	-	ns
$t_{\text{R}}$	Rise Time	-	15	ns
$t_{\text{F}}$	Fall Time	-	15	ns

\* ( $V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$ ,  $V_{\text{DD}} = V_{\text{DDIO}}$ ,  $T_{\text{a}} = 25^{\circ}\text{C}$ )

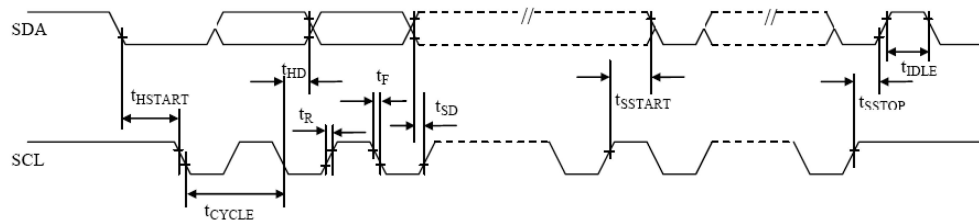




## 7.2 I2C interface characteristics

Symbol	Description	Min	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	2.5	-	$\mu\text{s}$
$t_{\text{HSTART}}$	Start Condition Hold Time	0.6	-	$\mu\text{s}$
$t_{\text{HD}}$	Data Hold Time (for "SDA <sub>OUT</sub> " Pin)	0	-	ns
	Data Hold Time (for "SDA <sub>IN</sub> " Pin)	300		
$t_{\text{SD}}$	Data Setup Time	100	-	ns
$t_{\text{SSTART}}$	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	$\mu\text{s}$
$t_{\text{SSTOP}}$	Stop Condition Setup Time	0.6	-	$\mu\text{s}$
$t_{\text{R}}$	Rise Time for Data and Clock Pin		300	ns
$t_{\text{F}}$	Fall Time for Data and Clock Pin		300	ns
$t_{\text{IDLE}}$	Idle Time before a New Transmission can Start	1.3	-	$\mu\text{s}$

\* ( $V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$ ,  $T_{\text{a}} = 25^{\circ}\text{C}$ )

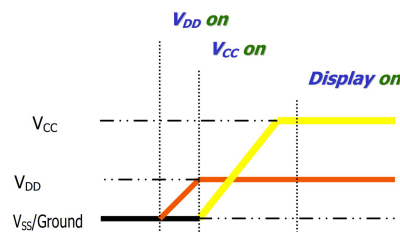


## 8 Power on/off sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

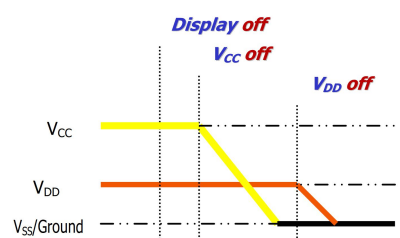
### 4.2.1 Power up Sequence:

1. Power up  $V_{DD}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up  $V_{CC}$
6. Delay 100ms  
(When  $V_{CC}$  is stable)
7. Send Display on command



### 4.2.2 Power down Sequence:

1. Send Display off command
2. Power down  $V_{CC}$
3. Delay 100ms  
(When  $V_{CC}$  is reach 0 and panel is completely discharges)
4. Power down  $V_{DD}$



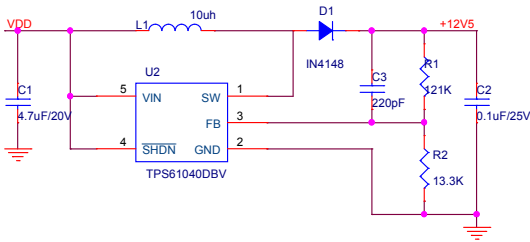
### Note 13:

- 1) Since an ESD protection circuit is connected between  $V_{DD}$  and  $V_{CC}$  inside the driver IC,  $V_{CC}$  becomes lower than  $V_{DD}$  whenever  $V_{DD}$  is ON and  $V_{CC}$  is OFF.
- 2)  $V_{CC}$  should be kept float (disable) when it is OFF.
- 3) Power Pins ( $V_{DD}$ ,  $V_{CC}$ ) can never be pulled to ground under any circumstance.
- 4)  $V_{DD}$  should not be power down before  $V_{CC}$  power down.

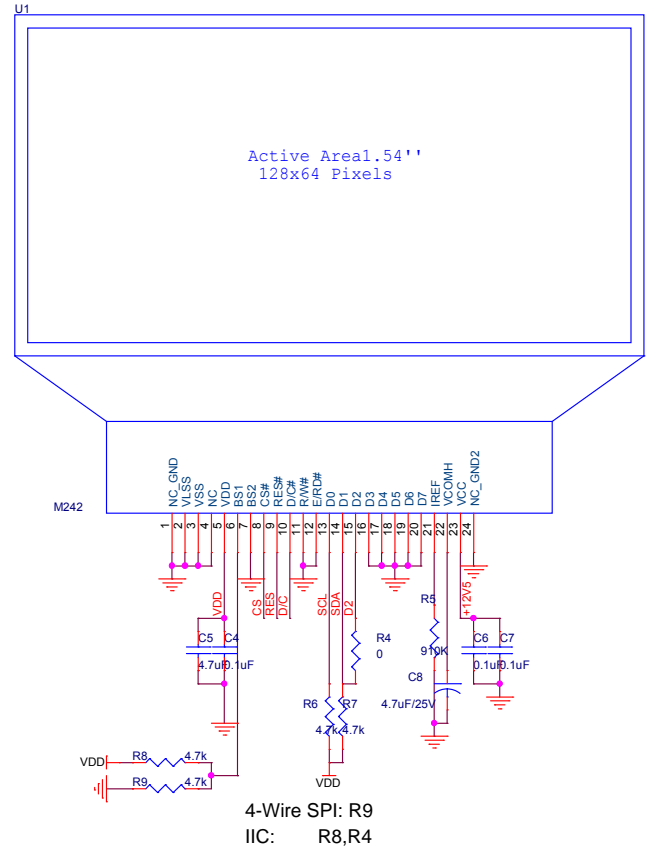
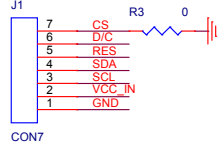
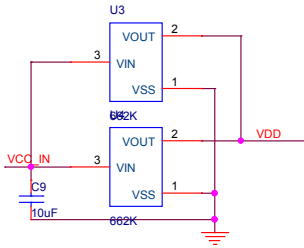
## 9 Schematic

### 9.1 Module schematic

1.54'' 128\*64

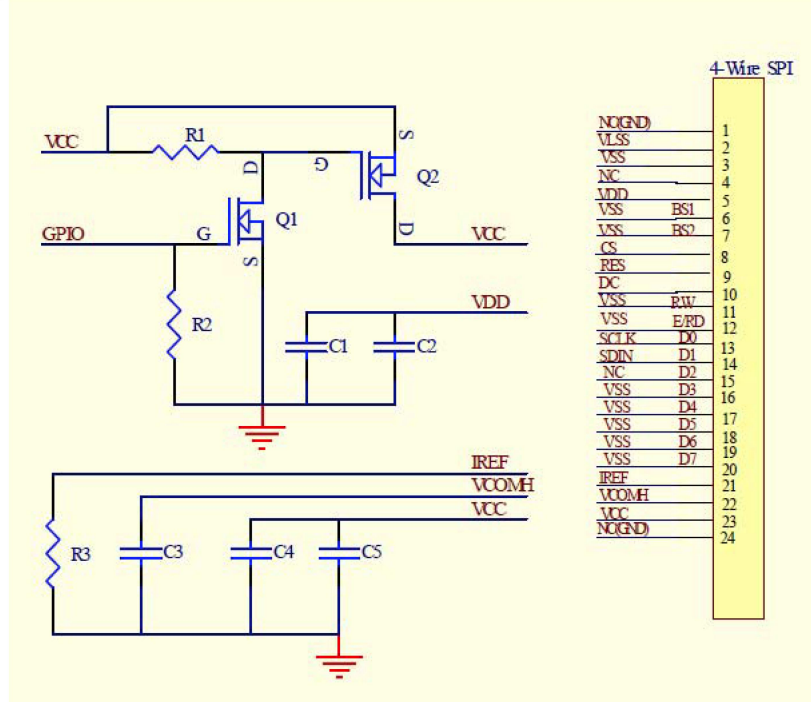


R3 default None  
R3 connect to GND if do not use CS pin



## 9.2 Application circuit for 4-wire SPI mode

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



### Recommended Components:

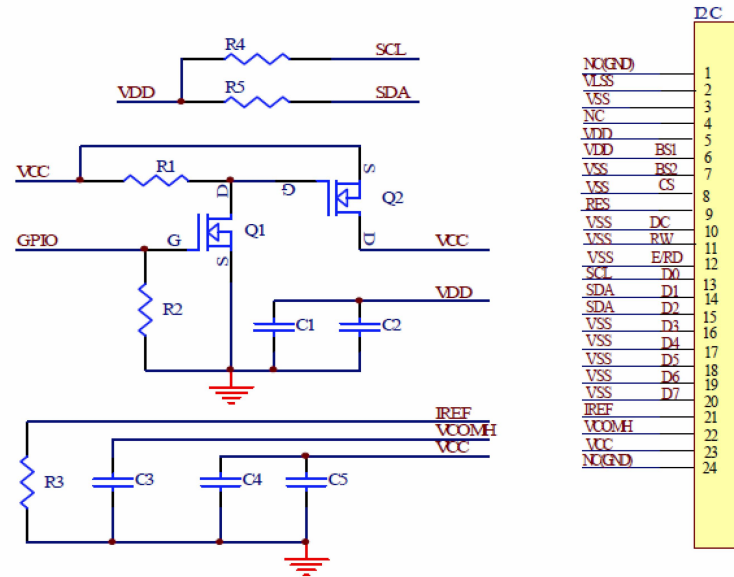
- C1, C2: 1 $\mu$ F / 16V, X5R
- C3: 2.2 $\mu$ F / 25V
- C4: 4.7 $\mu$ F / 25V, X7R
- C5: 0.1 $\mu$ F / 25V, X7R
- R1, R2: 47k $\Omega$
- R3: 910k $\Omega$ , R3 = (Voltage at IREF - VSS) / IREF
- Q2: FDN338P
- Q1: FDN335N

### Notes:

- VDD: 1.65V~3.3V
- VCC\_IN: 11.5~12.5V

## 9.3 Application circuit for IIC mode

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



#### Recommended Components:

- C1, C2: 1 $\mu$ F / 16V, X5R
- C3: 2.2 $\mu$ F / 25V
- C4: 4.7 $\mu$ F / 25V, X7R
- C5: 0.1 $\mu$ F / 25V, X7R
- R1, R2: 47k $\Omega$
- R3: 910k $\Omega$ , R3 = (Voltage at IREF - VSS) / IREF
- R4, R5: 4.7k $\Omega$
- Q2: FDN338P
- Q1: FDN335N

#### Notes:

VDD: 1.65V~3.3V

VCC\_IN: 11.5~12.5V

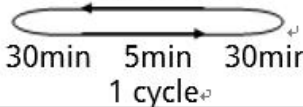
The I<sup>2</sup>C slave address is 0111100b'. If the customer ties D/C# to VDD, the I<sup>2</sup>C slave address will be 0111101b'.

## 10 Command Table

Please check in driver IC DATASHEET

## 11 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage	85°C	2

	temperature for a long time.	200hrs	
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 °C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40°C/85°C 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container.

## 12 Warranty and Conditions

<http://www.displaymodule.com/pages/faq> HYPERLINK

"http://www.displaymodule.com/pages/faq"