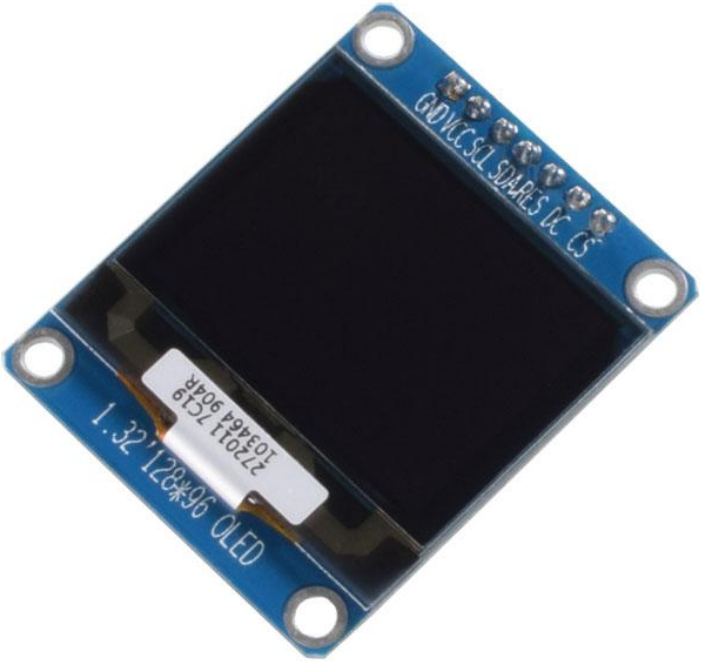
DisplayModule



DM-OLED132-645

1.32" 128 × 96 WHITE GRAPHIC OLED DISPLAY MOUDULE - SPI

Contents

1 Revision History

Date	Changes
2019-06-05	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.32	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome (White）	Colors
Resolution	128 x 96	pixel
Controller IC	SSD1327	-
Interface	4-wire SPI	-
Active Area	26.86 x 20.14	mm
Module Dimension	32.5 x 36.4 x 1.61	mm
Pixel Pitch	0.21 x 0.21	mm
Aperture Rate	82	%
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

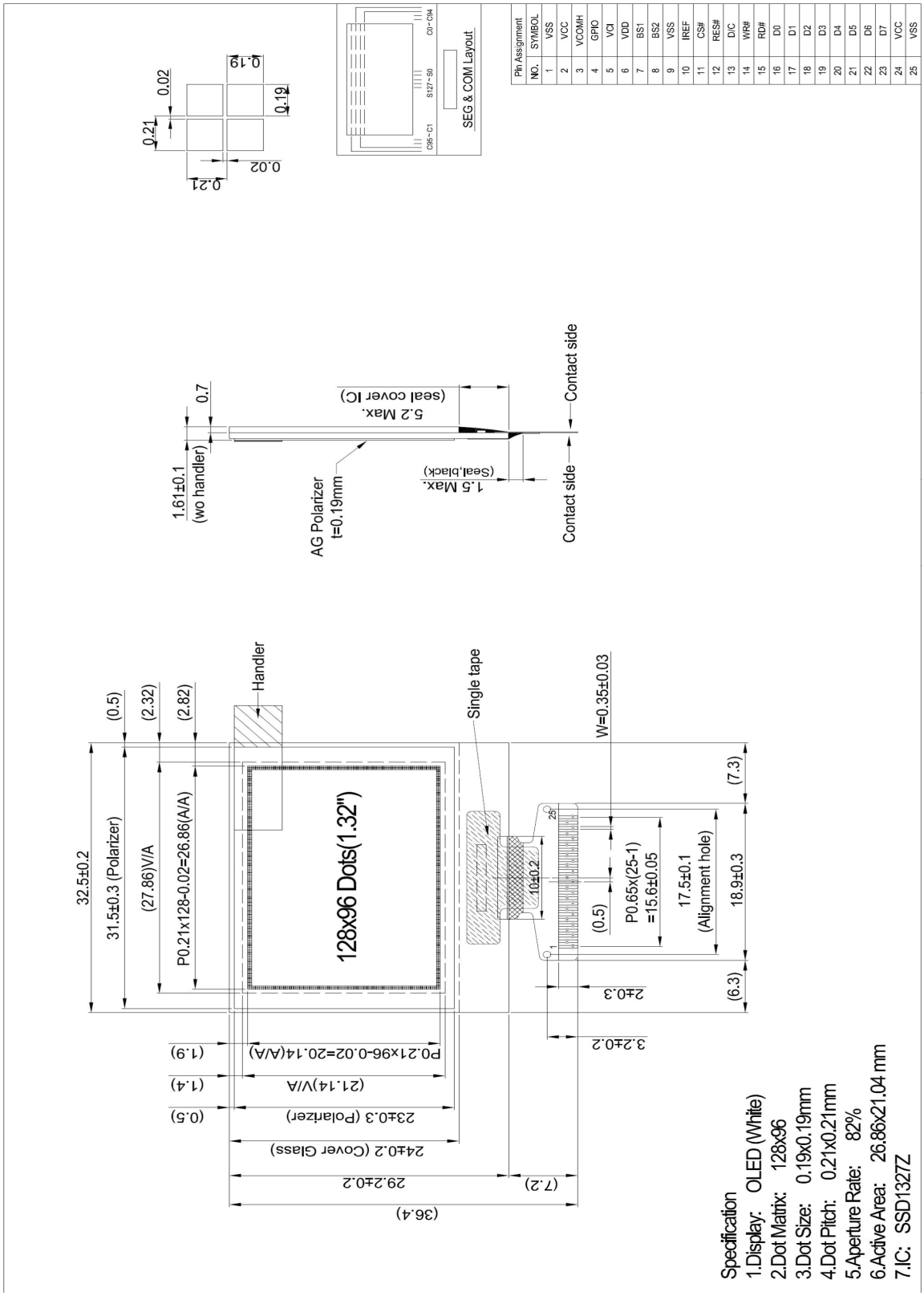
Pin No.	Symbol	Function Description
1	VSS	Ground.
2	VCC	Power supply for analog circuit.
3	VCOMH	Com Voltage Output. A capacitor should be connected between this pin and VSS.
4	GPIO	General I/O port.
5	VCI	Power supply for logic circuit.
6	VDD	A capacitor should be connected between this pin and VSS.
7	BS1	Interface selection input.
8	BS2	Interface selection input.
9	VSS	Ground.
10	IREF	Reference current input pin. A resistor should be connected between this pin and VSS.
11	CS#	Chip select input.
12	RES#	Reset signal input. When it's low, initialization of SSD1327 is executed.
13	D/C	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
14	WR#	This pin is used to receive the write data signal.
15	RD#	This pin is used to receive the read data signal.
16	D0	Data bus (for parallel interface)
17	D1	Data bus (for parallel interface)
18	D2	Data bus (for parallel interface)
19	D3	Data bus (for parallel interface)
20	D4	Data bus (for parallel interface)
21	D5	Data bus (for parallel interface)
22	D6	Data bus (for parallel interface)
23	D7	Data bus (for parallel interface)
24	VCC	Power supply for analog circuit.
25	VSS	Ground.

3.2 Module Pin Description

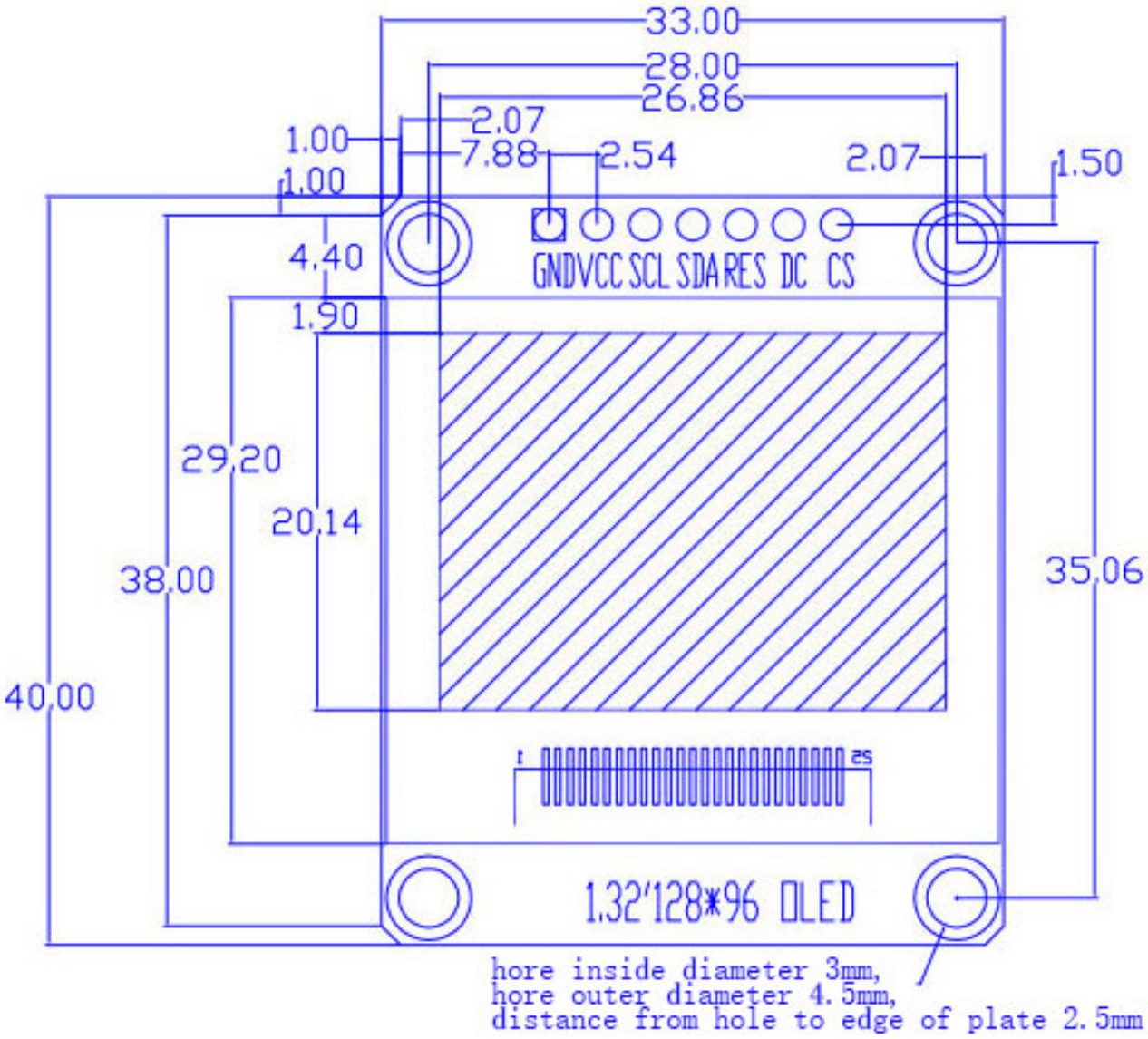
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC_IN	Power Supply 3.3V
3	SCL	SPI Clock
4	SDA	SPI DATA
5	RES	OLED reset Pin.
6	D/C	Data/Command Control This pin is Data/Command control pin.
7	CS	Chip Select This pin is pulled low to active. Connect to ground if no used .

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles		160	-	-	°	
C.I.E. (White)	(x) (y)	0.24 0.28	0.28 0.32	0.32 0.36		CIE1931
Pixel Luminance		80	100	-	cd/m²	
Standby Luminance		-	10	-	cd/m²	
Dark room Contrast Ratio	CR	-	2000:1	-		
Normal mode current consumption		-	25.5	27.5	mA	All pixels on
Standby mode current consumption		-	1	2	mA	Standby mode 10% pixels on
Normal mode power consumption		-	382.5	412.5	mW	All pixels on
Standby mode power consumption		-	15	30	mW	Standby mode 10% pixels on
Response Time			10		µs	

Normal mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x5f
- Frame rate : 105Hz
- Duty setting : 1/96

Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x0a
- Frame rate : 105Hz
- Duty setting : 1/96

5.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit	Remark
Operation Supply Voltage for panel	V_{CI}	Ta = 25℃	-0.3	4	V	IC maximum rating
Logic Supply Voltage for panel	V_{DD}		-0.5	2.75	V	
Display Supply Voltage for panel	V_{CC}	Ta = 25℃	-0.5	16	V	IC maximum rating
Display Supply Voltage for module	V_{CC_IN}		2.6	3.5	V	
Operating Temperature	T_{OP}		-40	70	℃	
Storage Temperature	T_{STG}		-40	85	℃	
Humidity				85	%	
Life Time		100 cd/m^2,50% checkerboard	13,000	-	hour	Note (1)
Life Time		80 cd/m^2,50% checkerboard	16,000	-	hour	Note (2)

Note:

(A) Under V_{CC} = 15V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m2 :

- Contrast setting : 0x5f
- Frame rate : 105Hz
- Duty setting : 1/96

(2) Setting of 80 cd/m2 :

- Contrast setting : 0x4f
- Frame rate : 105Hz
- Duty setting : 1/96

5.3 DC Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Operation Supply Voltage for panel	V_{CI}		2.6	-	3.5	V
Logic Supply Voltage for panel	V_{DD}		1.65	-	2.6	V
Display Supply Voltage for panel	V_{CC}		14.5	15	15.5	V
Display Supply Voltage for module	V_{CC_IN}		-	3.3	3.5	V
Operating Current V_{CI}	I_{CI}	V_{CI} = 3.5V, V_{CC} = 18V, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	35	50	µA
			Internal V_{DD} = 2.5V	95	120	
Operating Current V_{CC}	I_{CC}	V_{CI} = 3.5V, V_{CC} = 18V, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	600	750	µA
			Internal V_{DD} = 2.5V	600	750	mA
Segment output current Setting V_{CC} =18V, IREF=10uA	I_{SEG}	Contrast=FF	-	300	370	µA
		Contrast=AF	-	206	-	µA
		Contrast=7F	-	150	-	µA
		Contrast=3F	-	75	-	µA
		Contrast=1F	-	37.5	-	µA
Low Level Input Voltage	V_{IL}	I_{out}=100µA	0	-	0.2 x V_{CI}	V
High Level Input Voltage	V_{IH}	I_{out}=100µA	0.8 x V_{CI}	-	V_{CI}	V
Low Level Output Voltage	V_{OL}	I_{out}=100µA	0	-	0.1 x V_{CI}	V
High Level Output Voltage	V_{OH}	I_{out}=100µA	0.9 x V_{CI}	-	V_{CI}	V

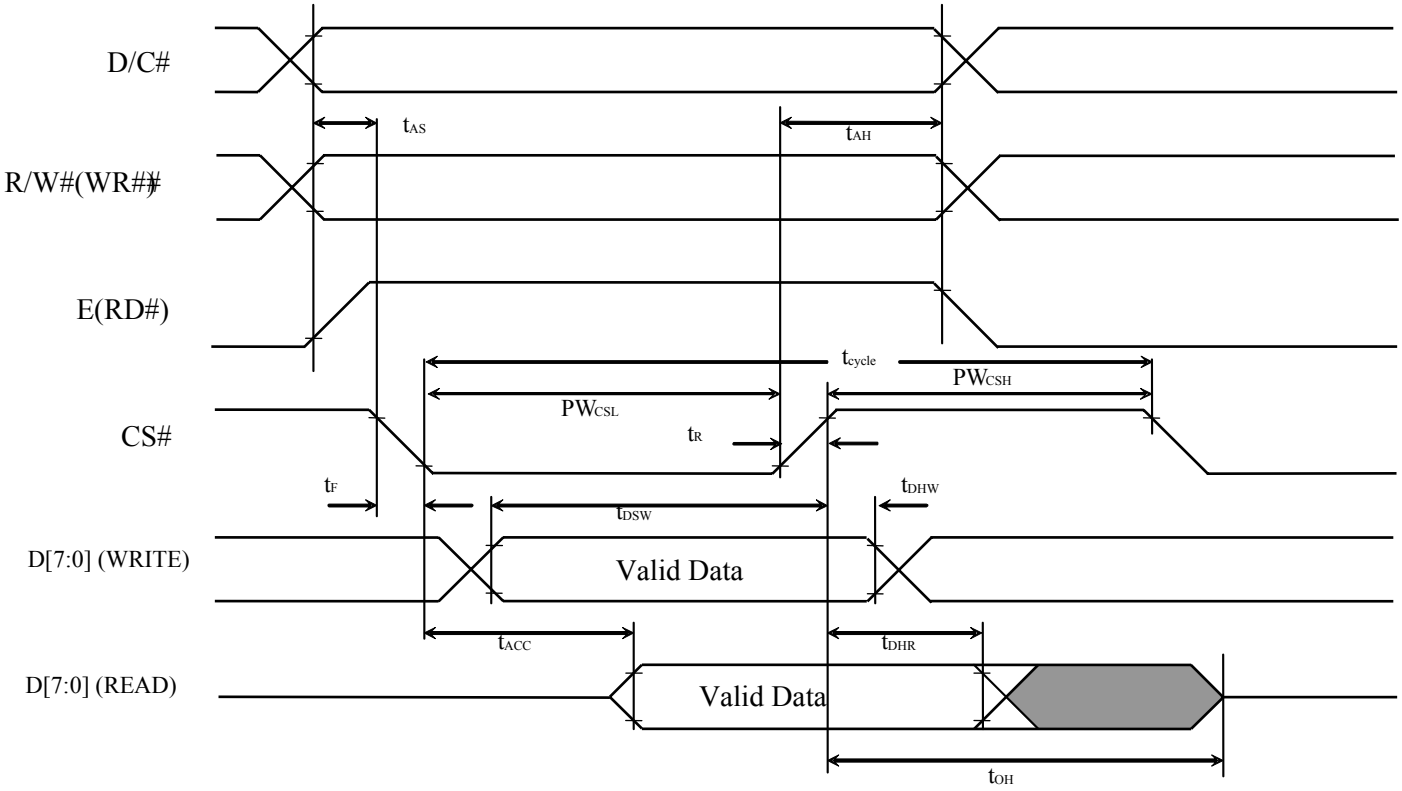
5.4 AC Characteristics

5.4.1 6800-series MCU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{CI} -V_{SS} = 1.65V to 3.3V, Ta = 25°C)

Figure 5-1 : 6800-series MCU parallel interface characteristics

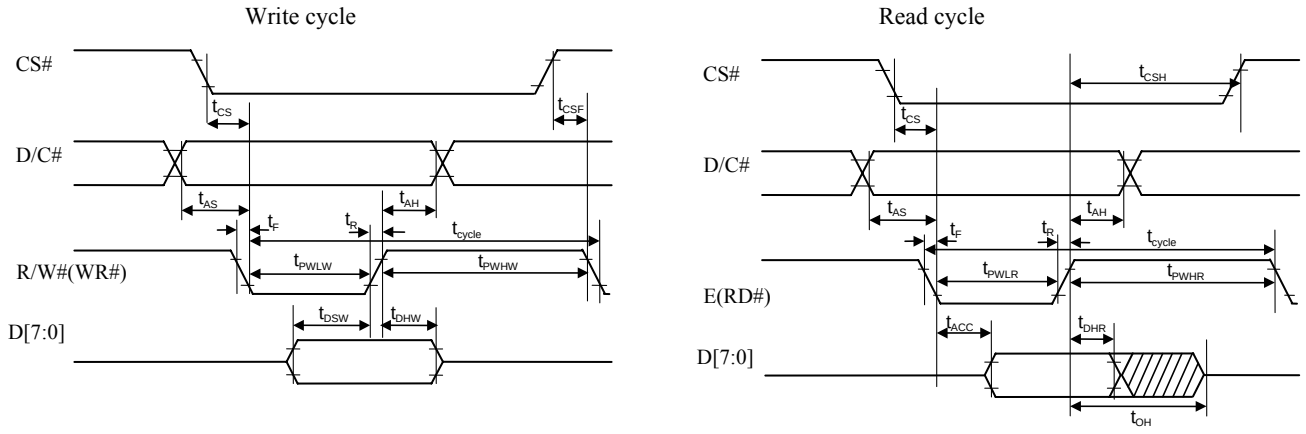


5.4.2 8080-Series MCU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns
t_{CS}	Chip select setup time	0	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	ns
t_{CSF}	Chip select hold time	20	-	ns

* (V_{CI} -V_{SS} = 1 65V to 3 3V Ta = 25°C)

Figure 5-2 : 8080-series MCU parallel interface characteristics

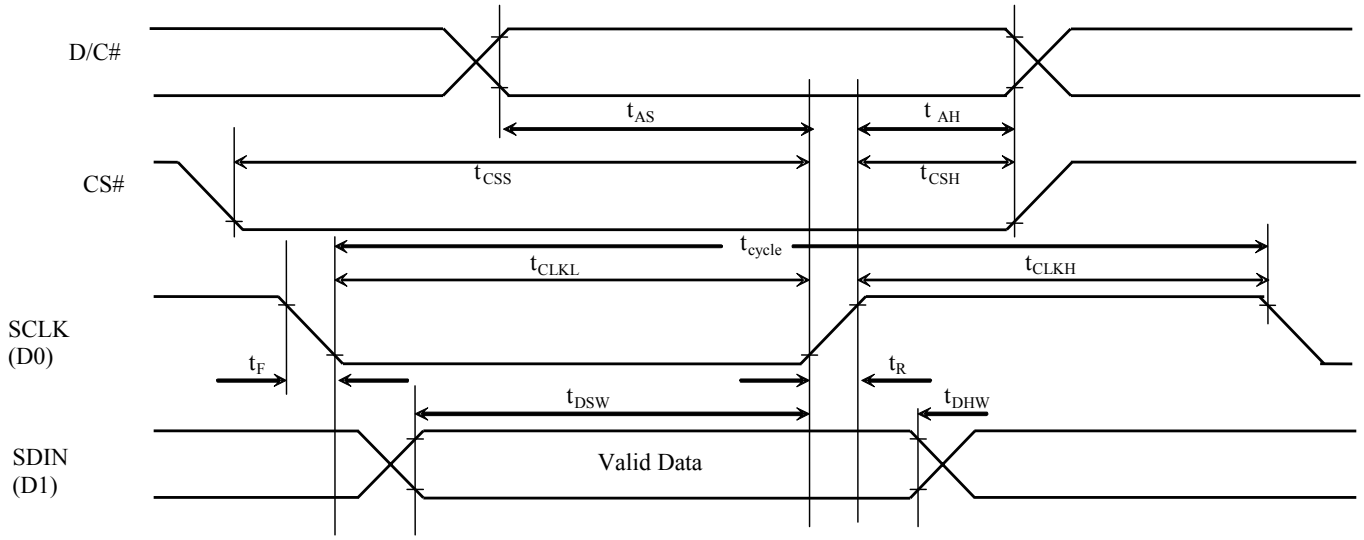


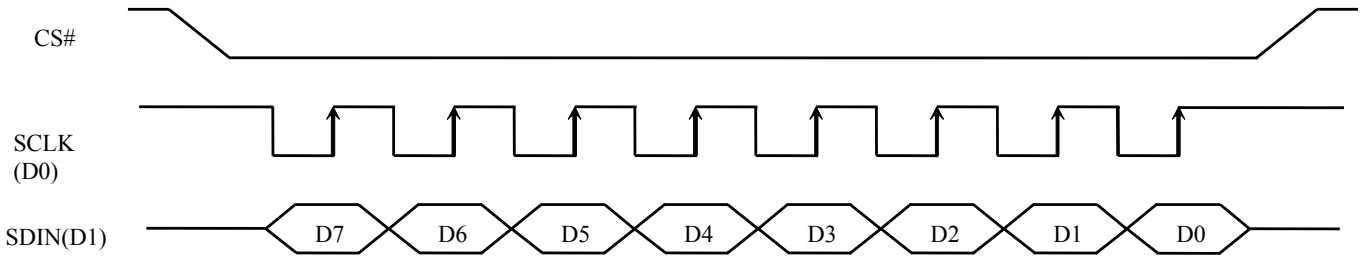
5.4.3 Serial Interface Timing Characteristics:4-wire Serial(default)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{CI} -V_{SS} = 1.65V to 3.3V, Ta = 25°C)

Figure 5-3 : Serial interface characteristics (4-wire SPI)



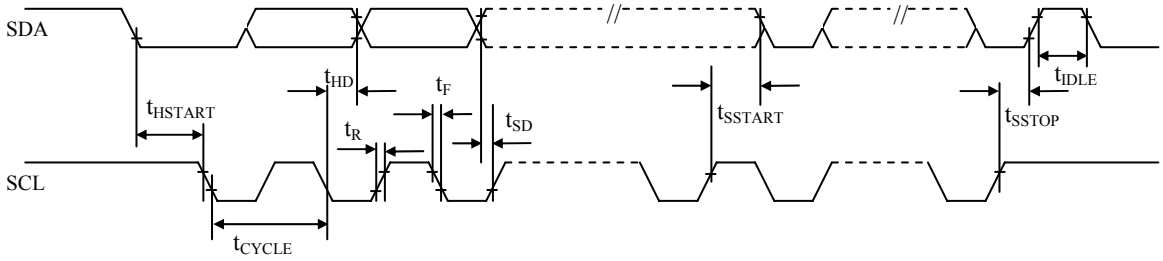


5.4.4 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	ns
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	us
t_R	Rise Time	-	300	ns
t_F	Fall Time	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3		us

* (V_{CI} -V_{SS} = 1.65V to 3.3V, Ta = 25°C)

Figure 5-5: I²C interface Timing characteristics



6 Power ON/OFF Timing Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1327 (assume internal V_{DD} is used).

Power ON sequence:

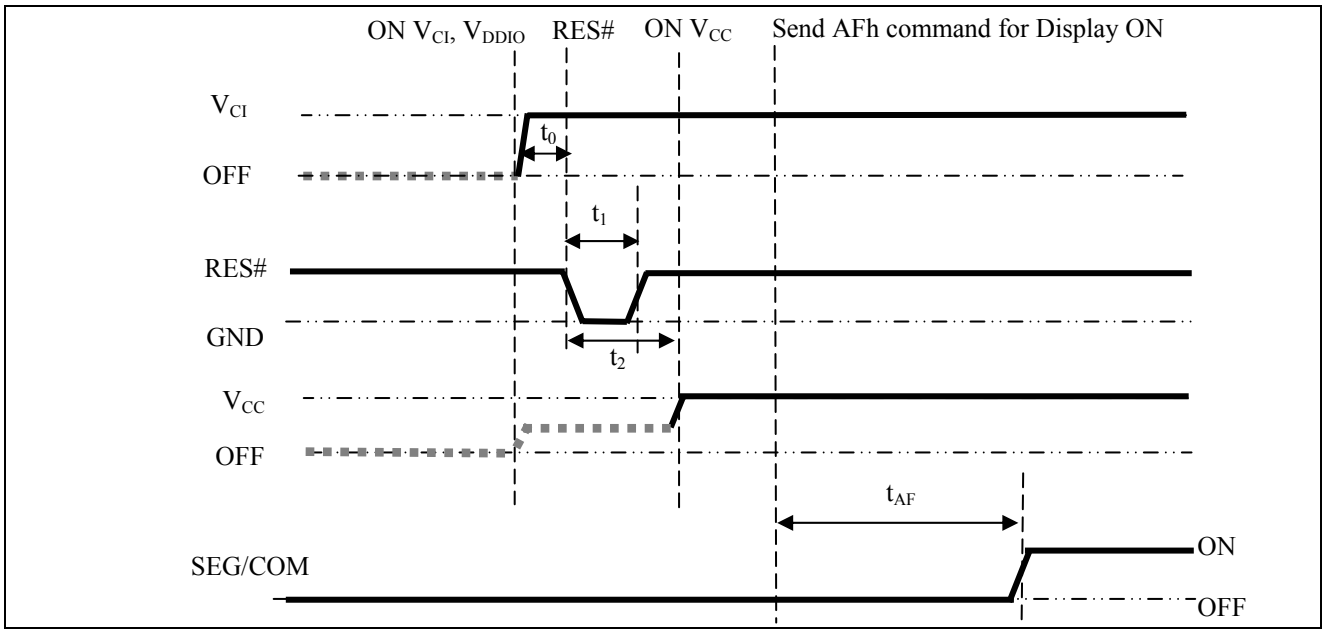
1.Power ON V_{CI}.

2.After V_{CI} becomes stable, set wait time at least 1ms (t0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) [4] and then HIGH (logic high).

3.After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.[1]

4.After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).

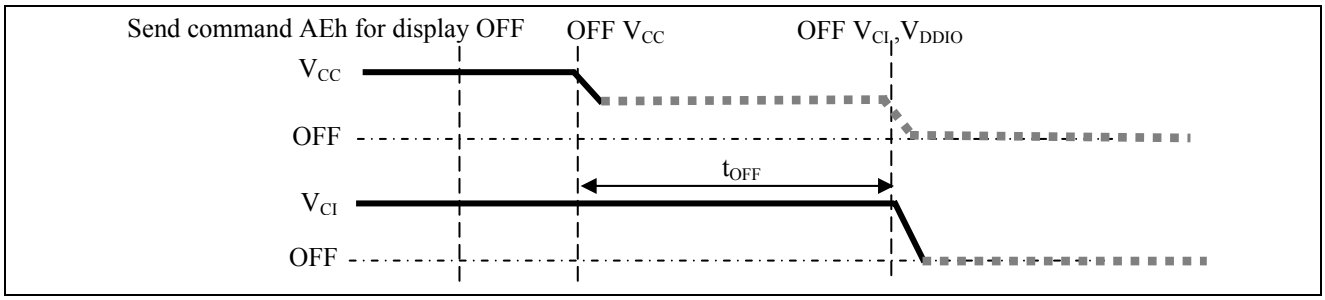
Figure 6-1 : The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2],[3]
3. Wait for t_{OFF}. Power OFF V_{CI}. (where Minimum t_{OFF}=0ms[5], Typical t_{OFF}=100ms)

Figure 6-2 : The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 6-1 and Figure 6-2.

(2) V_{CC} should be kept float (disable) when it is OFF.

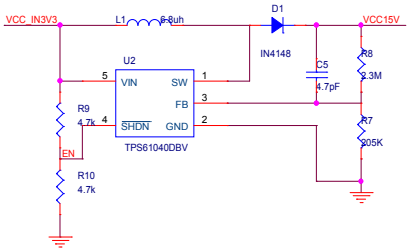
(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

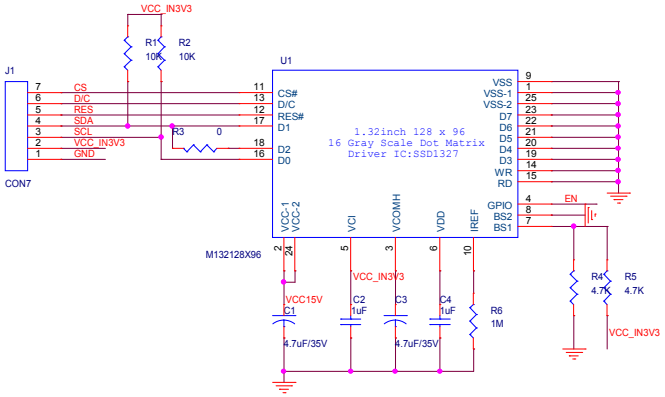
(5) V_{CI} should not be Power OFF before V_{CC} Power OFF.

7 Module Schematic

interface I2C/SPI(default)
1.GND=Ground
2.VCC_IN=3.3V
3.SCL=SPI Clock When I2C communication, it is the I2C clock line
4.SDA=SPI data When I2C communication, it is the I2C data line
5.RES=OLED reset
6.DC=OLED SPI Data/Commandcontrol pin (When I2C communication, is the I2C address control line)
7.CS=OLED SPI Chip Select(When I2C communication,CS needs to be grounded)



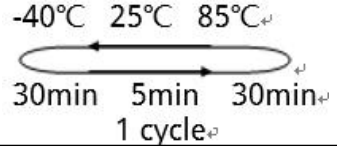
When EN is low the booster circuit can be closed.
Default R10 is not welded



I2C communication, R3 needs welding;
SPI communication, R3 doesn't need welding

SPI/IIC setting
SPI:R4 weld R5 R3 vacant
IIC:R5 R3 weld R4 vacant

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85℃ 120hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40℃ 120hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 120hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 ℃ 120hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	65℃,90%RH 120hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40℃/85℃ 100 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"