SeeYA 1.03”Micro-OLED（2560×2560RGB）

Model Name：SY103WAM01

Revision

Version	Date	Description
V0.0	2019.08.09	Initial release
V0.1	2020.01.21	Update general feature, optical characteristics and power sequence
V0.2	2020.04.08	Update Module Diagram and User Command
V0.3	2020.05.07	Update Module Diagram
V0.4	2020.06.17	Update optical characteristics and absolute maximum ratings, delete power consumption at different luminance level

Contents

1 General Description

This display is a 1.03 inch diagonal, 2560(RGB) × 2560 dots active matrix color OLED panel module based on single-crystal silicon transistors. This panel integrates panel driver and logic driver, and realizes small size, light weight, low power consumption and high resolution.
Applications: View finders, Head mounted displays, etc.

- 2560 * 2560 Real RGB Resolution
- AP Operated Resolution

  -- 2560 x 2560: (8*M, M=160~320) x RGB x (8*N, N=90~320)
- Frame rate: 2560x2560 up to 90Hz
- Normal operation supports full color mode: 16.7M colors
- Interface

  -- MIPII + I2C

  -- MIPI DPHY v1.2 with one / two port (4 / 8 lanes), 1.0Gbps/Lane

  -- MIPI DSI v1.01 R11 Video mode

  -- Support VESA-DSC v1.1 in-chip decoder (3X compression ratio)

  -- Support scaling up 1.33x (1920x1920 to 2560 x 2560) and 2x (1280x1280 to 2560 x 2560)
- Scan direction selection, up or down and right or left
- Orbit supported
- Wide range Brightness adjustment
- Sequential/Global emission
- Temperature compensation

2 General Feature

Parameter	Specification
Resolution	2560(H) x 2560 (V)
Number of dots	19.66M (2560x2560x3)
Pixel Size	7.2μm x 7.2μm
Pixel Arrangement	RGB π type
Useable Display Area	18.432mm x 18.432mm / 1.03'' diagonal
Luminance	1800cd/m² typical
Contrast Ratio	500,000:1 typical
Uniformity	> 85%
Operating Voltage	VDDI=1.8V AVDD=5V~6.5V(Suggest:6.3V) AVEE=-4V~-6V(Suggest:-4.5V) VDD=1.2V
Power Consumption	Total (1800nits,100%):1600mW
Gray Levels	256
Interface	MIPI (1 or 2-port D-PHY)
Frame Rate	60HZ~90HZ
Weight	TBD
Operating Temperature	-20°C to +70°C
Storage Temperature	-40°C to +80°C

3 Optical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Brightness[Note1]		1600	1800	2000	cd/m2
CR[Note2]	white to Black Contrast Ratio		500,000:1		
Uniformity [Note3]	End to end large-area uniformity	85			%
CIE Red	CIE-x		0.63		
	CIE-y		0.34		
CIE Green	CIE-x		0.25		
	CIE-y		0.67		
CIE Blue	CIE-x		0.15		
	CIE-y		0.07		
CIE White	CIE-x		0.313		
	CIE-y		0.329		
DCI-P3			85%		
View angle (White)	Color Shift (Δu’v’<0.02)	-30°		30°	
GL	Gray Levels Per Color		256		levels
FR	Refresh Rate	60		90	HZ
Power consumption@1800 nits,90Hz			1600		mW

Note1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the OLED screen. All input terminals OLED panel must be ground when measuring the center area of the panel;

Brightness is measured as peak luminance at full white pattern (Gray level=255);

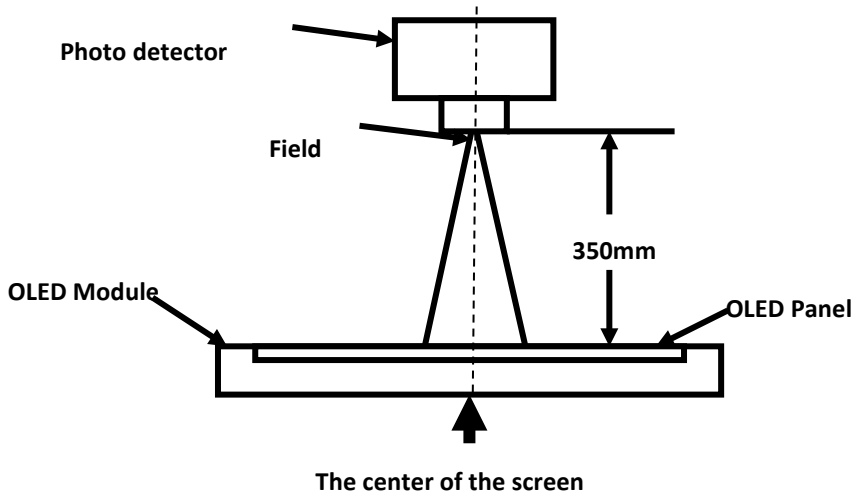


Fig. 1

Note2: Definition of CR (contrast ratio)

$$\text{Contrast ratio(CR)}=\frac{\text{Luminnace measured when OLED is on the "White" state}}{\text{Luminnace measured when OLED is on the "Black" state}}$$

"White state ": The state is that the OLED should be driven by Vwhite.

"Black state": The state is that the OLED should be driven by Vblack.

Note3: Definition of Uniformity at gray level 255 and at 1800 cd/m² luminance.

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length; W----- Active area width

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

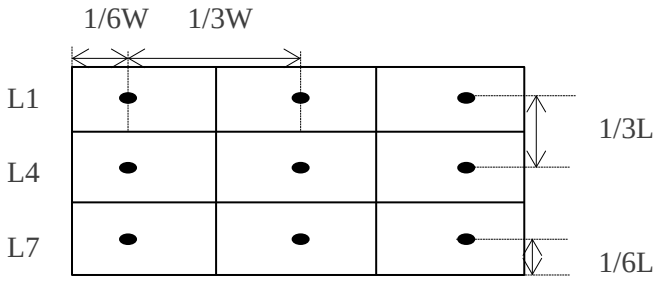


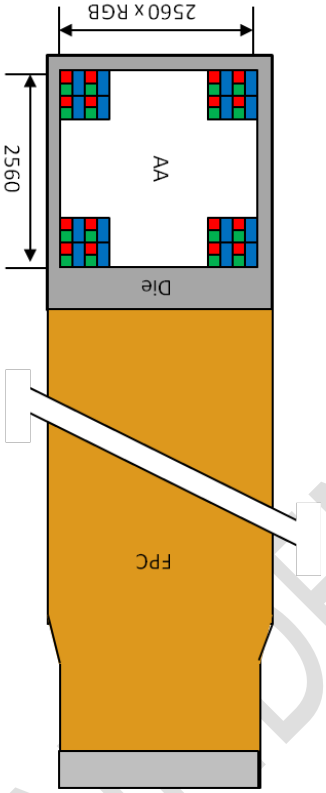
Fig. 2

Note4: Definition of Lifetime

Lifetime is measured at the center point of the module and at full white brightness (1800 cd/m²).

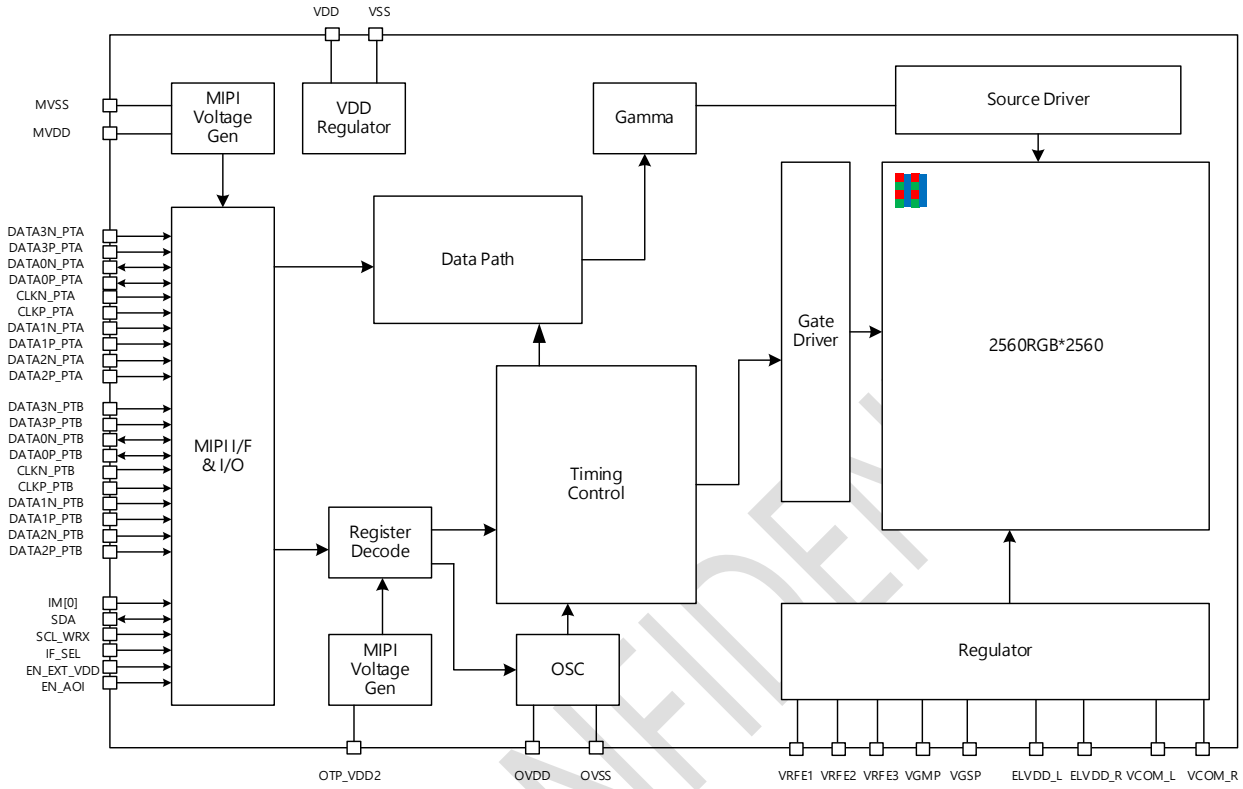
20% duty.

4 Pixel array

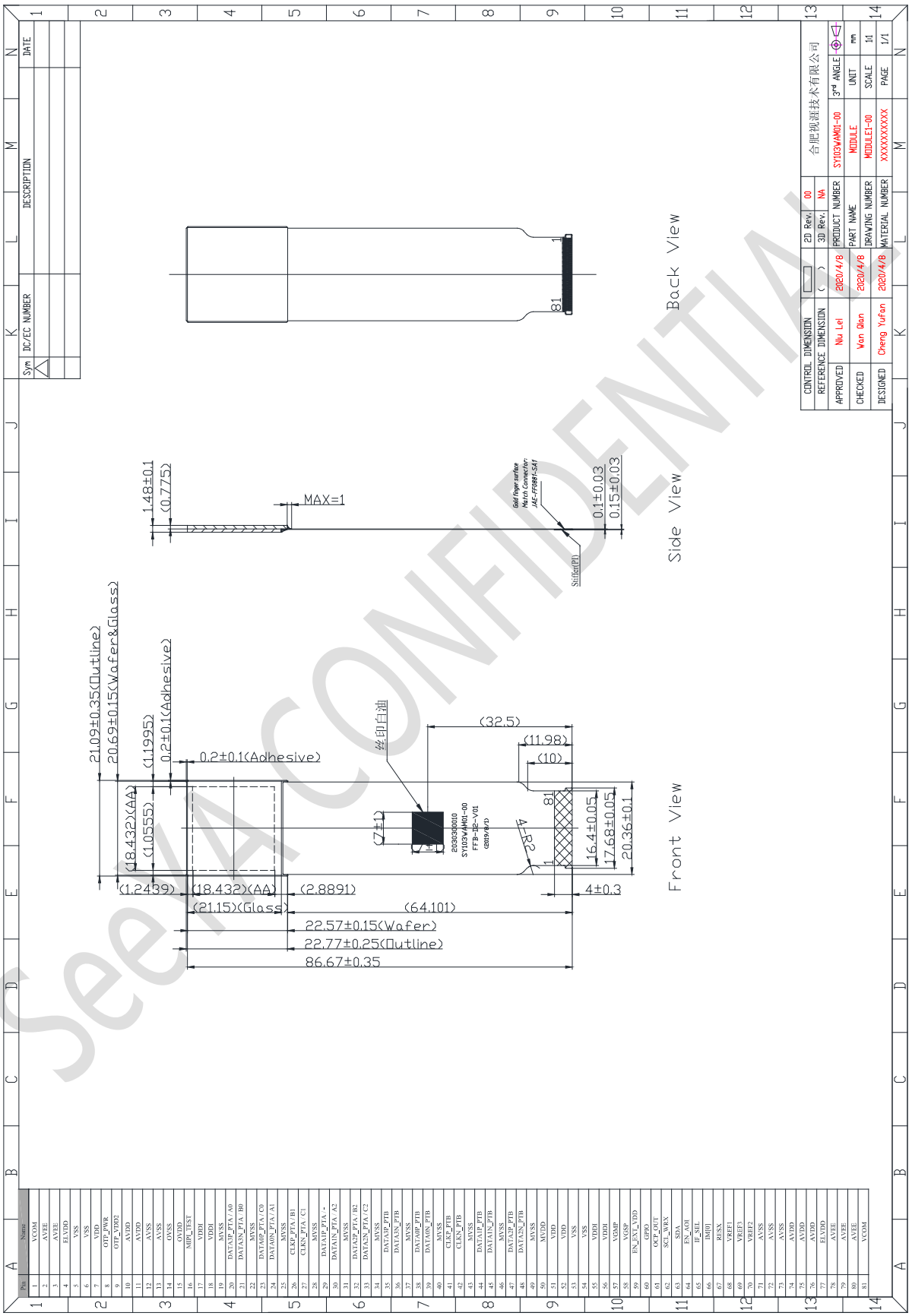


5 System block

System block diagram



6 Module Diagram



7 Pin Description

7.1 Pin Description

Pin No.	Symbol	Type	Description
1	VCOM	Output	Regulator output for common electrode voltage. connect a capacitor for stabilization, connect a TVS diode to GND.
2	AVEE	Power	-4.0V~-6.0V Power supply for OLED cell. connect a capacitor for stabilization.
3	AVEE	Power	-4.0V~-6.0V Power supply for OLED cell. then connect a capacitor for stabilization.
4	ELVDD	Power	Power supply for OLED cell. connect a capacitor for stabilization.
5	VSS	Power	System GND for internal digital system.
6	VSS	Power	System GND for internal digital system.
7	VDD	Power	Regulator output for logic system power. then connect a capacitor for stabilization. EN_EXT_VDD = 0: 3-power mode, VDD generated by internal regulator. EN_EXT_VDD = 1: 4-power mode, 1.2V VDD from external power IC.
8	OTP_PWR	Input	OTP program power. If not use, please connect to GND or OPEN.
9	OTP_VDD2	Output	Regulator output for MTP analog system power. Connect a capacitor for stabilization.
10	AVDD	Power	5V~6.5VPower supply for analog system. then connect a capacitor for stabilization.
11	AVDD	Power	5V~6.5VPower supply for analog system. then connect a capacitor for stabilization.
12	AVSS	Power	System GND for analog system.
13	AVSS	Power	System GND for analog system.
14	OVSS	Power	System GND for oscillator.
15	OVDD	Output	Regulator output for common electrode voltage. Connect a capacitor for stabilization.
16	MIPI_TEST	Input/ Output	Test pin for MIPI.
17	VDDI	Power	Power supply for interface system except for the interface.
18	VDDI	Power	Power supply for interface system except for the interface.
19	MVSS	Power	System GND for MIPI interface.
20	DATA3P_PTA	Input/Output	This pin is DSI D3+ signal if MIPI Port A interface is used. DATA3P/N_PTA is differential small amplitude signals. If not used, please keep it open.
21	DATA3N_PTA	Input/Output	This pin is DSI D3- signal if MIPI Port A interface is used. DATA3P/N_PTA is differential small amplitude signals. If not used, please keep it open.
22	MVSS	Power	System GND for MIPI interface.
23	DATA0P_PTA	Input/Output	This pin is DSI D0+ signal if MIPI Port A interface is used. DATA0P/N_PTA is differential small amplitude signals. If not used, please keep it open.
24	DATA0N_PTA	Input/Output	This pin is DSI D0- signal if MIPI Port A interface is used. DATA0P/N_PTA is differential small amplitude signals. If not used, please keep it open.
25	MVSS	Power	System GND for MIPI interface.
26	CLKP_PTA	Input	This pin is DSI CLK+ signal if MIPI Port A interface is used. CLKP/N_PTA is differential small amplitude signals. If not used, please keep it open.
27	CLKN_PTA	Input	This pin is DSI CLK- signal if MIPI Port A interface is used. CLKP/N_PTA is differential small amplitude signals. If not used, please keep it open.
28	MVSS	Power	System GND for MIPI interface.
29	DATA1P_PTA	Input/Output	This pin is DSI D1+ signal if MIPI Port A interface is used. DATA1P/N_PTA is differential small amplitude signals. If not used, please keep it open.

30	DATA1N_PTA	Input/Output	This pin is DSI D1- signal if MIPI Port A interface is used. DATA1P/N_PTA is differential small amplitude signals. If not used, please keep it open.
31	MVSS	Power	System GND for MIPI interface.
32	DATA2P_PTA	Input/Output	This pin is DSI D2+ signal if MIPI Port A interface is used. DATA2P/N_PTA is differential small amplitude signals. If not used, please keep it open.
33	DATA2N_PTA	Input/Output	This pin is DSI D2- signal if MIPI Port A interface is used. DATA2P/N_PTA is differential small amplitude signals. If not used, please keep it open.
34	MVSS	Power	System GND for MIPI interface.
35	DATA3P_PTB	Input/Output	This pin is DSI D3+ signal if MIPI Port B interface is used. DATA3P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
36	DATA3N_PTB	Input/Output	This pin is DSI D3- signal if MIPI Port B interface is used. DATA3P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
37	MVSS	Power	System GND for MIPI interface.
38	DATA0P_PTB	Input/Output	This pin is DSI D0+ signal if MIPI Port B interface is used. DATA0P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
39	DATA0N_PTB	Input/Output	This pin is DSI D0- signal if MIPI Port B interface is used. DATA0P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
40	MVSS	Power	System GND for MIPI interface.
41	CLKP_PTB	Input	This pin is DSI CLK+ signal if MIPI Port B interface is used. CLKP/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
42	CLKN_PTB	Input	This pin is DSI CLK- signal if MIPI Port B interface is used. CLKP/N_PTB is differential small amplitude signals. If not used, please keep it open.
43	MVSS	Power	System GND for MIPI interface.
44	DATA1P_PTB	Input/ Output	This pin is DSI D1+ signal if MIPI Port B interface is used. DATA1P/N_PTB is differential small amplitude signals. If not used, please keep it open.
45	DATA1N_PTB	Power	This pin is DSI D1- signal if MIPI Port B interface is used. DATA1P/N_PTB is differential small amplitude signals. If not used, please keep it open.
46	MVSS	Input/ Output	System GND for MIPI interface.
47	DATA2P_PTB	Input/ Output	This pin is DSI D2+ signal if MIPI Port B interface is used. DATA2P/N_PTB is differential small amplitude signals. If not used, please keep it open.
48	DATA2N_PTB	Input/ Output	This pin is DSI D2- signal if MIPI Port B interface is used. DATA2P/N_PTB is differential small amplitude signals. If not used, please keep it open.
49	MVSS	Power	System GND for MIPI interface.
50	MVDD	Output	Regulator output for MIPI digital system power. Connect a capacitor for stabilization.
51	VDD	Power	Regulator output for logic system power. then connect a capacitor for stabilization. EN_EXT_VDD = 0: 3-power mode, VDD generated by internal regulator. EN_EXT_VDD = 1: 4-power mode, 1.2V VDD from external power IC.
52	VDD	Power	Regulator output for logic system power. then connect a capacitor for stabilization. EN_EXT_VDD = 0: 3-power mode, VDD generated by internal regulator. EN_EXT_VDD = 1: 4-power mode, 1.2V VDD from external power IC.
53	VSS	Power	System GND for internal digital system.
54	VSS	Power	System GND for internal digital system.
55	VDDI	Power	power supply for interface system except for MIPI interface.
56	VDDI	Power	power supply for interface system except for MIPI interface.
57	VGMP	Output	Regulator output for gamma high voltage generation. Connect a capacitor for stabilization.
58	VGSP	Output	Regulator output for gamma low voltage generation. Connect a capacitor for stabilization.

<table>
<tr><td>59</td><td>EN_EXT_VDD</td><td>Input</td><td>Enable signal for external VDD power mode
EN_EXT_VDD = 0 : internal VDD, EN_EXT_VDD = 1: external VDD</td></tr>
<tr><td>60</td><td>GPIO</td><td>Output</td><td>Digital global purpose in/out test pin</td></tr>
<tr><td>61</td><td>OCP_OUT</td><td>Output</td><td>Over current protect output flag.</td></tr>
<tr><td>62</td><td>SCL_WRX</td><td>Input/
Output</td><td>Synchronous clock signal in I2C I/F.
If this pin is not used, please connect to VDDI.</td></tr>
<tr><td>63</td><td>SDA</td><td>Input/
Output</td><td>Bi-direction data PIN in I2C I/F.
If this pin is not used, please connect to VDDI.</td></tr>
<tr><td>64</td><td>EN_AOI</td><td>Input</td><td>AOI mode enable.
EN_AOI =0, AOI mode disable, EN_AOI =1, AOI mode enable</td></tr>
<tr><td>65</td><td>IF_SEL</td><td>Input</td><td>C/D PHY I/F selection (0:DPHY, 1: CPHY)</td></tr>
<tr><td>66</td><td>IM[0]</td><td>Input</td><td>Use to select the Interface type.
<table>
<tr><th>IM [0]</th><th>Command Execute</th><th>Image Write</th></tr>
<tr><td>0</td><td>MIPI</td><td>MIPI</td></tr>
<tr><td>1</td><td>I2C</td><td>MIPI</td></tr>
</table>
Note1: MIPI 1port or 2port is selected by register setting.
Note2: PSWAP/DSWAP [1:0] is set by register.

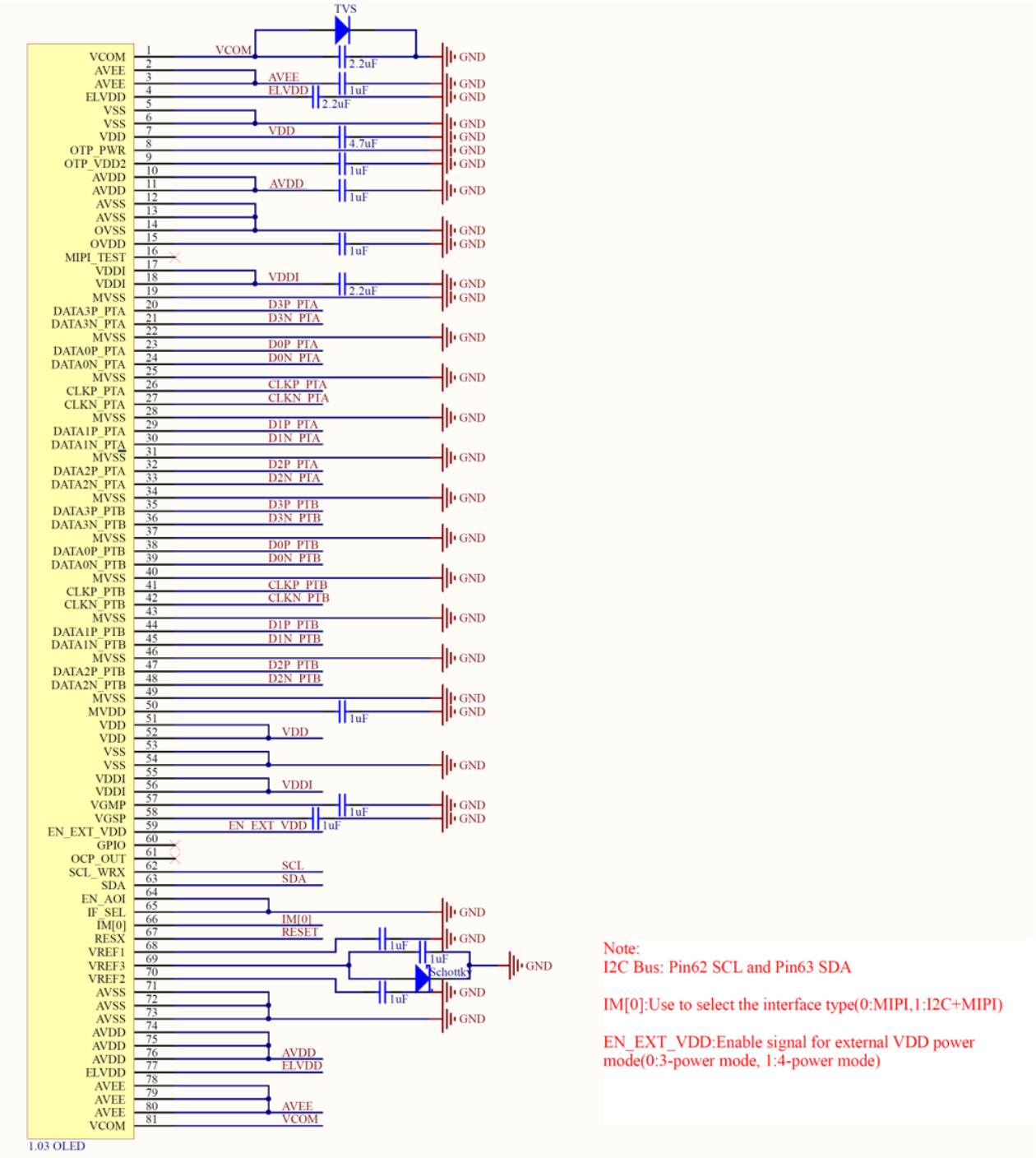
IF_SEL=0 :
<table>
<tr><td rowspan="2">PSWAP</td><td rowspan="2">DSWAP[1:0]</td><td colspan="10">DPHY</td></tr>
<tr><td>DATA3P</td><td>DATA3N</td><td>DATA0P</td><td>DATA0N</td><td>CLKP</td><td>CLKN</td><td>DATA1P</td><td>DATA1N</td><td>DATA2P</td><td>DATA2N</td></tr>
<tr><td rowspan="4">0</td><td>00</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr>
<tr><td>01</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>10</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>11</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr>
<tr><td rowspan="4">1</td><td>00</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr>
<tr><td>01</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr>
<tr><td>10</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>11</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr>
</table>
IF_SEL=1:
<table>
<tr><td rowspan="2">PSWAP</td><td rowspan="2">DSWAP[1:0]</td><td colspan="11">C-PHY</td></tr>
<tr><td>A0</td><td>B0</td><td>C0</td><td>A1</td><td>B1</td><td>C1</td><td>X</td><td>A2</td><td>B2</td><td>C2</td></tr>
<tr><td rowspan="4">0</td><td>00</td><td>A0</td><td>B0</td><td>C0</td><td>A1</td><td>B1</td><td>C1</td><td>X</td><td>A2</td><td>B2</td><td>C2</td></tr>
<tr><td>01</td><td>A0</td><td>B0</td><td>C0</td><td>A2</td><td>B2</td><td>C2</td><td>X</td><td>A1</td><td>B1</td><td>C1</td></tr>
<tr><td>10</td><td>A2</td><td>B2</td><td>C2</td><td>A1</td><td>B1</td><td>C1</td><td>X</td><td>A0</td><td>B0</td><td>C0</td></tr>
<tr><td>11</td><td>A1</td><td>B1</td><td>C1</td><td>A0</td><td>B0</td><td>C0</td><td>X</td><td>A2</td><td>B2</td><td>C2</td></tr>
<tr><td rowspan="4">1</td><td>00</td><td>C0</td><td>B0</td><td>A0</td><td>C1</td><td>B1</td><td>A1</td><td>X</td><td>C2</td><td>B2</td><td>A2</td></tr>
<tr><td>01</td><td>C0</td><td>B0</td><td>A0</td><td>C2</td><td>B2</td><td>A2</td><td>X</td><td>C1</td><td>B1</td><td>A1</td></tr>
<tr><td>10</td><td>C2</td><td>B2</td><td>A2</td><td>C1</td><td>B1</td><td>A1</td><td>X</td><td>C0</td><td>B0</td><td>A0</td></tr>
<tr><td>11</td><td>C1</td><td>B1</td><td>A1</td><td>C0</td><td>B0</td><td>A0</td><td>X</td><td>C2</td><td>B2</td><td>A2</td></tr>
</table></td></tr>
<tr><td>67</td><td>RESX</td><td>Input</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>68</td><td>VREF1</td><td>Output</td><td>Regulator output for internal reference voltage.
Connect a capacitor for stabilization.</td></tr>
<tr><td>69</td><td>VREF3</td><td>Output</td><td>Regulator output for internal reference voltage.
Connect a capacitor for stabilization.
Connect a Schottky diode to GND</td></tr>
<tr><td>70</td><td>VREF2</td><td>Output</td><td>Regulator output for internal reference voltage.
Connect a capacitor for stabilization.</td></tr>
<tr><td>71</td><td>AVSS</td><td>Power</td><td>System GND for analog system.</td></tr>
<tr><td>72</td><td>AVSS</td><td>Power</td><td>System GND for analog system.</td></tr>
<tr><td>73</td><td>AVSS</td><td>Power</td><td>System GND for analog system.</td></tr>
<tr><td>74</td><td>AVDD</td><td>Power</td><td>5V~6.5VPower supply for analog system.
connect a capacitor for stabilization.</td></tr>
<tr><td>75</td><td>AVDD</td><td>Power</td><td>5V~6.5VPower supply for analog system.
connect a capacitor for stabilization.</td></tr>
<tr><td>76</td><td>AVDD</td><td>Power</td><td>5V~6.5VPower supply for analog system.
connect a capacitor for stabilization.</td></tr>
<tr><td>77</td><td>ELVDD</td><td>Power</td><td>Power supply for OLED cell.
connect a capacitor for stabilization.</td></tr>
<tr><td>78</td><td>AVEE</td><td>Power</td><td>-4.0V~-6.0V Power supply for OLED cell.
connect a capacitor for stabilization.</td></tr>
<tr><td>79</td><td>AVEE</td><td>Power</td><td>-4.0V~-6.0V Power supply for OLED cell.
connect a capacitor for stabilization.</td></tr>
<tr><td>80</td><td>AVEE</td><td>Power</td><td>-4.0V~-6.0V Power supply for OLED cell.
connect a capacitor for stabilization.</td></tr>
<tr><td>81</td><td>VCOM</td><td>Output</td><td>Regulator output for common electrode voltage.
connect a capacitor for stabilization, connect a TVS diode to GND.</td></tr>
</table>

7.2 Application circuit

Below table is the instruction of peripheral circuit. Regarding power supply capacitor connections, mount an appropriate capacitor for each power supply.

No.	Signal Name	Typical Value	Maximum Rated Voltage	Note
1	VDDI	Cap, 2.2uF	6.3V	-
2	AVDD	Cap, 1.0uF	10V	-
3	ELVDD	Cap, 2.2uF	10V	-
4	AVEE	Cap, 1uF	10V	-
5	VDD	Cap, 4.7uF	6.3V	-
6	MVDD	Cap, 1uF	6.3V	-
7	VGMP	Cap, 1uF	10V	-
8	VGSP	Cap, 1uF	10V	-
9	VREF1	Cap, 1uF	6.3V	-
10	VREF2	Cap, 1uF	6.3V	-
11	VREF3	Cap, 1uF Schottky Diode	6.3V	
12	VCOM	Cap, 2.2uF TVS	10V	Recommend: TVS VBR min>8V
13	OTP_VDD2	Cap, 1uF	6.3V	-
14	OVDD	Cap, 1uF	6.3V	-

Below circuit is one of typical example for reference to drive the module with D-PHY.



8 Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When this Micro-OLED product is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use this Micro-OLED product within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, this Micro-OLED product will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage (1)	VDDI	5.5	V
Power Supply Voltage (2)	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
Power Supply Voltage in AOI mode	VDDI	1.32	V
	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
MIPI Differential Input	CLKP_PTA/B, CLKN_PTA/B DATAP0_PTA/B, DATAN0_PTA/B DATAP1_PTA/B, DATAN1_PTA/B DATAP2_PTA/B, DATAN2_PTA/B DATAP3_PTA/B, DATAN3_PTA/B	1.32	V
Input Voltage of Interface	Vin	-0.3 ~ VDDI+0.3	V
Output Voltage of Interface	Vo	-0.3 ~ VDDI+0.3	V
Operating temperature	Topr	-20 ~ 70	°C
Storage temperature	Tstg	-40 ~ 80	°C

8.2 DC Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage						
AVDD Input Level	AVDD	-	5.0		6.5	V
Digital I/O Power Supply (non-MIPI I/O)	VDDI	-		1.8		V
Digital I/O Input Level @Logic High	VIH	VDDI=1.65V ~ 1.95V	0.7*VDDI	-	VDDI	V
Digital I/O Input Level @Logic Low	VIL	VDDI=1.65V ~ 1.95V	0	-	0.3*VDDI	V
Digital I/O Output Level @Logic High	VOH	Iout = -1mA	0.8*VDDI	-	VDDI	V
Digital I/O Output Level @Logic Low	VOL	Iout = +1mA	0	-	0.2*VDDI	V
Digital I/O Input leakage @Logic High	IIHD	Vin = VDDI			1	uA
Digital I/O Input leakage @Logic Low	IILD	Vin = 0	-1			uA
MIPI I/O Power Supply	MVDD	-	-	1.2	-	V
MIPI Input leakage @Logic High	IIHMD	Vin = MVDD			1	uA
MIPI Input leakage @Logic Low	IILMD	Vin = 0	-1			uA
Panel Reference Voltage	VCOM	-	-1	-	-5.5	V
Source Driver						

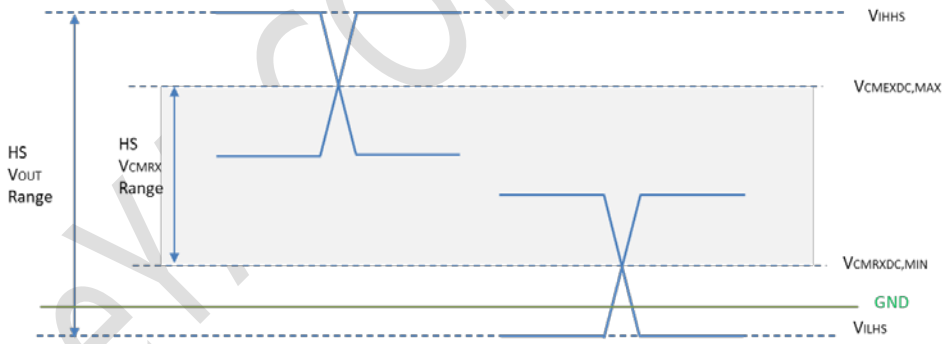
Gamma Reference Voltage	VGMP		4		5.5	V
	VGSP		0.3		2	V
Source Output Deviation (Positive output)	VDEV,POS	AVDD-1.2V<Sout≤AVDD-0.6V		TBD		mV
		1.2V ≤ Sout ≤ AVDD-1.2V		TBD		mV
Source Output Offset	VOFSET	AVDD-1.2V<Sout≤AVDD-0.6V		TBD		mV
		1.2V ≤ Sout ≤ AVDD-1.2V		TBD		mV

8.3 DSI DC/AC Characteristic

8.3.1 Receiver characteristic

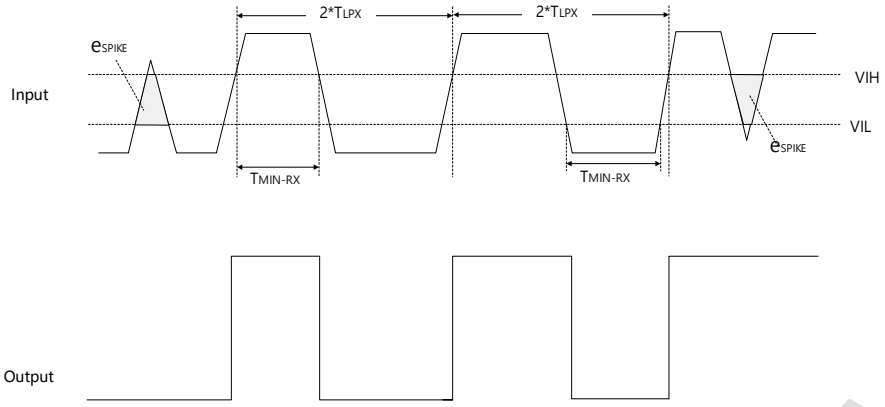
High speed receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	-	330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IDTH}	Differential input high threshold	-	-	70	mV
V_{IDTL}	Differential input low threshold	-70	-	-	mV
V_{IHHS}	Single-ended input high voltage	-	-	460	mV
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV
C_{CM}	Common-mode termination	-	-	60	pF



Low power receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
V_{IH}	Logic 1 input voltage	880	-	-	mV
V_{IL}	Logic 0 input voltage, not in ULP state	-	-	550	mV
V_{IL_ULPS}	Logic 0 input voltage, ULP state	-	-	300	mV
V_{HYST}	Input hysteresis	25	-	-	mV
e_{SPIKE}	Input pulse rejection	-	-	300	V·ps
T_{MIN-RX}	Minimum pulse width response	20	-	-	



8.3.2 Transmitter Characteristics

High-Speed Transmitter Characteristics

Parameter	Description	Min	Typ.	Max	Unit
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	-	-	360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
t_R and t_F (note1,2)	20%-80%rise time and fall time	-	-	0.3	UI
		-	-	0.35	UI

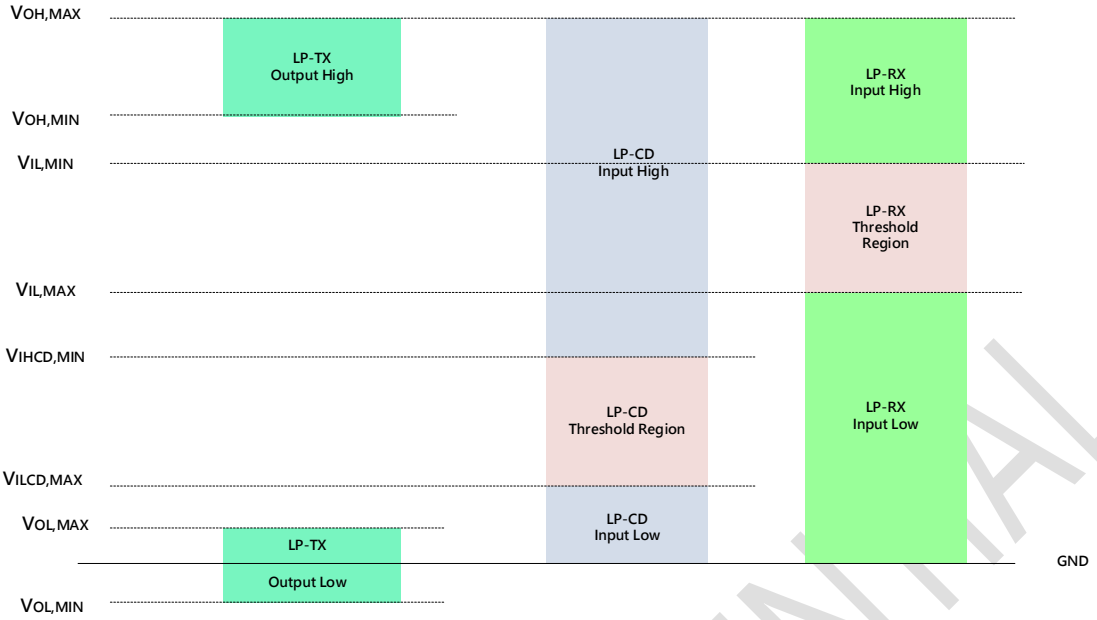
Note:

1. Applicable when supporting maximum HS bitrates ≤ 1Gbps (UI≥1ns)

2. Applicable when supporting maximum HS bitrates > 1Gbps(UI<1ns) but ≤ 1.5Gbps(UI≥0.667ns)

Low-Power Transmitter Characteristics

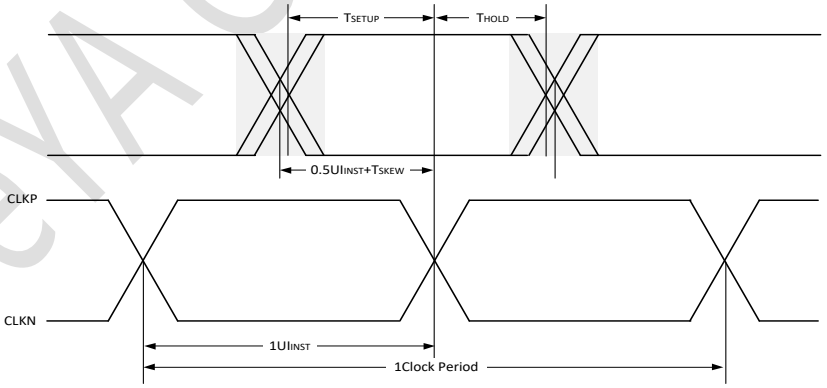
Parameter	Description	Min	Typ.	Max	Unit
V_{OH}	The output high level	1.1	1.2	1.3	V
V_{OL}	The output low level	-50	-	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω
V_{IHCD}	Logic1 contention threshold	450	-	-	mV
V_{ILCD}	Logic0 contention threshold	-	-	200	mV



8.4 Timing Characteristics

8.4.1 High Speed Mode Characteristics

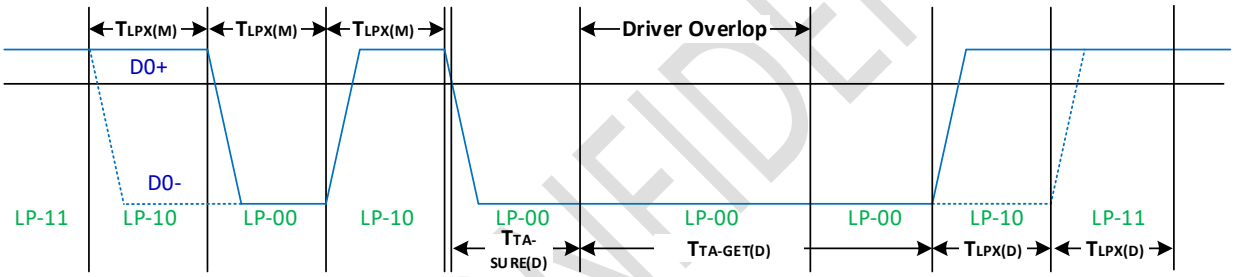
Parameter	Symbol	Min	Typ.	Max	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS



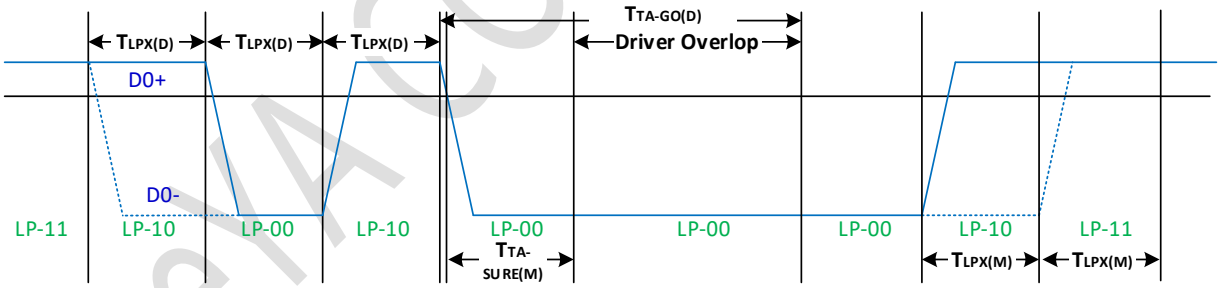
8.4.2 Low Power Mode Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state(LP-00) during a Link Turnaround	T_{LPX}	-	$2*T_{LPX}$	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround	$5* T_{LPX}$			
T_{TA-GO}	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround	$4* T_{LPX}$			

- Bus Turnaround from MPU to display module



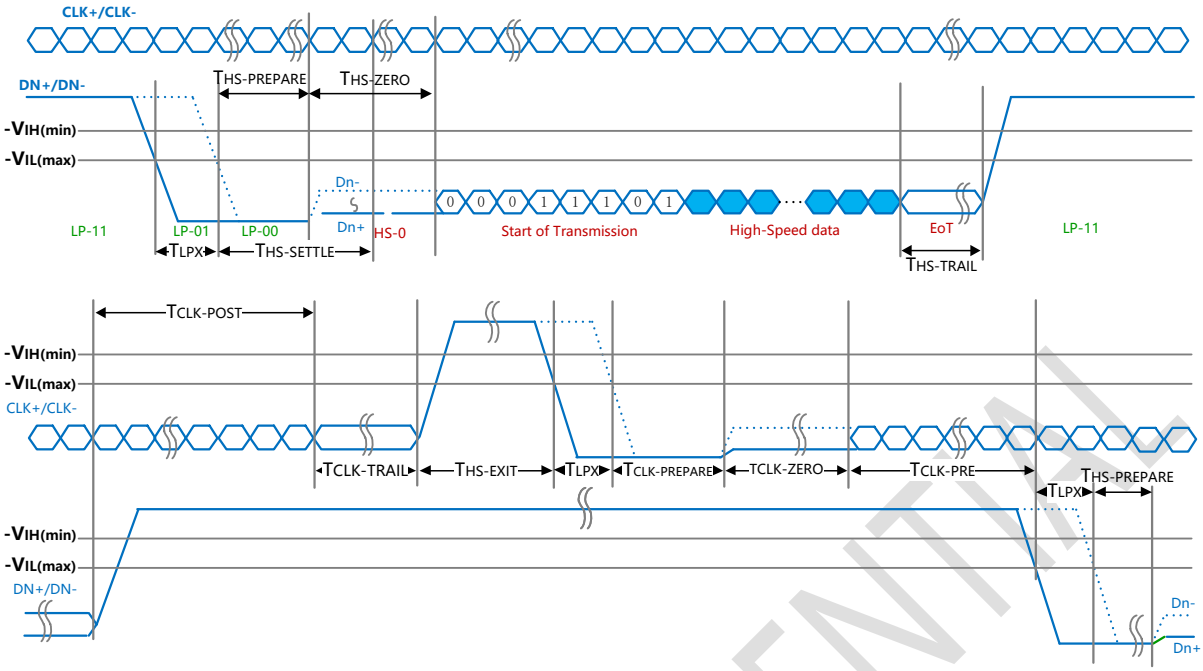
- Bus Turnaround from MPU to display module



8.4.3 High Speed Mode Operation Timing Characteristics

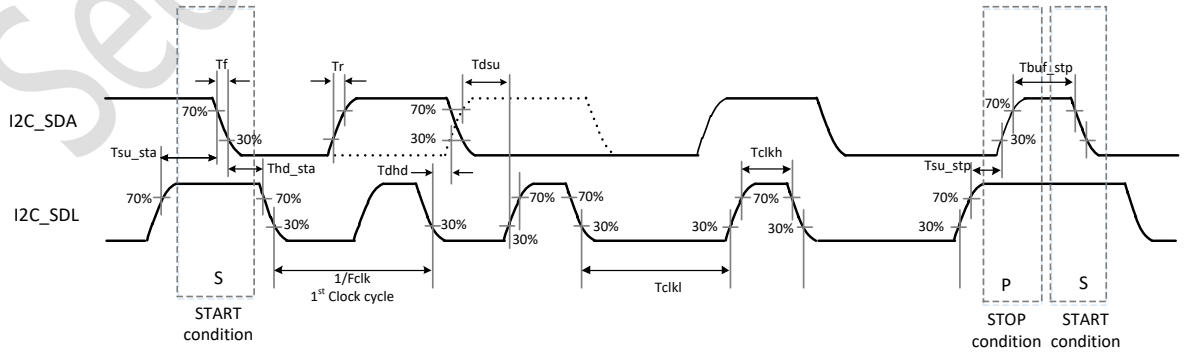
Parameter	Description	Min	Typ.	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning	60ns+52*UI	-	-	ns

	of TCLK-TRAIL				
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE	95	-	300	ns
$T_{CLK-TERM\_EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst t	60	-	-	ns
$T_{CLK-PREPARE}+T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst	100	-	-	ns
T_{D-TERM_EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	35ns+4* UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns+4* UI	-	85ns+6* UI	ns
$T_{HS-PREPARE}+T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	145ns+10*UI	-	-	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value. value.	85ns+6* UI	-	145ns+10*UI	ns



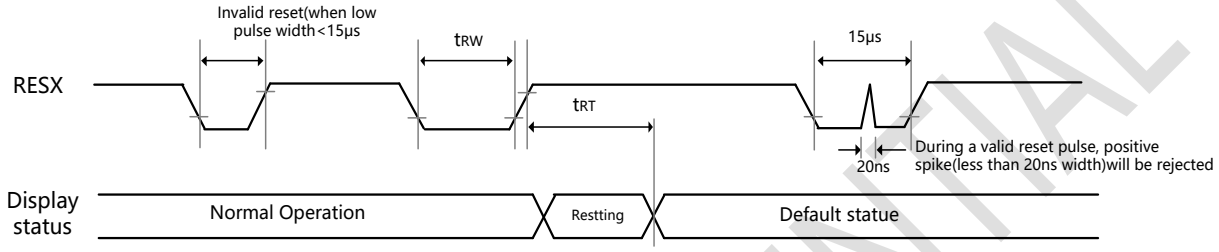
8.4.4 I2C-Bus Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditio
I2C Clock Frequency	Fclk	-	-	400	kH	
I2C Clock Low	Tclkl	130	-	-	ns	
I2C Clock High	Tclkh	600	-	-	ns	
I2C Data Rising Time	Tdr	-	-	300	ns	
I2C Data Falling Time	Tdf	-	-	300	ns	
I2C Data Setup Time	Tdsu	100	-	-	ns	
I2C Data Hold Time	Tdhd	-	-	TBD	ns	
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns	
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns	
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns	
I2C Bus Free Time (Stop Condition)	Tbuf_stp	130	-	-	ns	



8.5 Reset Timing Characteristics

When Reset happens in Sleep-out mode, this Micro-OLED product will enter blanking sequence with the maximum time 120 msec. Then this Micro-OLED product will remain in blanking state and return \ default state. During reset complete time (tRT), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.

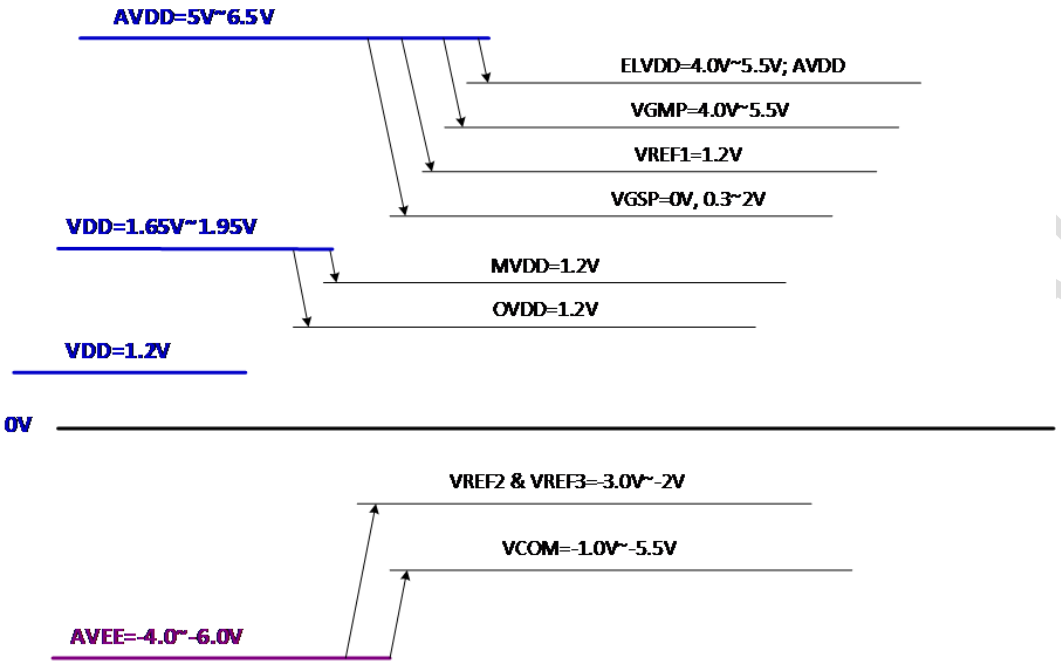


Reset time @VDDI=1.65V to 1.95V, AVSS = VSS = MVSS = 0V, Ta=-40°C to 85°C

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RESX	tRW	Reset low pulse width	15			us	
	tRT	Reset Complete time			20	ms	When reset applied at sleep-in mode
					120	ms	When reset applied at sleep-out mode

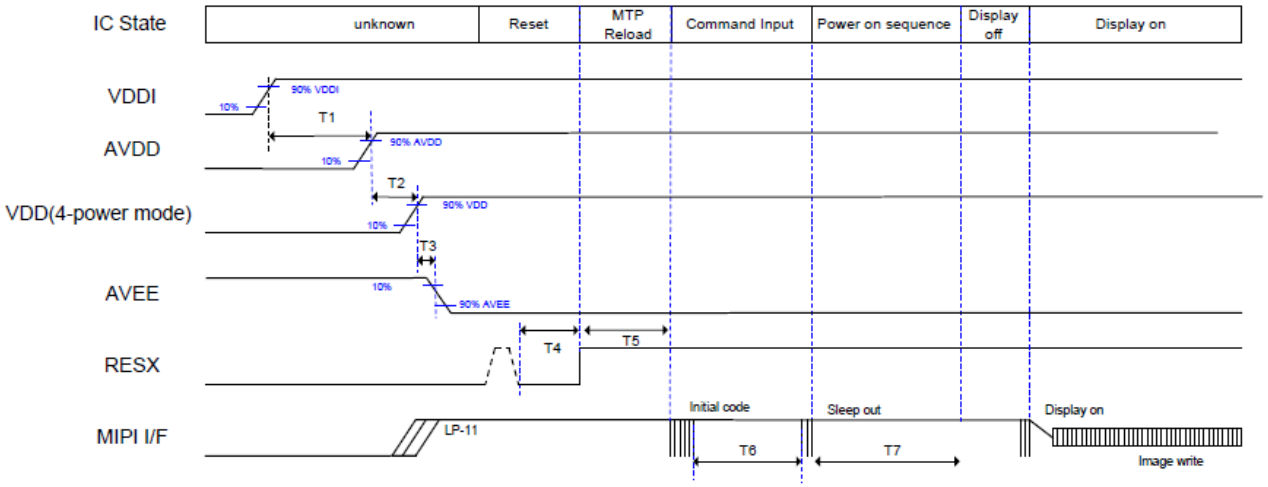
9 Power Generation

9.1 Power Generation Scheme

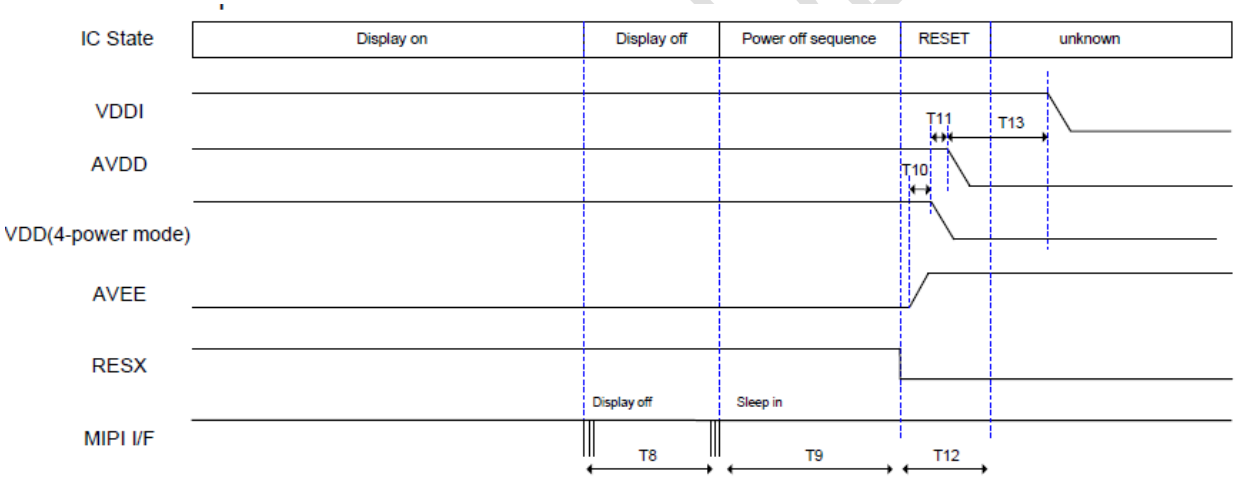


9.2 Power Sequence

Power on sequence



Power off sequence



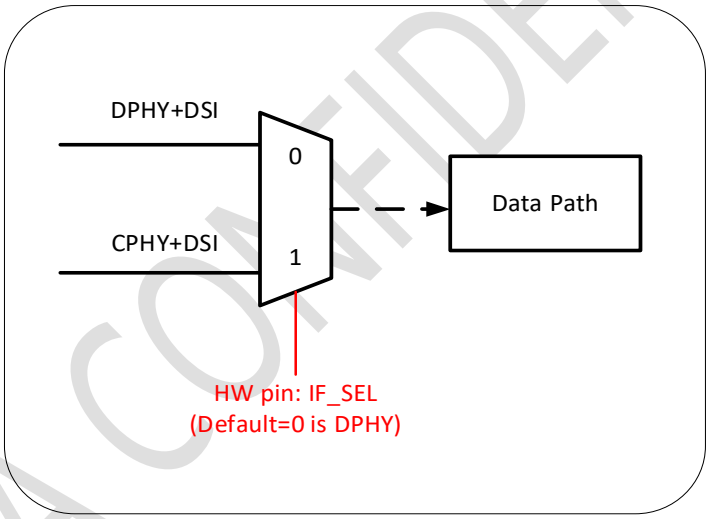
Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between VDDI and AVDD
T2	1	-	-	ms	Power on time between AVDD and VDD
T3	1	-	-	ms	Power on time between VDD and AVEE
T4	1	-	-	ms	Effective hardware reset period
T5	20	-	-	ms	OTP reload time
T6	0	-	-	ms	The time is between initial code finished and sleep-out command
T7	2	-	8	VS	Power on sequence, the period can be modified
T8	1	-	-	VS	Blanking region
T9	-	1	-	VS	Power off sequence, the period can be modified
T10	1	-	-	ms	Power off time between AVEE and VDD
T11	1	-	-	ms	Power off time between VDD and AVDD
T12	1	-	-	ms	Effective hardware reset period
T13	1	-	-	ms	Power off time between AVDD and VDDI

10 Interface

This Micro-OLED product supports MIPI interface and inter-integrated circuit interface (I2C). 1 port MIPI or 2 port MIPI is selected by register, and I2C is selected by IM0, the detail interface selection by IM0 pin and register of PORT1_2_SEL shows in below table.

IM0	PORT1_2_SEL	Command Execute	Image Write
0	0	MIPI	MIPI 1port
0	1	MIPI	MIPI 2 port
1	0	I2C	MIPI 1port
1	1	I2C	MIPI 2 port

This Micro-OLED product supports MIPI interface with D-PHY and C-PHY which is selected by IF_SEL pin.



10.1 I2C Interface

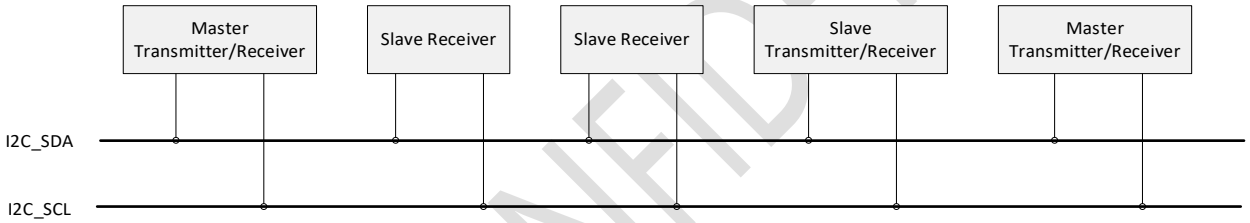
The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte maybe sent. The master generates all clock pulses, including the ninth acknowledge clock pulse.

10.1.1 I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definition

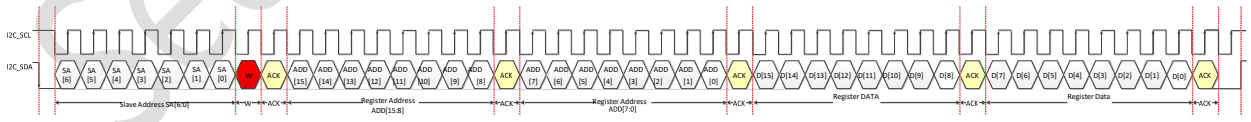
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



10.1.2 Write Sequence

This Micro-OLED product supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

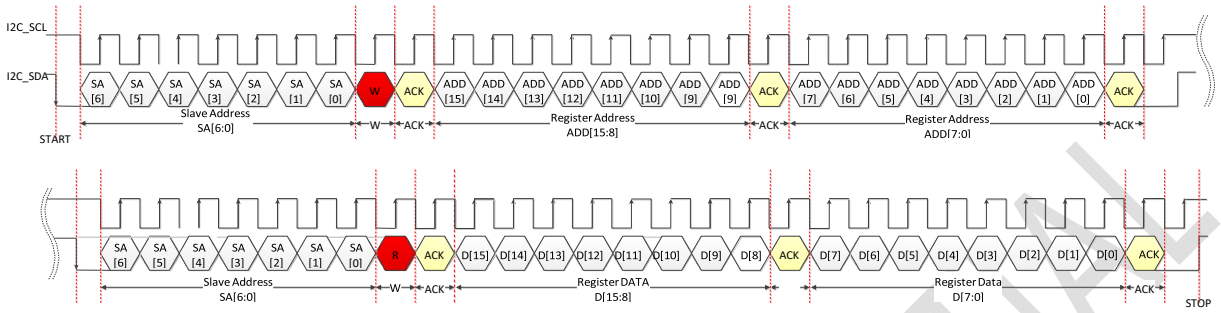
(1) Data transfer for register writing should follow the format shown as below.
(2) After the START condition, a slave address is sent. R/$\overline{W}$ bit is setting to "0" for Write.
(3) The slave issues an ACK to the master.
(4) 8-bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) The chip SA [6:0] =1001100.



W: Write Bit, W= "1" here, R: Read Bit,R= "0" here
ACK: Acknowledge Bit, ACK= "0" here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data

10.1.3 Read Sequence

This Micro-OLED product supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W: Write Bit, W= “0” here, R: Read Bit,R= “1” here
ACK: Acknowledge Bit, ACK= “0” here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data
NACK: Negative Acknowledge Bit, NACK= “1” here

10.2 MIPI Interface

Display serial interface (DSI) specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specification by adoption pixel formats and command set. The detail Lane configuration for DPHY and CPHY are listed below.

[DPHY]

For DPHY, there are one Clock Lane and 1~4 Data Lane. The configuration for DPHY between host and this Micro-OLED product shows as the table below.

Lane Pair	Available Operation Mode	
Clock Lane	Unidirectional Lane	Forward High-Speed Clock Escape Mode (ULPS only)
Data Lane 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 3	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

[DPHY]

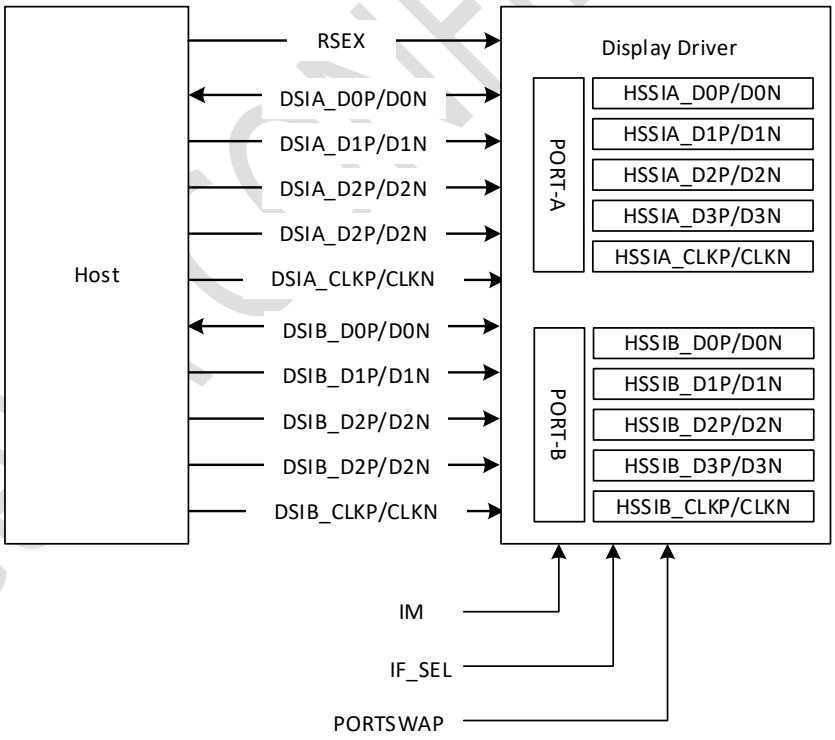
For CPHY, there is no Clock Lane since it’s embedded clock in Data Lane. There are 1~3 Trio (Lane) in CPHY. The configuration for CPHY between host and this Micro-OLED product shows as the table below.

Trio	Available Operation Mode	
Trio 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Trio 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Trio 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

10.2.1 DSI System Configuration

[DPHY]

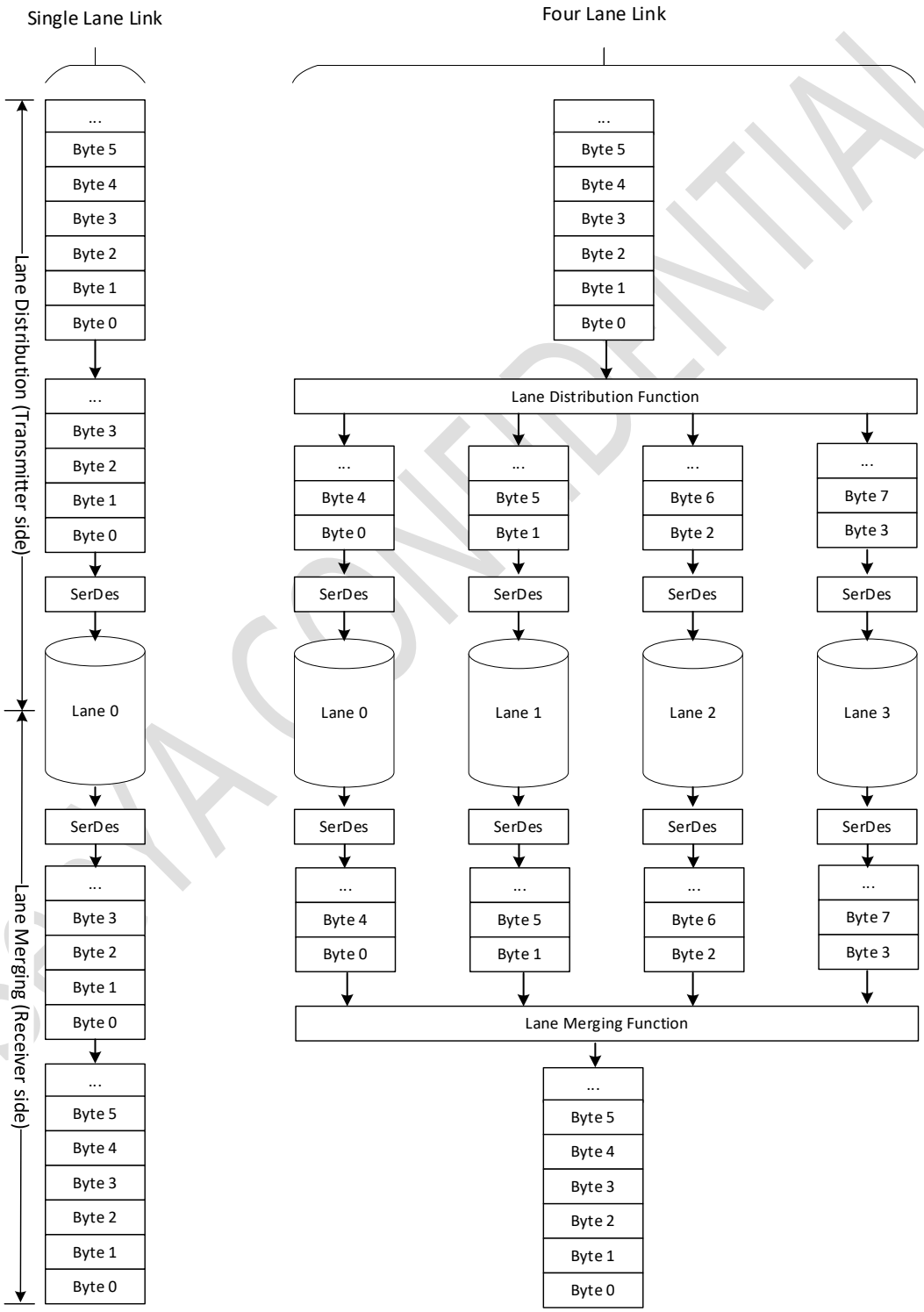
This Micro-OLED product supports MIPI 2 port with 2, 3 or 4 lane configurations for DPHY. The system configuration is shown as the figure below. There are HW pin(IM, IF_SEL, PORTSWAP) and registers (Lane_num_cfg, PSWAP, DSWAP) which can set the interface and lane related configuration.



10.2.2 Multi-Lane Distribution and Merging

[DPHY]

DSI is a lane-scalable interface. Multi-lane implementations shall use a single common clock signal, shared by all data lane. In the transmitter, there will be a layer to distribute a sequence of packet bytes across N Lanes. And in the receiver, there will be a layer to merge this sequence of packet byte back to correct order. The data processing flow is shown as the figure below for DPHY one-lane/four-lane condition.



10.2.3 Interface Level Communication

[DPHY]

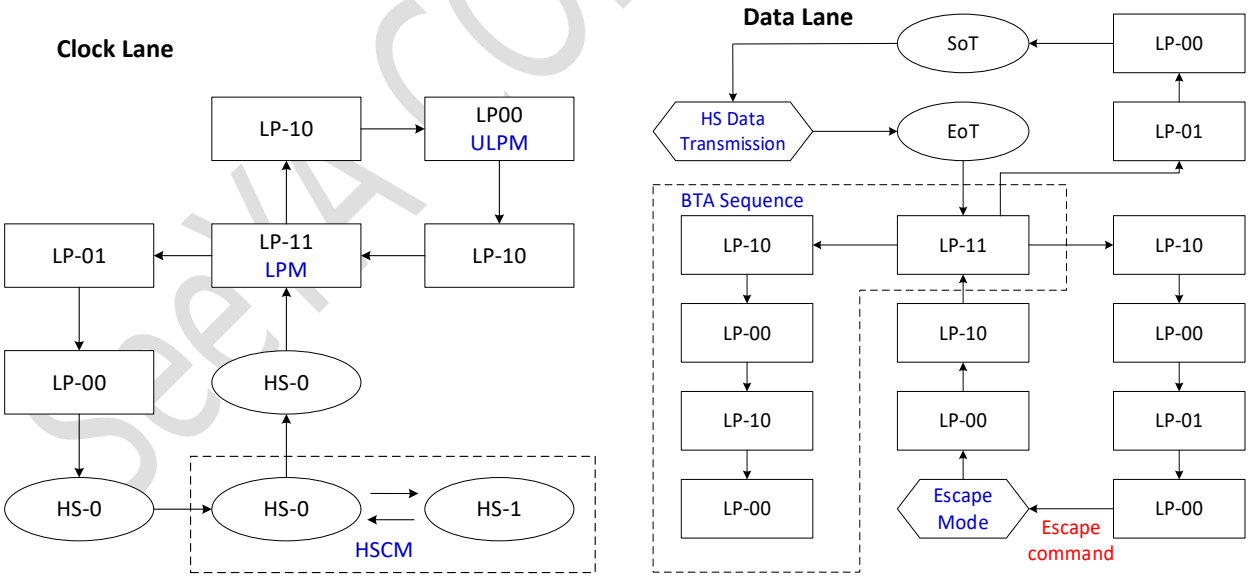
DSI uses data and clock lane for DPHY communication. The Lane state is determined by driving certain Line levels. During normal operation, either a HS-TX or a LP-TX is driving a Lane. The HS-TX always drives the Lane differentially. The LP-TX drives two Lines for a Lane independently and single-ended. These results of High-Speed Lane states and Low-Power Lane states for DPHY are as the table below.

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

10.2.4 Operation Modes

[DPHY]

During normal operation a Lane will be either in Control or High-Speed mode. The clock lane can be driven into three different modes: Low-Power Mode(LPM), Ultra-Low-Power Mode(ULPM) or High-Speed Clock Mode(HSCM). The Data Lane can be driven into following different modes: Escape Mode, HS Data Transmission, Bi-directional Data Lane Turnaround(BTA). The entry and leaving protocol flow chart for DPHY are as below.



10.2.4.1 Escape Modes

[DPHY]

Escape mode is a special mode of operation for Data Lanes using Low-Power stated. With this mode some additional functionality becomes available. A data Lane shall enter Escape mode via Escape mode Entry procedure:

LP-11 →LP-10 →LP-00 →LP-01 →LP-00. An 8-bit entry command shall be sent to indicate the requested action. The available Escape mode commands and actions are as the table below.

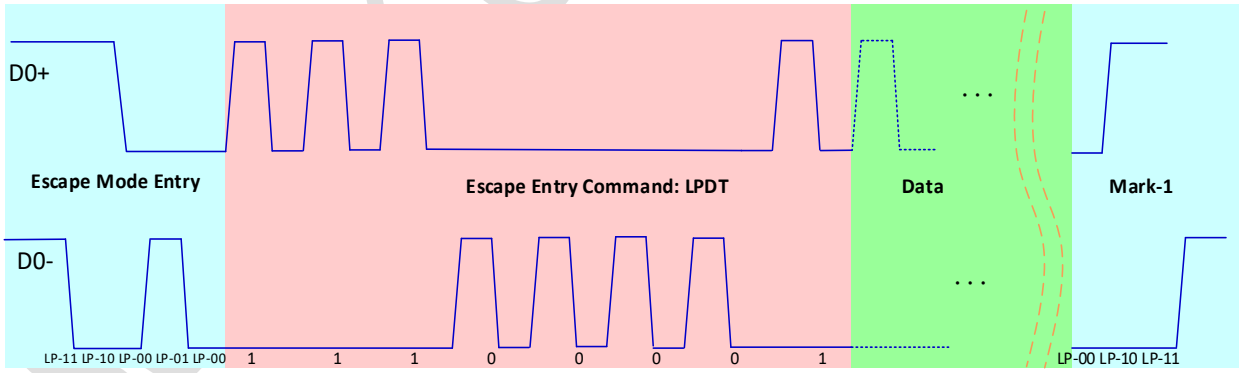
Escape Command	Command Type	Entry Command Pattern (First bit → Last bit)
Low-Power Data Transmission	Mode	1110 0001
Ultra-Low Power State	Mode	0001 1110
Undefined mode	Mode	1001 1111
Undefined mode	Mode	1101 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001
Unknow	Trigger	1010 0000

10.2.4.2 Low Power Data Transmission

[DPHY]

If the Escape mode Entry procedure is followed up by Entry Command for Low Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed. The LPDT waveform is as follows and the figure below.

1. Escape mode Entry Sequence
2. Escape Entry Command(87h) for LPDT
3. LP data for LPDT
4. Mark-1 to leave Escape mode

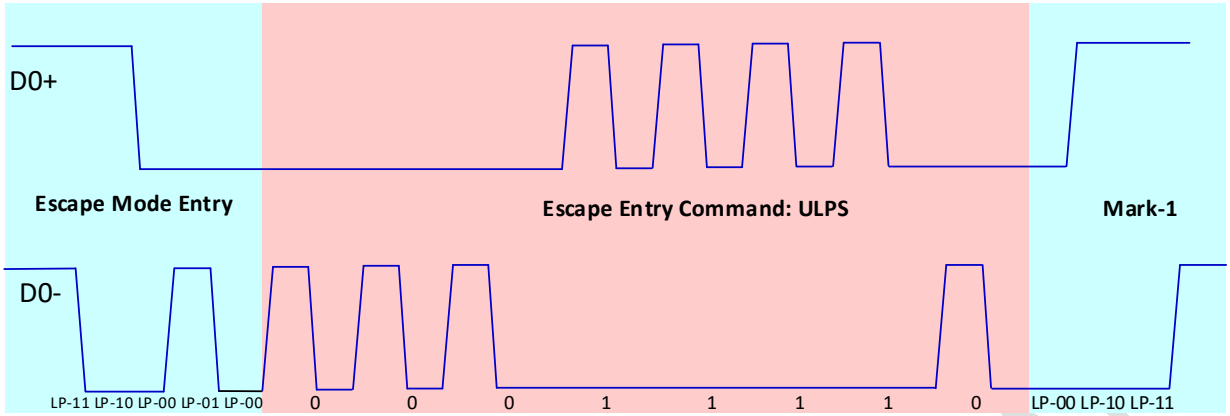


10.2.4.3 Ultra-Low-Power State

[DPHY]

The MCU can force data lane in Ultra-Low-Power State(ULPS) by Escape Mode with ULPS Entry Command. The sequence to force data lane in ULPS is as follows and the figure below.

1. Escape mode Entry Sequence
2. Escape Entry Command(78h) for ULPS
3. Mark-1 to leave Escape mode



10.2.5 High-Speed Data Transmission (HSDT)

[DPHY]

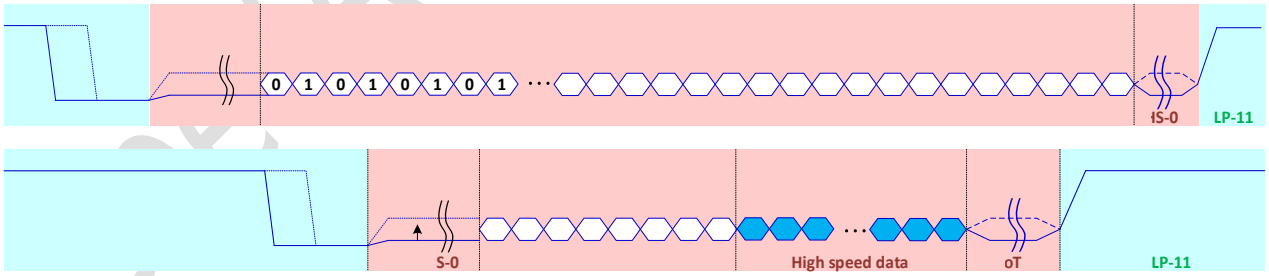
For High-Speed Data Transmission in DPHY, Clock lane has to enter High-Speed Clock Mode (HSCM) before Data lanes enter High-Speed Data Transmission. And the Data lanes have to leave High-Speed Data Transmission after Clock lanes already left HSCM. The High-Speed Data Transmission sequence for DPHY is as the figure below.

- **Data Lane**

1. HS request sequence: LP-11 → LP-01 → LP-00
2. Keep HS-0 for certain time
3. Start of Transmission sequence(B8h)
4. HS data for HSDT
5. End of Transmission sequence (HS-0 if last data bit is HS-1, HS-1 if last data bit is HS-0)
6. Back to LP-11 to leave HSDT

- **Clock Lane**

1. HS request sequence: LP-11 → LP-01 → LP-00
2. Keep HS-0 for certain time
3. High speed clock mode
4. Keep HS-0 for certain time
5. Back to LP-11 to leave HSCM



10.2.6 Burst of High-Speed Data Transmission

[DPHY]

For HSDT, there can be one data packet or multiple packets in one HS burst. These data packets can be long packet (LPa) or Short packet (SPa). HSDT with End of Transmission Packet(EoTP) or without it is selectable.

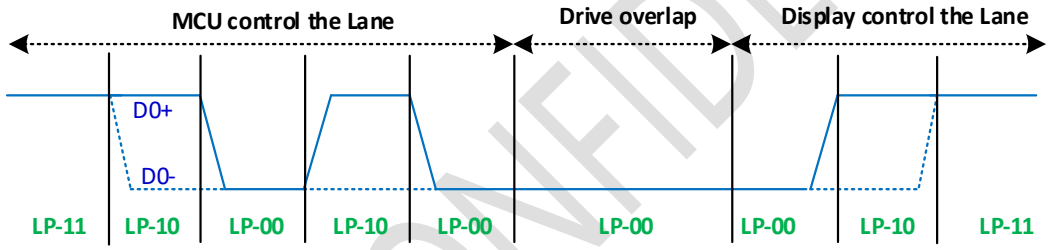
10.2.7 Bi-directional Lane Turnaround(BTA)

[DPHY]

The transmission direction of a bi-directional lane can be swapped by means of a turnaround procedure. The procedure enable information transfer in the opposite direction and this procedure is the same for either a change from forward-to-reverse or reverse-to-forward direction. The BTA procedure is as follows and the figure below.

MCU send Turnaround Request sequence:

1. LP-11 → LP-10 → LP-00 → LP-10 → LP-00
2. MCU change to Hi-Z state and wait for display module start to control the D0 Lane
3. Display module control the Lane and change to stop state:
   LP-00 → LP-10 → LP-11



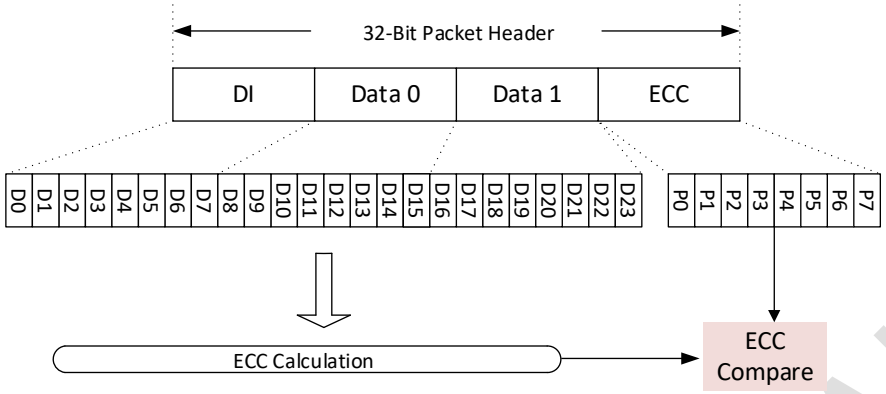
10.2.8 Interface Level Communication

There are two packet structures are defined for communication: Short Packets(SPa) and Long Packets(LPa). For both packet structures, the Data Identifier(DI) is always the first bit of the packet.

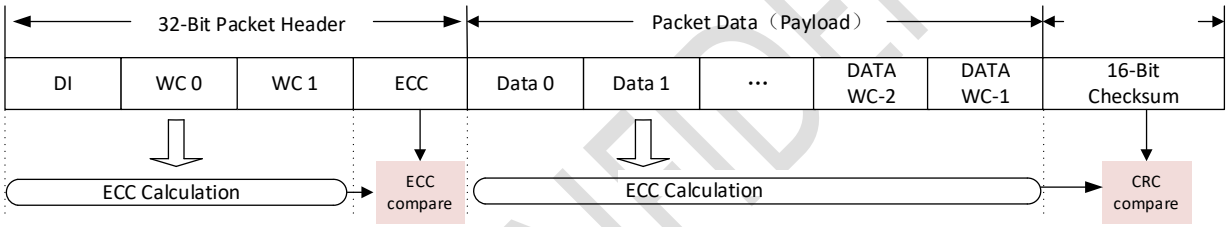
10.2.8.1 General Packet Structure

[DPHY]

For DPHY, Short Packets are four bytes in length including 1 byte DI, 2 bytes data or command and 1 byte Error Correction Code(ECC). The ECC byte is used to check if the first 3 bytes in Packet Header (DI and data) is correct or not. And the ECC byte allows single-bit error to be corrected and 2-bit errors to be detected. The packet format for Short Packets are illustrated as the following.



As to Long Packets, they shall consist of three elements: 4 bytes Packet Header, Data Payload with a variable number of bytes and 2 bytes Packet Footer. The Packet Header includes 1 byte DI, 2 bytes Word Count(WC) and 1 byte ECC. The Word Count in Packet Header will decide the number of total bytes of the Data Payload. The Packet Footer has 2 bytes Checksum used to check if the Payload Data is correct or not. The packet format for Long Packets are illustrated as the following.



10.2.8.2 Bit Order and Byte Order for Packets

[DPHY]

The bit order for packets is the Least Signification Bit sent first and the Most Significant Bit sent last. And for the byte order for packets is the Least Signification Byte sent first and the Most Significant Byte sent last.

10.2.8.3 Common Packet Elements

[DPHY]

There are several common elements for Long and Short Packets such as DI byte and ECC byte. The DI byte consists of 2-bit Virtual Channel identifier (VC = DI[7:6]) and 6-bit Data Type field (DT = DI[5:0]). The DI structure is as the following.

Data Indentifier(DI)							
Virtual Channel(VC)		Data Type(DT)					
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

Virtual Channel is used to assign which peripherals for packets transmission. Data Type specifies if the packet is a Long or Short Packet and the packet format. The Data Type are defined as the table below.

Data Types for Peripheral-Sourced Packets

Data Type(hex)	Data Type(binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short

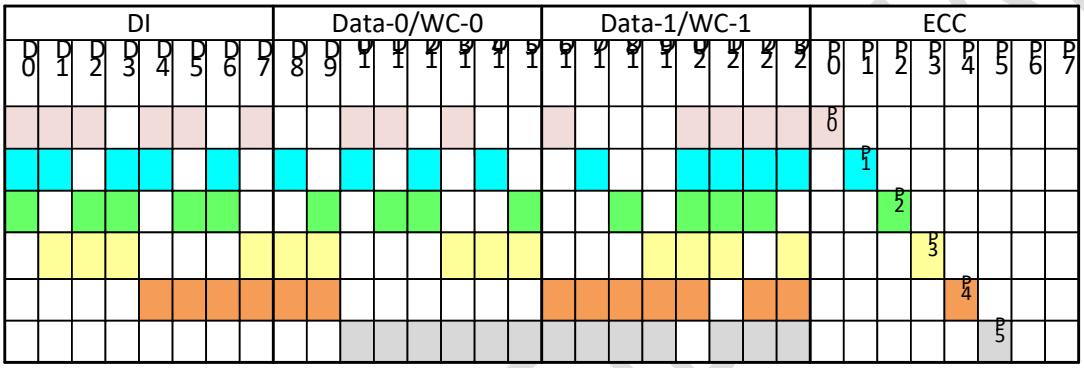
0x11	01 0001	Generic Short READ Response, 1 byte returned	Short
0x12	01 0010	Generic Short READ Response, 2 bytes returned	Short
0x1A	01 1010	Generic Long READ Response	Long
0x1C	01 1100	DCS Long READ Response	Long
0x21	10 0001	DCS Short READ Response, 1 byte returned	Short
0x22	10 0010	DCS Short READ Response, 2 bytes returned	Short

Data Types for Processor-Sourced Packets

Data Type(hex)	Data Type(binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x07	00 0111	Compression Mode Command	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write	Long
0x0A	00 1010	Picture Parameter Set	Long
0x0B	00 1011	Compressed Pixel Stream	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

As to ECC, the host processor shall always calculate and transmit an ECC byte to identify the error for the Packet Header. The bits of ECC are defined as the rule below. The symbol '^' means XOR function. P7 and P6 are set to 0 because Error Correction Code is based on 64-bit value but this ECC implementation is only used for 24-bit value.

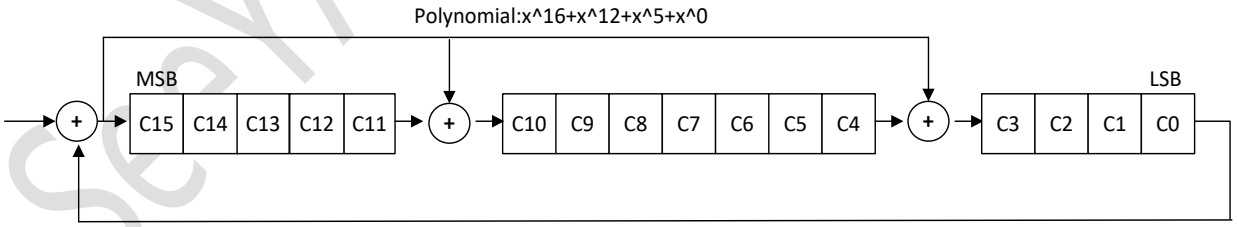
P7 = 0
P6 = 0
P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23



10.2.8.4 Packet Footer for Long Packets

[DPHY]

The Packet Footer for Long Packets is a checksum value which is calculated from the Data Payload in the Long Packet. The checksum is using a 16-bit Cyclic Redundancy Check(CRC) with a generator polynomial of x^16 + x^12 + x^5 + x^0. The Receiver will calculate checksum value from received Data Payload and compare this CRC value with the Packet Footer sent by transmitter. If calculated CRC values equal to Packet Footer, the received Data Payload are correct. The CRC implementation is presented as the following.



10.2.8.5 Packet Pixel Stream Format

[DPHY]

There are 4 packet pixel stream format: 16-bit RGB 5-6-5, 18-bit RGB 6-6-6, loosely packed 18-bit RGB 6-6-6 and 24-bit RGB 8-8-8. The Data Type for these pixel stream format are shown as the table below.

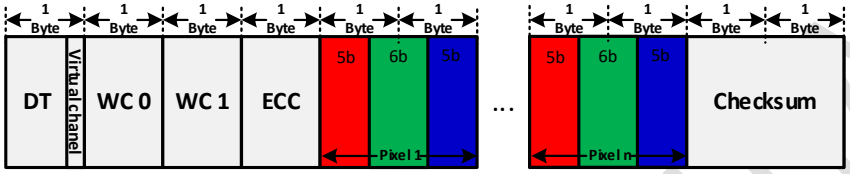
Data Type(hex)	Data Type(binary)	Description	Packet Size
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long

0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

Note: This Micro-OLED product only support 24-bit RGB pixel stream format

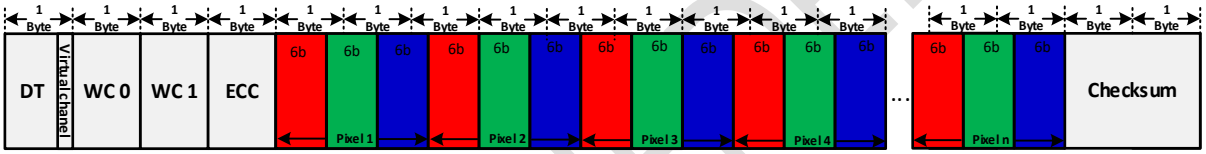
10.2.8.6 16- bit RGB Format, Data Type = 0x0E

The data of 16-bit RGB pixel format comprise of five bits red, six bits green and five bits blue. Note that the "Green" component is split across two bytes. The pixel stream format is shown as the figure below.



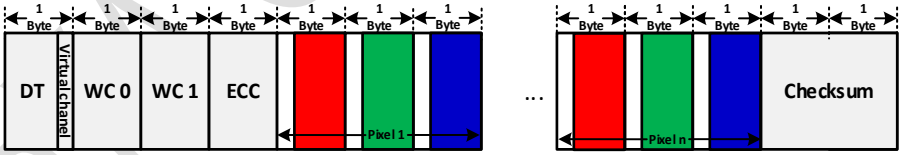
10.2.8.7 18- bit RGB Format, Data Type = 0x1E

The data of 18-bit RGB pixel format comprise of six bits red, six bits green and six bits blue. The pixel stream format is shown as the figure below.



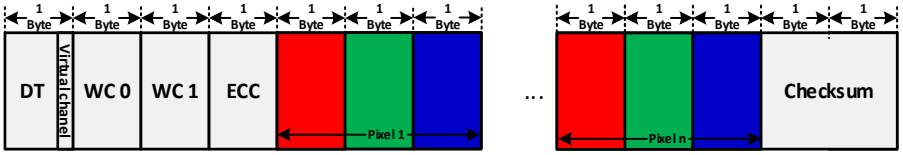
10.2.8.8 18-bit Loosely RGB Format, Data Type = 0x2E

The data of 18-bit loosely RGB pixel format comprise of six bits red, six bits green and six bits blue. But the six bits of each color is shifted to the upper bits of the byte and the bit[1:0] of each payload byte are ignored. This requires more bandwidth than the "packed" format but requires less shifting and multiplexing logic in the packing and unpacking function. The pixel stream format is shown as the figure below.



10.2.8.9 24-bit RGB Format, Data Type = 0x3E

The data of 24-bit RGB pixel format comprise of eight bits red, eight bits green and eight bits blue. The pixel stream format is shown as the figure below.



10.2.9 Peripheral-to-Processor LP Transmissions

[DPHY]

All systems require bi-directional capability for returning READ data, acknowledge or error information to the Host

Processor. It shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use Low Power mode of Transmission.

Packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction. There are four basic types for peripheral-to-processor transactions: Acknowledge, Acknowledge and Error Report, Response to Read Request, Tearing Effect(TE)

Acknowledge and Error Report is a Short Packet sent if any errors were detected in preceding transmissions from the Host Processor. Once the Errors are reported, the accumulated errors in the error register are cleared.

An error report is a short packet comprised of two bytes following the DI byte and with an ECC byte following the Error Report bytes. Detection and reporting of each error types is signified by setting the corresponding bit to “1”. The bit assignment for all error reporting is shown as the table below.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, single-bit(detected and corrected)
9	ECC Error, multi-bit(detected, not corrected)
10	Payload Checksum Error
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

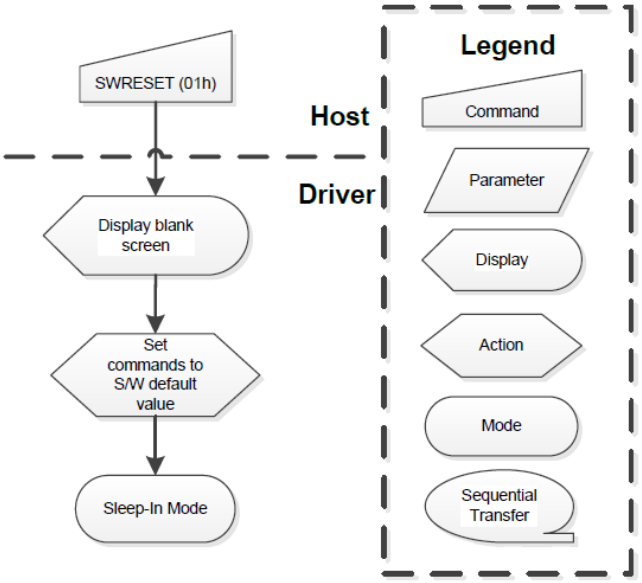
11 User Command

Command list

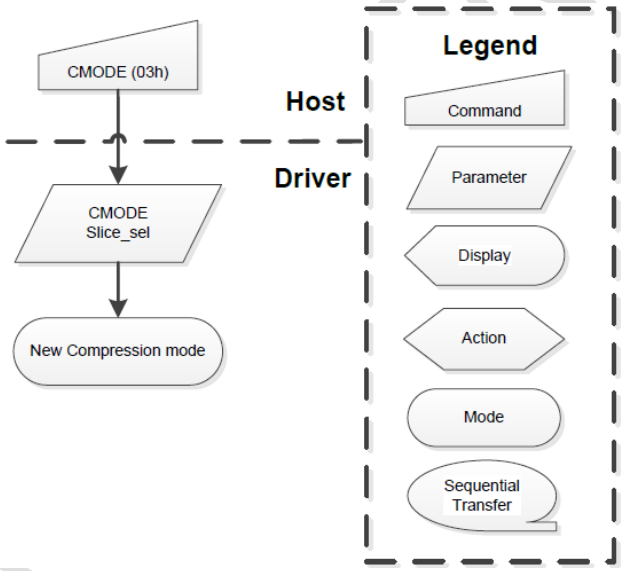
Instruction	R/W	Address		D7	D6	D5	D4	D3	D2	D1	D0	Default
		MIPI	Non-MIPI									
SWRESET	W	01h	0100h	No Parameter								N/A
CMODE	R/W	03h	0300h	slice2_sel	-	-	-	-	-	-	CMODE	80h
SLPIN	W	10h	1000h	No Parameter								N/A
SLPOUT	W	11h	1100h	No Parameter								N/A
ALLPOFF	W	22h	2200h	No Parameter								N/A
ALLPON	W	23h	2300h	No Parameter								N/A
TCON	R/W	25h	2500h	-	-	-	-	-	-	-	TC_ENABLE	00h
GAMSET	R/W	26H	2600h	GC[7:0]								01h
			2601h	TC1_TS_Man	DD_TS	-	TC1_TS_SEL[4:0]					40h
DSPOFF	W	28h	2800h	No Parameter								N/A
DSPON	W	29h	2900h	No Parameter								N/A
CASET	R/W	2Ah	2A00h	XS[15:8]								00h
	R/W		2A01h	XS[7:0]								00h
RASET	R/W	2Bh	2B00h	YS[15:8]								00h
	R/W		2B01h	YS[7:0]								00h
TEON	R/W	35h	3500h	-	-	-	-	-	-	-	M	00h
MADCTL	R/W	36h	3600h	-	-	-	-	RGB	-	RSMX	RSMY	00h
IDMOFF	R/W	38h	3800h	No Parameter								N/A
IDMON	R/W	39h	3900h	No Parameter								N/A
COLMOD	R/W	3Ah	3A00h	VIPF[3:0]				-	-	-	-	70h
WRDISBV	W	51h	5100h	DBV[7:0]								00h
	W		5101h	-	-	-	-	-	-	-	DBV[8]	00h
WRCTRLD	W	53h	5300h	-	-	BCTRL	-	DD	DD_TC	-	HBHC_ SEL	00h
SCACTRL	W	69h	6900h							SC_MOD_SEL[1:0]		00h
IFCONFG	R/W	6Bh	6B00h	-	-	-	PORT1_2_SEL_ CMD1	-	-	-	-	10h
RESCTRL1	R/W	80h	8000h	-	-	-	-	-	-	-	OSC_FREQ_SEL	01h
			8001h	NC[7:0]								40h
			8002h	NL[7:0]								40h
			8003h	-	-	-	NC[8]	-	-	-	NL[8]	11h
RESCTRL2	R/W	81h	8100h	-	-	-	-	-	-	T1A[9:8]		01h
	R/W		8101h	T1A[7:0]								54h
	R/W		8102h	-	-	-	-	-	-	VBPDA[9:8]		00h
	R/W		8103h	VBPDA[7:0]								08h
	R/W		8104h	-	-	-	-	-	-	VFPDA[9:8]		00h
	R/W		8105h	VFPDA[7:0]								10h
	R/W		8106h	-	-	-	-	-	PSELA[2:0]			00h
RESCTRL3	R/W	82h	8200h	-	-	-	-	-	-	T1B[9:8]		01h
	R/W		8201h	T1B[7:0]								54h
	R/W		8202h	-	-	-	-	-	-	VBPDB[9:8]		00h

	R/W		8203h	VBPDB[7:0]								08h
	R/W		8204h	-	-	-	-	-	-	VFPDB[9:8]		00h
	R/W		8205h	VFPDB[7:0]								10h
	R/W		8206h	-	-	-	-	-	PSELB[2:0]			01h
PORCH_EXT	R/W	83h	8300h	VBP_EXT[9:8]		VFP_EXT[9:8]		-	-	-	EN_VBP_VFP_EXT	00h
	R/W		8301h	VBP_EXT[7:0]								20h
	R/W		8302h	VFP_EXT[7:0]								20h

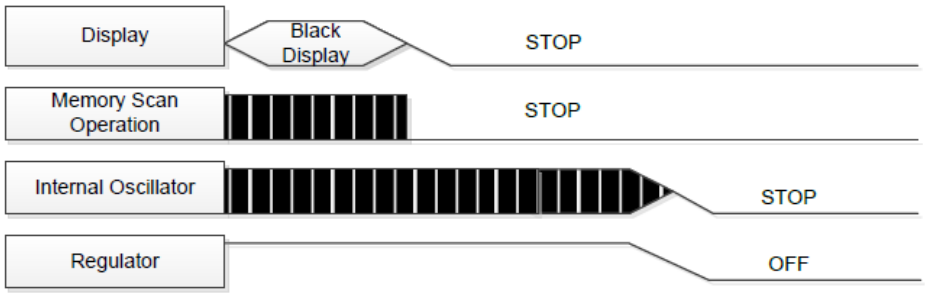
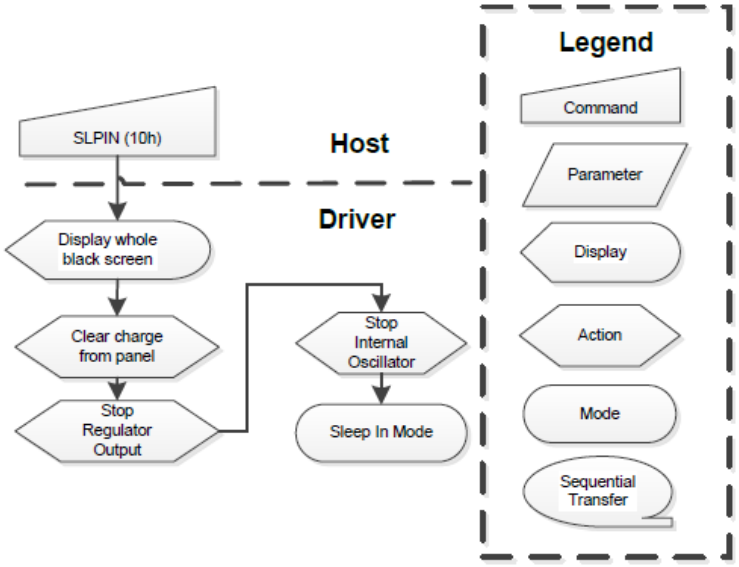
SWRESET(0100h): Software Reset

<table>
<tr><td>0100H</td><td colspan="12">SWRESET</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>SWRESET</td><td>W</td><td>01h</td><td>0100h</td><td>-</td><td colspan="8">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">When the Software Reset command is executed, all related register and parameters are reset to their S/W Reset default values.</td></tr>
<tr><td>Restriction</td><td colspan="12">It is necessary to wait 10m sec to send any command following the S/W Reset.
If S/W Reset is executed in Sleep-out mode, it is necessary to wait 120m sec to send Sleep-Out command. The Software Reset command cannot be sent during Sleep-Out sequence. Any new command cannot be sent within 8-frame until device enters Sleep-In mode.</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td>Power On Sequence</td><td>0100h</td><td>N/A</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

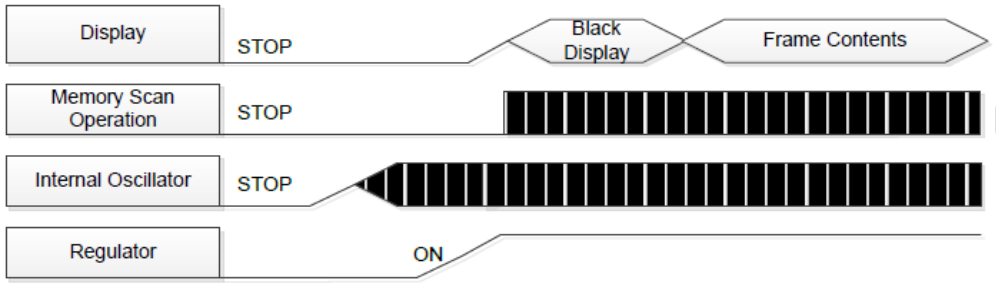
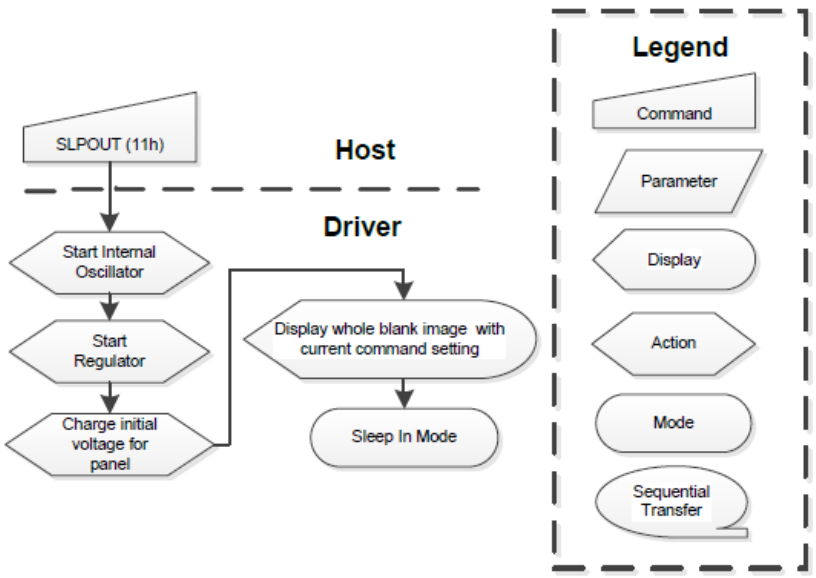
CMODE(0300h): Compression Mode

<table>
<tr><td>0400H</td><td colspan="12">RDID123</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>CMODE</td><td>R/W</td><td>03h</td><td>0300h</td><td>-</td><td>D7</td><td></td><td></td><td></td><td></td><td></td><td></td><td>D0</td></tr>
<tr><td>Description</td><td colspan="12">These commands are used for compression mode
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>slice_sel</td><td>Compression slice selection</td><td>0=1 slice
1=2 slice</td></tr>
<tr><td>D0</td><td>CMODE</td><td>Enable/Disable compression mode</td><td>0=Disable
1=Enable</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0300h</td><td>80h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

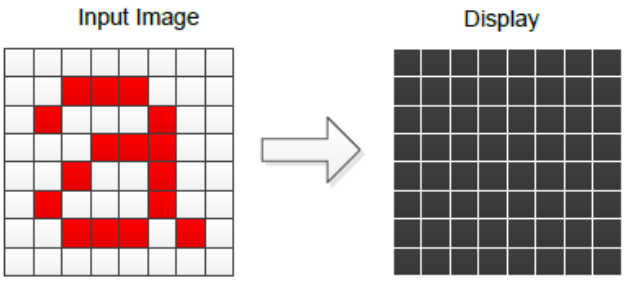
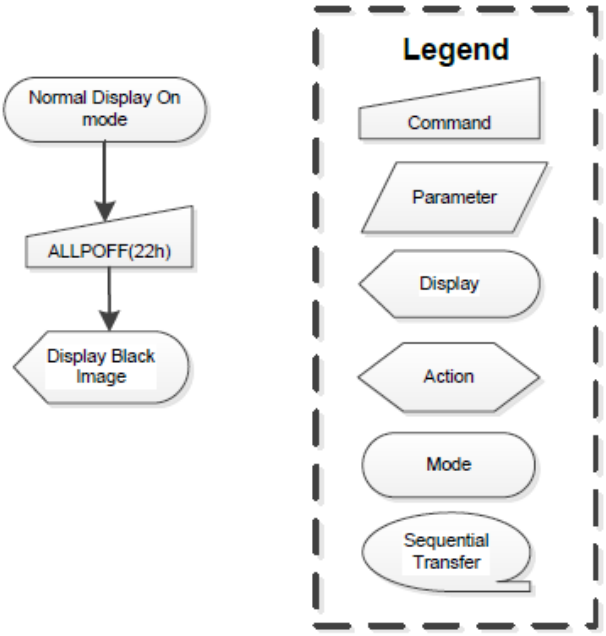
SLPIN (1000h): Sleep In

<table>
<tr><td>1000H</td><td colspan="12">SLPIN</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>SLPIN</td><td>W</td><td>10h</td><td>1000h</td><td>-</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command force display module to enter Sleep-In mode. Under Sleep-In mode, internal display oscillator, and panel scanning are all stopped. The interface and related registers are still working and keeps its values.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>1000h</td><td>Sleep In Mode</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

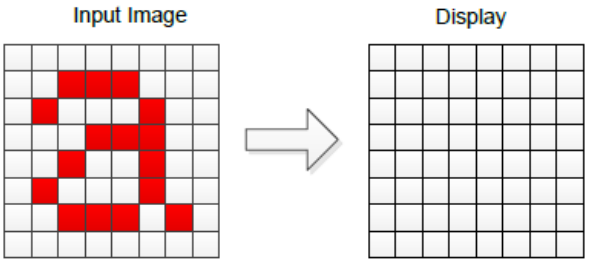
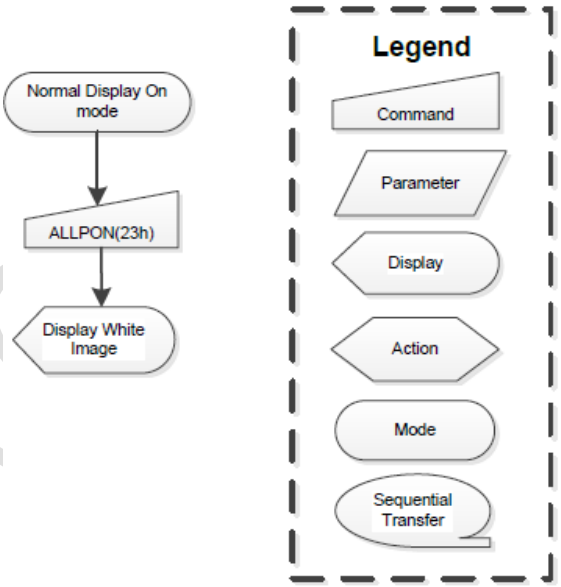
SLPOUT (1100h): Sleep Out

1100H	SLPOUT											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	W	11h	1100h	-	No Parameter							
Description	This command force display module to exit *Sleep-In* mode. Under *Sleep-out* mode regulator, internal display oscillator, and panel scanning are allenable. 											
Restriction	-											
Default	Status	Default Value										
	Power On Sequence	1100h	Sleep In Mode									
	SW Reset	The same as above										
	HW Reset	The same as above										
Flow chart												

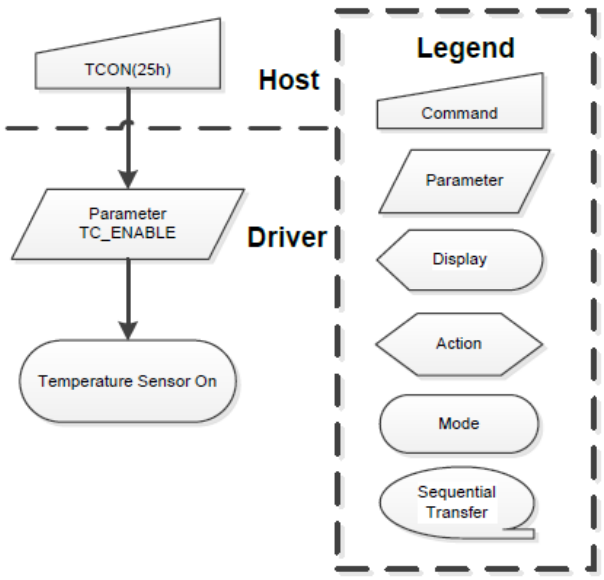
ALLPOFF (2200h): All Pixels OFF

<table>
<tr><td>2200H</td><td colspan="12">ALLPOFF</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>ALLPOFF</td><td>W</td><td>22h</td><td>2200h</td><td>-</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command forces the display module to display black image in Display-On Mode.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td>Power On Sequence</td><td>2200h</td><td>All Pixel Off</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

ALLPON (2300h): All Pixel ON

<table>
<tr><td>2300H</td><td colspan="12">ALLPON</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>ALLPON</td><td>W</td><td>23h</td><td>2300h</td><td>-</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command forces the display module to display white image in Display-OnMode.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>2300h</td><td>All Pixel Off</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

TCON (2500h): Temperature Sensor Enable

<table>
<tr><td>2300H</td><td colspan="12">ALLPON</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>ALLPON</td><td>R/W</td><td>25h</td><td>2500h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>D0</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to turn on temperature sensor.
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D0</td><td>TC_ENABLE</td><td>Temperature sensor enable</td><td>0=Temperature sensor off
1=Temperature sensor on</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>2500h</td><td>00h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

GAMSET (2600h): Gamma Set

2600H	GAMSET											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
GAMSET	R/W	26h	2600h	-	GC[7:0]							
			2601h	-	D7	D6	-	D[4:0]				

Description

This command sets used gamma code and white balance of displaymodule.

Bit	Symbol	Description	Comment
D[7:0]	GC[7:0]	Gamma code selection	GC [0]=1: Normal mode Others= Reserved
D7	TC1_TS_Man	TC1 Manual mode	0: Disable TC manual mode 1: Enable TC manual mode
D6	DD_TS	Temperature dimming	0: Disable TS dimming 1: Enable TS dimming
D[4:0]	TC1_TS_SEL[4:0]	Temperature Index for manual mode	See Table as below

Temperature index table

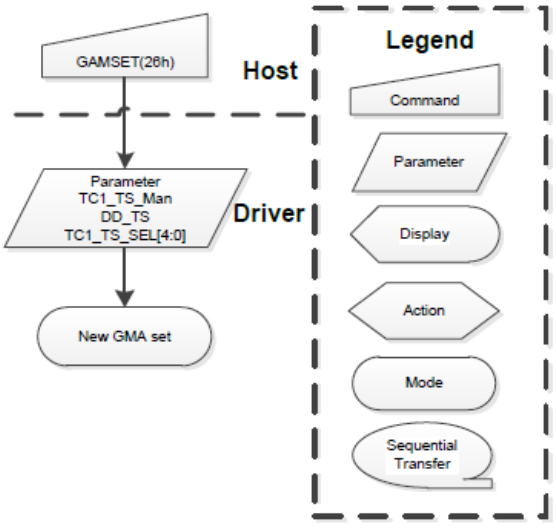
TC1_TS_SEL[4:0]	Temperature (degree)	TC1_TS_SEL[4:0]	Temperature (degree)
00h	0	07h	35
01h	5	08h	40
02h	10	09h	45
03h	15	0Ah	50
04h	20	0Bh	55
05h	25	0Ch	60
06h	30	Others	Reserved

Restriction: -

Default

Status	Default Value	
Power On Sequence	2600h	01h
	2601h	40h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart

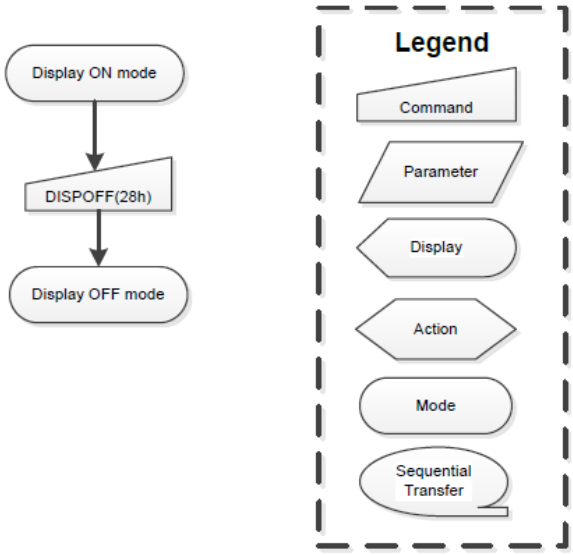


DISPOFF (2800h): Display OFF

2800H	DISPOFF											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	W	28h	2800h	-	No Parameter							
Description	This command forces the display module to stop displaying image data.											
Restriction	This command has no effect when display driver is already in *DISPLAY-OFF* mode											

Default	Status	Default Value	
	Power On Sequence	2800h	Display Off
	SW Reset	The same as above	
	HW Reset	The same as above	

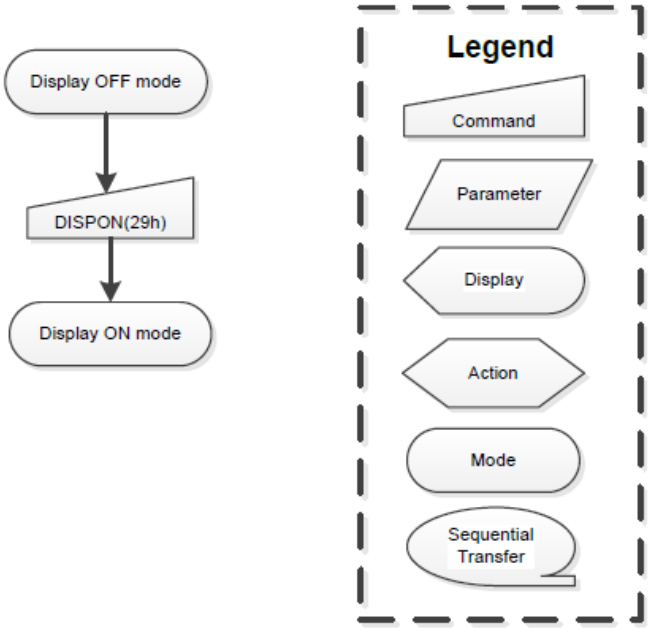
Flow Chart



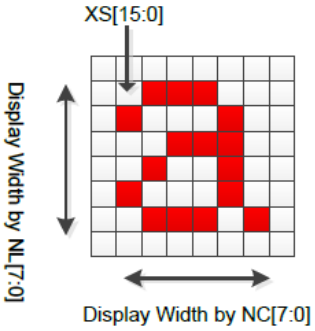
DISPON (2900h): Display ON

2900H	DISPON											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	W	29h	2900h	-	No Parameter							
Description	This command forces the display module to start displaying image data.											
Restriction	This command has no effect when display driver is already in *DISPLAY-ON* mode.											

Default	Status	Default Value	
	Power On Sequence	2900h	Display Off
	SW Reset	The same as above	
	HW Reset	The same as above	



CASET (2A00h): Column Address Set

2A00H	CASET										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
CASET	R/W	2Ah	2A00h	-	XS[15:8]							
			2A01h	-	XS[7:0]							
Description	This command indicates display start position of display module in columns. XS[15:0]: Display line start position.  										
Restriction	1. XS= 0 + 2N, N=integer 2. Display content can be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can't exceed display area. XS should follow the rule as below: PIXEL_SHIFT_X_DIR=0(Left) Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 - PIXEL_SHIFT_X_COUNT*2 ≤ 2568 (A08h) PIXEL_SHIFT_X_DIR=1(Right) Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 + PIXEL_SHIFT_X_COUNT*2 ≤ 2568 (A08h)										

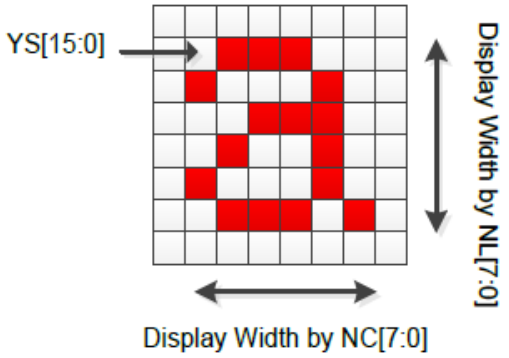
Default	Status	Default Value	
	Power On Sequence	2A00h	00h
		2A01h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

RASET (2B00h): Row Address Set

2A00H	CASET										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RASET	R/W	2Bh	2B00h	-	YS[15:8]							
			2B01h	-	YS[7:0]							

Description

This command indicates display start position of display module in rows.
XS[15:0]: Display line start position.

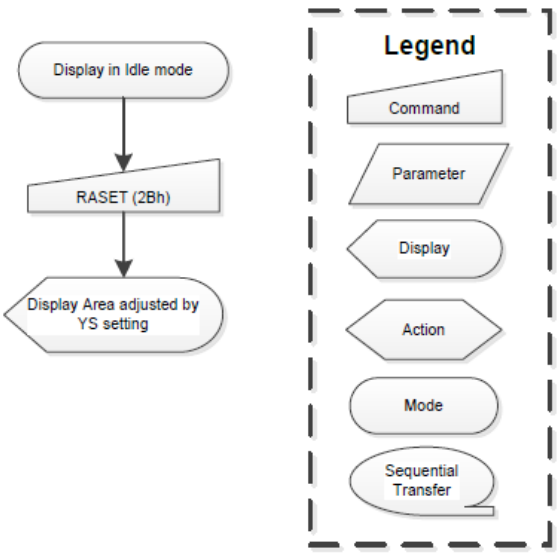


Restriction

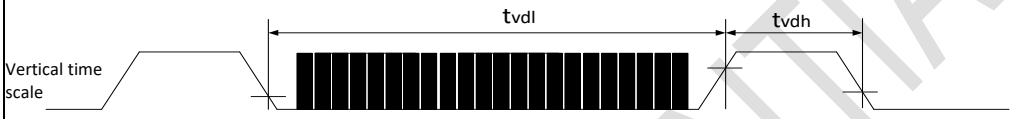
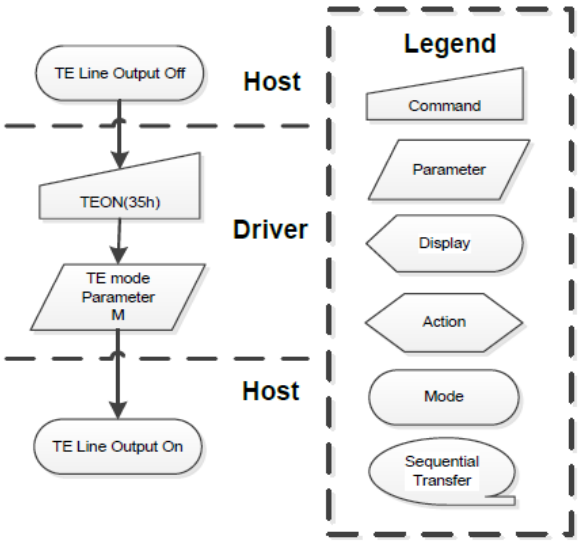
1. YS= 0 + 2N, N=integer
2. Display content cane be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can't exceed display area. YS should follow the rule as below: PIXEL_SHIFT_Y_DIR=0(Up)
   Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 - PIXEL_SHIFT_Y_COUNT*2 ≤ 2568 (A08h)
   PIXEL_SHIFT_Y_DIR=1(Down)
   Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 + PIXEL_SHIFT_Y_COUNT*2 ≤ 2568 (A08h)

Default

Status	Default Value	
Power On Sequence	2B00h	00h
	2B01h	00h
SW Reset	The same as above	
HW Reset	The same as above	



TEON (3500h): Tearing Effect Line ON

3500H	TEON										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
TEON	W	35h	3500h	-	-	-	-	-	-	-	-	M
Description	This command is used to turn on Tearing Effect Output signal outputting to pad. The Tearing Effect Line On has one parameter which describes the mode of Tearing Effect Output signal. When M="0": The Tearing Effect Output line consists of V-Blanking information only  When M="1": The Tearing Effect Output line consists of V-Blanking and H-Blanking information only 										
Restriction	Tearing Effect output will be low if the display module is in *Sleep-In* mode.										
Default	Status	Default Value									
	Power On Sequence	3500h	Tearing Effect Off								
	SW Reset	The same as above									
	HW Reset	The same as above									
Flow Chart											

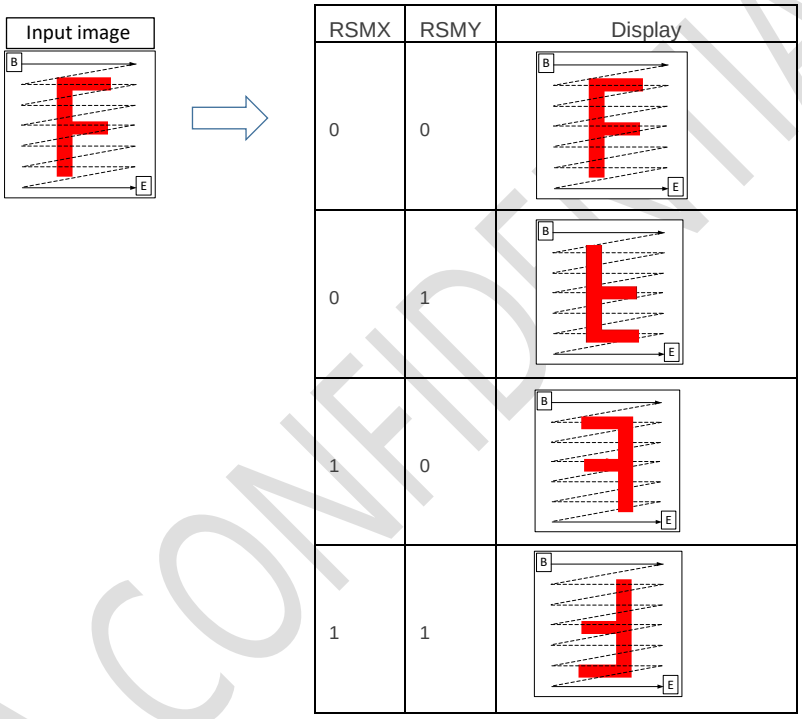
MADCTL (3600h): Set Address Mode

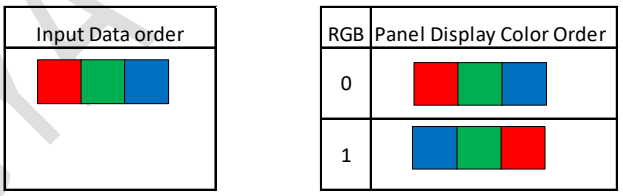
3600H	MADCTL										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	R/W	36h	3600h	-	-	-	-	-	D3	-	D1	D0

Description

This command set scan direction of source and gate and data order.

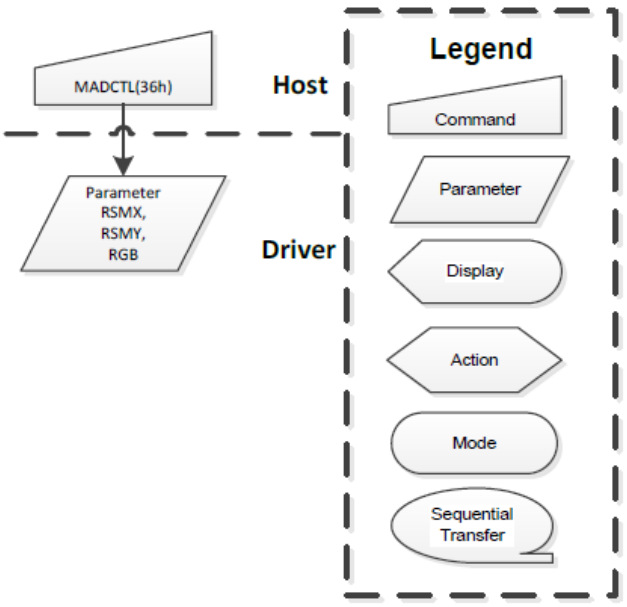
Bit	Symbol	Description	Comment
D3]	RGB	Color Order of sub-pixel of true RGB type	1=BGR 0=RGB
D1	RSMX	Horizontal Flip	1=Normal Display 0= Horizontal Flip
D0	RSMY	Vertical Flip	1= Normal Display 0= Vertical Flip





Restriction: -

Default	Status	Default Value	
	Power On Sequence	3600h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

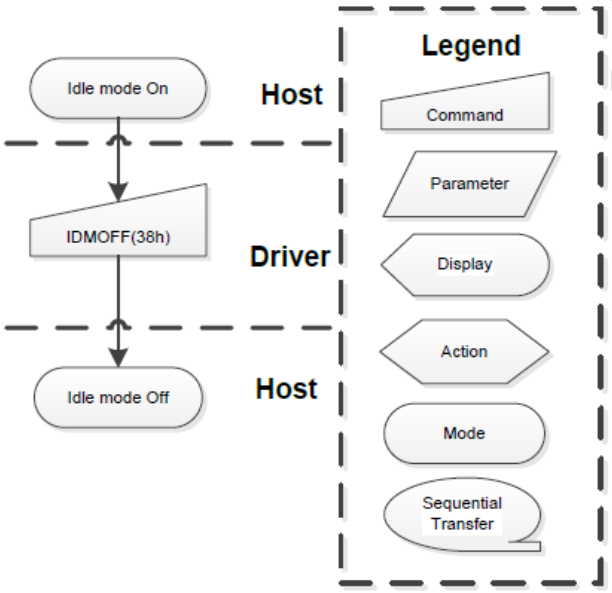
Flow Chart	

IDMOFF (3800h): Idle Mode Off

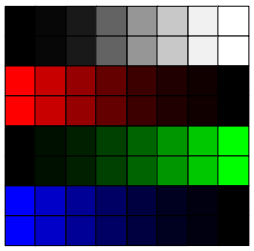
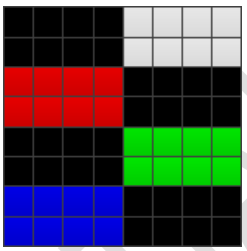
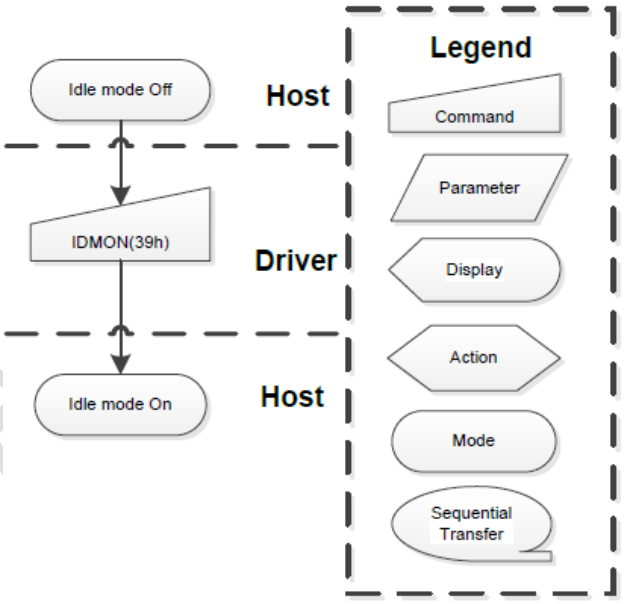
3800H	IDMOFF											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
IDMOFF	W	38h	3800h	-	No Parameter							
Description	This command cause display module to exit *Idle* mode.											
Restriction	This command has no effect when display module is not in *Idle* mode.											

Default	Status	Default Value	
	Power On Sequence	3800h	Idle mode off
	SW Reset	The same as above	
	HW Reset	The same as above	

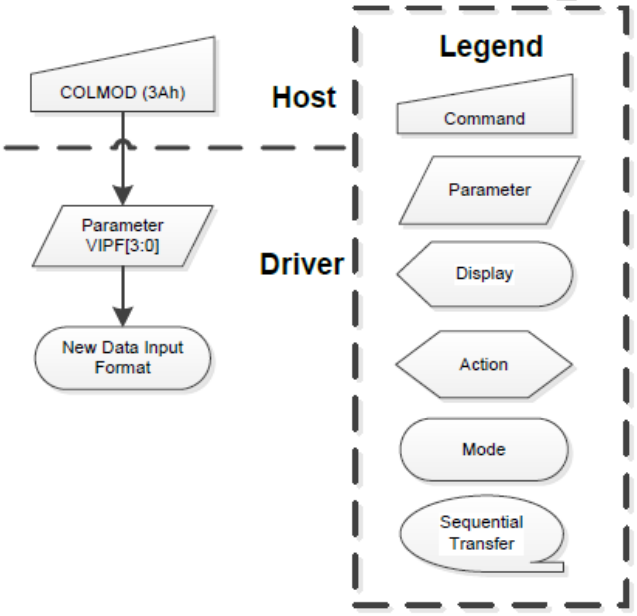
Flow Chart



IDMON (3900h): Idle Mode On

<table>
<tr><td>3900H</td><td colspan="12">IDMON</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>IDMON</td><td>W</td><td>39h</td><td>3900h</td><td>-</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command cause display module to enter Idle mode. In the idle mode, color expression is reduced.
Input Image
 
Display
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when display module is already in Idle mode.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td colspan="2">Default Value</td></tr><tr><td>Power On Sequence</td><td>3900h</td><td>Idle mode off</td></tr><tr><td>SW Reset</td><td colspan="2">The same as above</td></tr><tr><td>HW Reset</td><td colspan="2">The same as above</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

COLMOD (3A00h): Interface Pixel Format

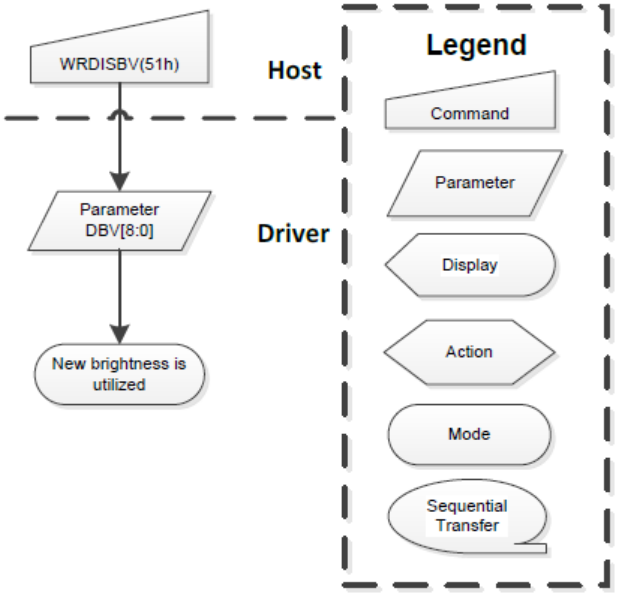
<table>
<tr><td>3A00H</td><td colspan="12">COLMOD</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>COLMOD</td><td>R/W</td><td>3Ah</td><td>3A00h</td><td>-</td><td colspan="5">D[7:4]</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current pixel format of the display:
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D[7:4]</td><td>VIPF[3:0]</td><td>DPI Pixel Format</td><td>7=24-bit/pixel
Others=Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>3A00h</td><td>70h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

WRDISBV (5100h): Write Display Brightness

5100H	WRDISBV										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	W	51h	5100h	-	DBV[7:0]							
			5101h	-	-	-	-	-	-	-	-	DBV [8]
Description	This command is used to adjust brightness.											
Restriction	-											

Default	Status	Default Value	
	Power On Sequence	5100h	00h
		5101h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart



WRCTRLD (5300h): Write CTRL Display

5300H	WRCTRLD										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	W	53h	5300h	-	-	-	D5	-	D3	D2	-	D0

Description

This command is used to set brightness control and display dimingcontrol.

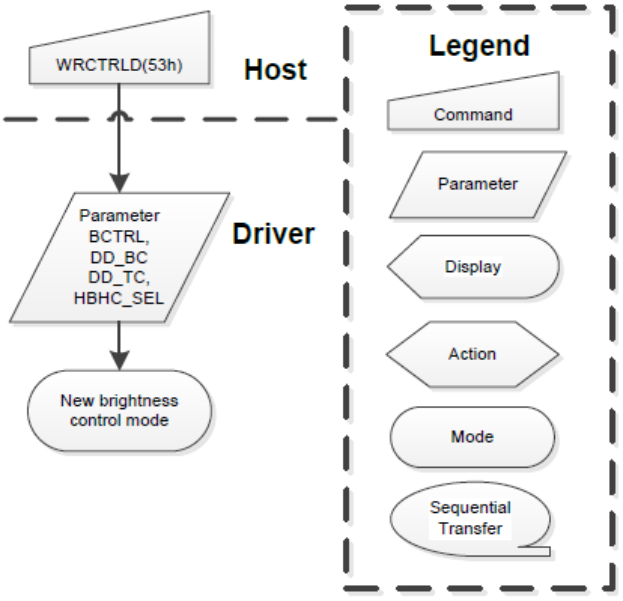
Bit	Symbol	Description	Comment
D5	BCTRL	Brightness control	1= Brightness control enable 0= Brightness control disable
D3	DD_BC	Display dimming control	1= Display dimming control enable 0= Display dimming control disable
D2	DD_TC	Temperature index dimming control	1 = Temperature dimming control enable 0 = Temperature dimming control disable
D0	HBHC_SEL	Display mode control	1=High Brightness Low Contrast 0=Low Brightness High Contrast

Restriction: -

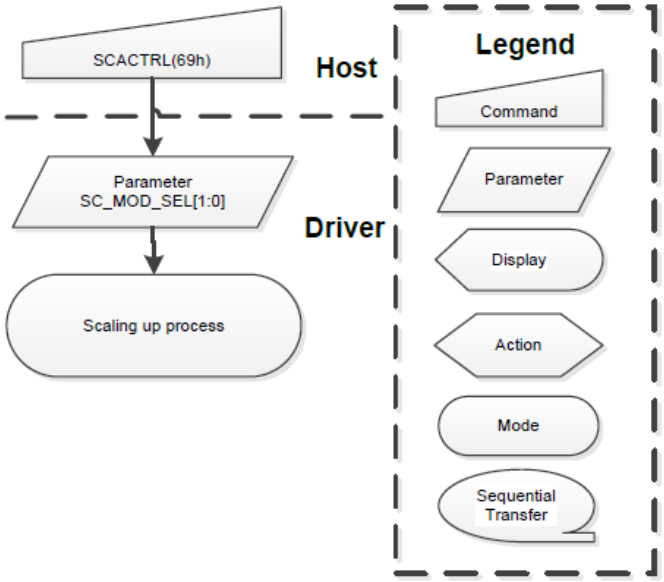
Default

Status	Default Value	
Power On Sequence	5300h	00h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart



SCACTRL (6900h): Scaling Up Control

<table>
<tr><td>6900H</td><td colspan="12">SCACTRL</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>SCACTRL</td><td>R/W</td><td>69h</td><td>6900h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="2">D[1:0]</td></tr>
<tr><td>Description</td><td colspan="12">This command sets operation mode of MIPI clock lane during porch time.
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D[1:0]</td><td>SC_MOD_SEL</td><td>Scaling up ratio selection</td><td>0= off
1= 2x scaling up
2=1.33x scaling up
3= reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>6900h</td><td>00h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

IFCONF (6B00h): Interface Configure

6900H	IFCONFG											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
IFCONFG	R/W	6Bh	6B00h	-	-	-	-	D4	-	-	-	-

Description

PORT_1_2_SEL_CMD1: Set MIPI Port1 or Port2 selection. XOR with PORT1_2_SEL (CMD2 page0 B102 D7).

Bit	Symbol	Description	Comment
D4	PORT1_2_SEL_CMD1	MIPI 1 port or 2 port selection	Refer to the table below

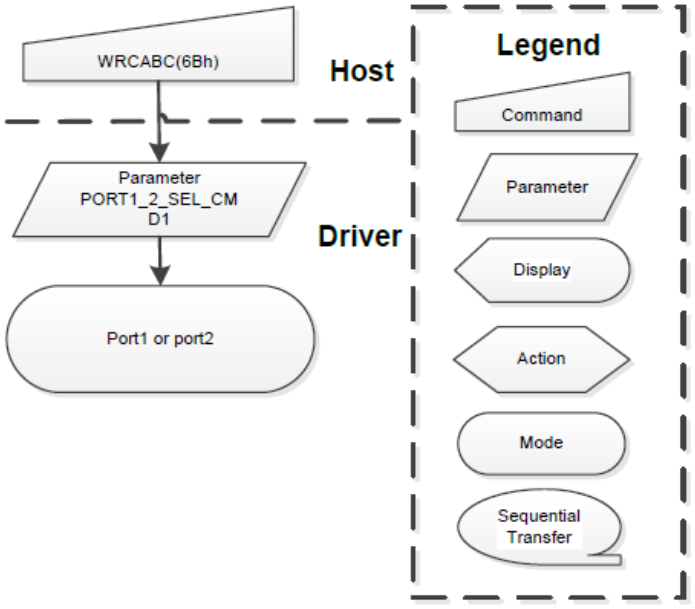
PORT_1_2_SEL_CMD1 (CMD1)	PORT1_2_SEL (CMD2 p0)	MIPI Port Selection
0h	0h	1-Port
0h	1h	2-Port
1h	0h	2-port
1h	1h	1-port

Restriction: -

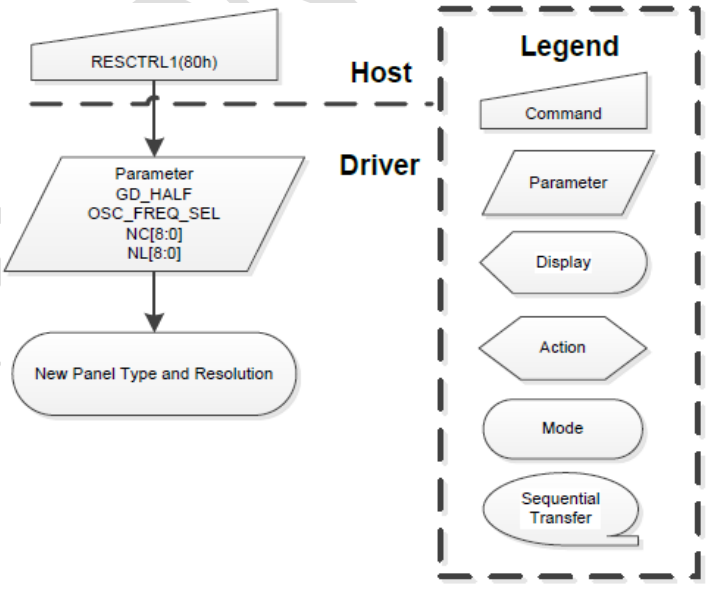
Default

Status	Default Value	
Power On Sequence	6B00h	10h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart



RESCTRL1 (8000h): Resolution Control1

<table>
<tr><td>8000H</td><td colspan="12">RESCTRL1</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="4">RESCTRL 1</td><td rowspan="4">R/W</td><td rowspan="4">80h</td><td>8000h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>D0</td></tr>
<tr><td>8001h</td><td>-</td><td colspan="9">NC[7:0]</td></tr>
<tr><td>8002h</td><td>-</td><td colspan="9">NL[7:0]</td></tr>
<tr><td>8003h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>NC[8]</td><td>-</td><td>-</td><td>-</td><td>NL[8]</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set panel type and display resolution.
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D0</td><td>OSC_FREQ_SEL</td><td>OSC frequency selection</td><td>0= 69.75MHz
1= 93MHz</td></tr>
<tr><td>D[8:0]</td><td>NC[8:0]</td><td>X-axis resolution</td><td>X-axis resolution= NC[8:0]*8</td></tr>
<tr><td>D[8:0]</td><td>NL[8:0]</td><td>Y-axis resolution</td><td>Y-axis resolution= NL[8:0]*8</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Resolution switch is only valid in SLPIN mode.</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td rowspan="4">Power On Sequence</td><td>8000h</td><td>01h</td></tr>
<tr><td>8001h</td><td>40h</td></tr>
<tr><td>8002h</td><td>40h</td></tr>
<tr><td>8003h</td><td>11h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

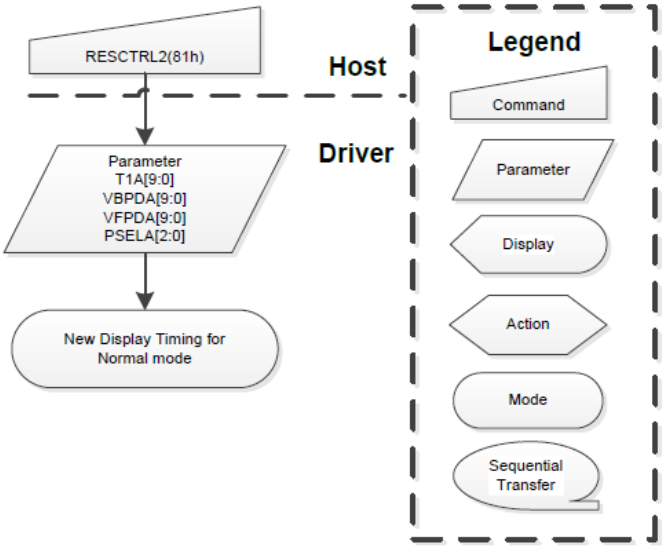
RESCTRL2 (8100h): Resolution Control2

8100H	RESCTRL2										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL 2	R/W	81h	8100h	-	-	-	-	-	-	-	T1A[9:8]	
			8101h	-	T1A[7:0]							
			8102h	-	-	-	-	-	-	-	VBPDA[9:8]	
			8103h	-	VBPDA[7:0]							
			8104h	-	-	-	-	-	-	-	VFPDA[9:8]	
			8105h	-	VFPDA[7:0]							
			8106h	-	-	-	-	-	-	PSELA[2:0]		

Description

This command is used to set panel type and display resolution.

Bit	Symbol	Description	Comment	
D[9:0]	T1A[9:0]	Clock number of 1-Hsync for data path in normal mode	T1A[9:0]	Number of Clock
			0h	1-dpclk
			1h	2-dpclk
			:	:
			3FEh	1023-dpclk
			3FFh	1024-dpclk
D[9:0]	VBPDA[9:0]	VBP line number in normal mode	VBPDA[9:0]	Line Number of VBP
			0~1h	Reserved
			2h	2-dpclk
			:	:
			3FBh	1019-dpclk
			3FC~3FFh	Reserved
D[9:0]	VFPDA[8:0]	VFP line number in normal mode	VFPDA[9:0]	Line Number of VFP
			0~1h	Reserved
			2h	2-dpclk
			:	:
			3FEh	1022-dpclk
			3FFh	1023-dpclk
D[2:0]	PSELA[2:0]	OSC divisor for data path in normal mode	PSELA[2:0]	OSC divisor
			0h	1
			1h	2
			2h	3
			3h	4
			4h	6
			5h	8
			6h	12
			7h	24

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td rowspan="7">Power On Sequence</td><td>8100h</td><td>01h</td></tr>
<tr><td>8101h</td><td>54h</td></tr>
<tr><td>8102h</td><td>00h</td></tr>
<tr><td>8103h</td><td>08h</td></tr>
<tr><td>8104h</td><td>00h</td></tr>
<tr><td>8105h</td><td>10h</td></tr>
<tr><td>8106h</td><td>00h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

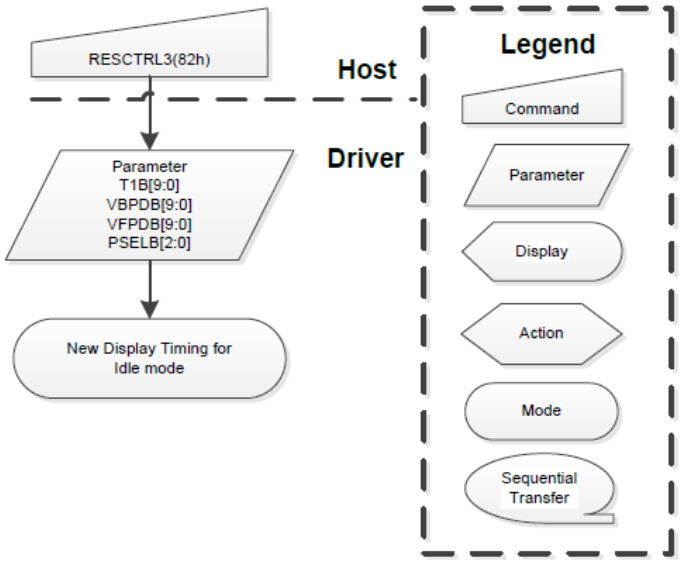
RESCTRL3 (8200h): Resolution Control3

8200H	RESCTRL3										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL 3	R/W	82h	8200h	-	-	-	-	-	-	-	T1B[9:8]	
			8201h	-	T1B[7:0]							
			8202h	-	-	-	-	-	-	-	VBPDB[9:8]	
			8203h	-	VBPDB[7:0]							
			8204h	-	-	-	-	-	-	-	VFPDB[9:8]	
			8205h	-	VFPDB[7:0]							
			8206h	-	-	-	-	-	-	PSELB[2:0]		

Description

This command is used to set panel type and display resolution.

Bit	Symbol	Description	Comment	
D[9:0]	T1B[9:0]	Clock number of 1-Hsync for data path in idle mode	T1B[9:0]	Number of Clock
			0h	1-dpclk
			1h	2-dpclk
			:	:
			3FEh	1023-dpclk
			3FFh	1024-dpclk
D[9:0]	VBPDB[9:0]	VBP line number in idle mode	VBPDB[9:0]	Line Number of VBP
			0~1h	Reserved
			2h	2-dpclk
			:	:
			3FBh	1019-dpclk
			3FC~3FFh	Reserved
D[9:0]	VFPDB[8:0]	VFP line number in idle mode	VFPDB[9:0]	Line Number of VFP
			0~1h	Reserved
			2h	2-dpclk
			:	:
			3FEh	1022-dpclk
			3FFh	1023-dpclk
D[2:0]	PSELB[2:0]	OSC divisor for data path in idle mode	PSELB[2:0]	OSC divisor
			0h	1
			1h	2
			2h	3
			3h	4
			4h	6
			5h	8
			6h	12
			7h	24

<table>
<tr><td>Restriction</td><td colspan="3">-</td></tr>
<tr><td rowspan="10">Default</td><td colspan="3"><table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td rowspan="8">Power On Sequence</td><td>8200h</td><td>01h</td></tr>
<tr><td>8201h</td><td>54h</td></tr>
<tr><td>8202h</td><td>00h</td></tr>
<tr><td>8203h</td><td>08h</td></tr>
<tr><td>8204h</td><td>00h</td></tr>
<tr><td>8205h</td><td>10h</td></tr>
<tr><td>8206h</td><td>01h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="3"> 
</td></tr>
</table>

PORCH_EXT (8300h): Porch CTRL

<table>
<tr><td>8300H</td><td colspan="12">PORCH_EXT</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="3">PORCH_EXT</td><td rowspan="3">R/W</td><td rowspan="3">83h</td><td>8300h</td><td>-</td><td colspan="2">VBP_EXT[9:8]</td><td colspan="2">VFP_EXT[9:8]</td><td>-</td><td>-</td><td>-</td><td>D0</td></tr>
<tr><td>8301h</td><td>-</td><td colspan="8">VBP_EXT[7:0]</td></tr>
<tr><td>8302h</td><td>-</td><td colspan="8">VFP_EXT[7:0]</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set porch setting under displaying data with externaltiming.
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D0</td><td>EN_VBP_VFP_EXT</td><td>Enable VBP/VFP setting under DM=1</td><td>1= refer to setting of VBP_EXT and VFP_EXT
0=refer to Host's external timing</td></tr>
<tr><td>D[9:0]</td><td>VBP_EXT[9:0]</td><td>The porch line number of VBP when EN_VBP_VFP_EXT=1</td><td>-</td></tr>
<tr><td>D[9:0]</td><td>VFP_EXT[9:0]</td><td>The porch line number of VFP when EN_VBP_VFP_EXT=1</td><td>-</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th colspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><td colspan="2" rowspan="3">Power On Sequence</td><td>8300h</td><td>00h</td></tr>
<tr><td>8301h</td><td>20h</td></tr>
<tr><td>8302h</td><td>20h</td></tr>
<tr><td colspan="2">SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td colspan="2">HW Reset</td><td colspan="2">The same as above</td></tr>
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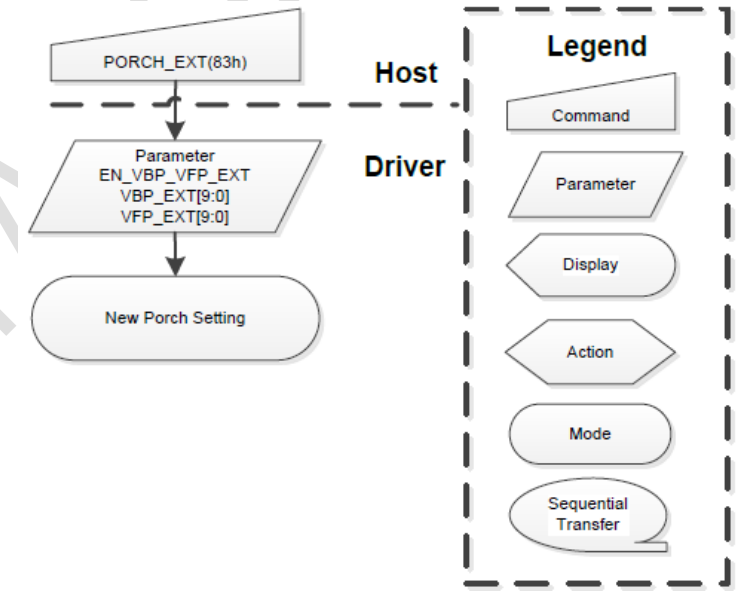
<tr><td>Flow Chart</td><td colspan="12"> 
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