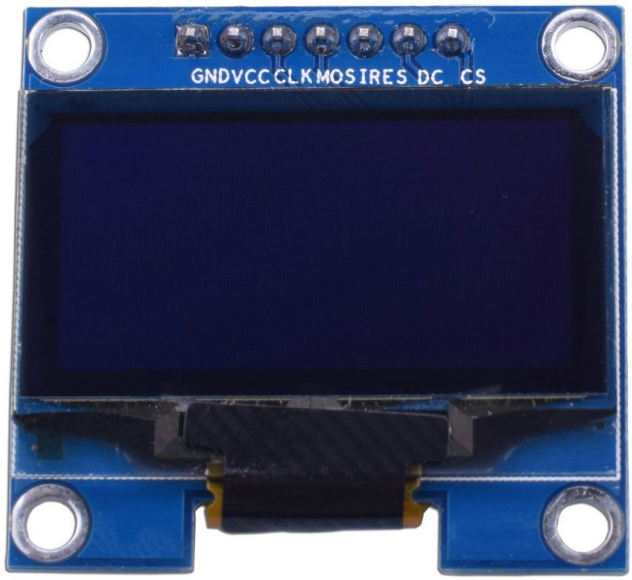
DisplayModule



DM-OLED13-627

1.3” 128 X 64 WHITE GRAPHIC OLED DISPLAY MODULE WITH SPI, I2C INTERFACE

Contents

1 Revision History

Date	Changes
2015-12-28	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.3	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome (White)	Colors
Resolution	128 x 64	pixel
Controller IC	SH1106	-
Duty	1/64	
Interface	SPI, I2C	-
Active Area	29.42 x 14.7	mm
Panel Dimension	34.5 x 23.0 x 1.4	mm
Weight	2.18	g

3 Pin Description

3.1 Panel Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1</td><td>NC</td><td>No Connection</td></tr>
<tr><td>2-3
4-5</td><td>C2P/C2N
C1P/C1N</td><td>Positive Terminal of the Flying Inverting Capacitor
Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>6</td><td>VBAT</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter.This pin should be disconnected when VPP is supplied externally</td></tr>
<tr><td>7-8</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>9</td><td>VDD</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>10</td><td>NC</td><td>No Connection</td></tr>
<tr><td>11
12</td><td>BS1
BS2</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS1</th><th>BS2</th></tr>
<tr><td>I2C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>13</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>14</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>15</td><td>D/C#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input atD7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>16</td><td>R/W#</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.</td></tr>
</table>

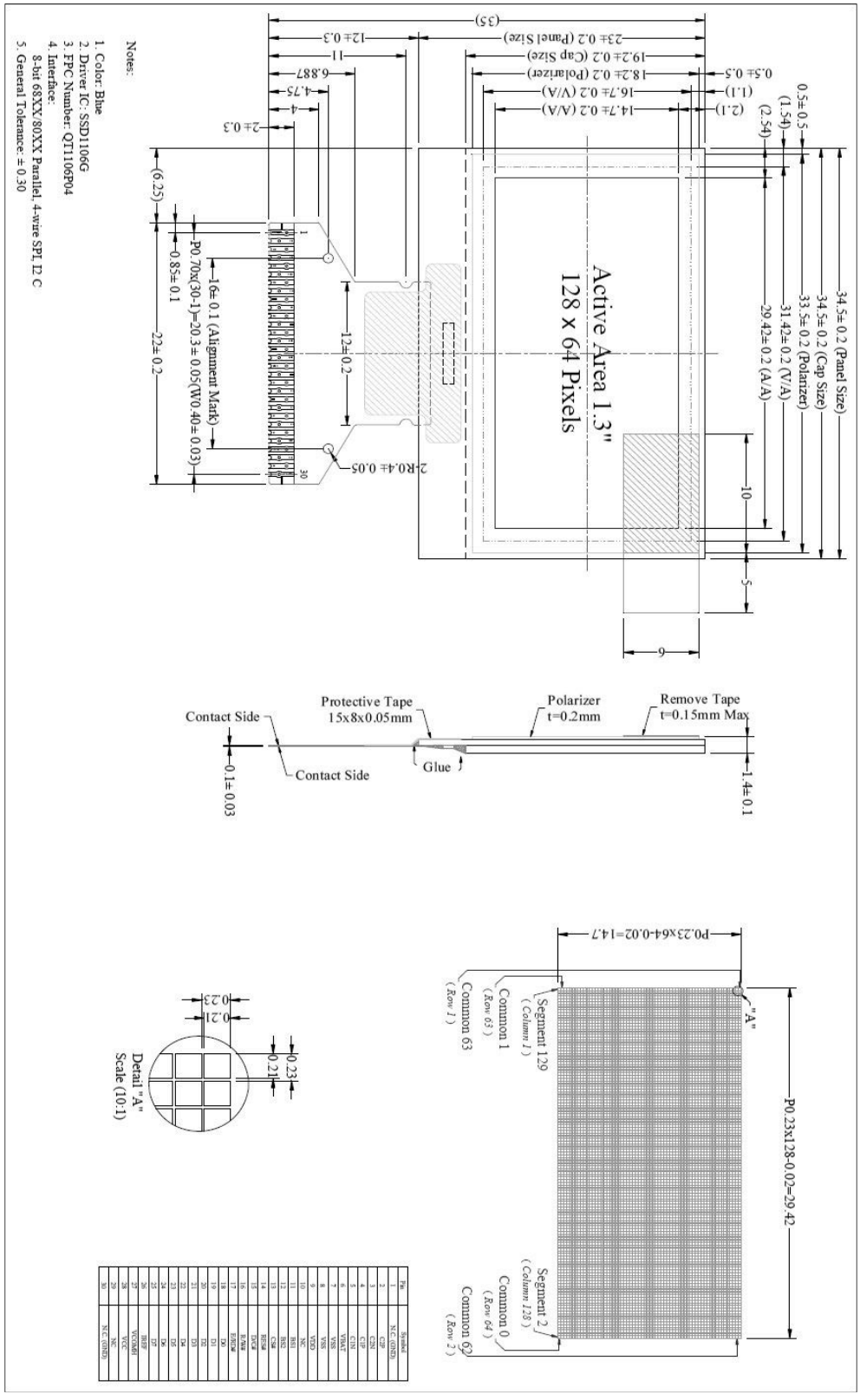
		When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
17	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-seriesmicroprocessor, this pinwill be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#)signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
18-25	D0-D7	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.
26	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5A maximum.
27	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
28	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
29	NC	No Connection
30	NC	No Connection

3.2 Module Pin Description

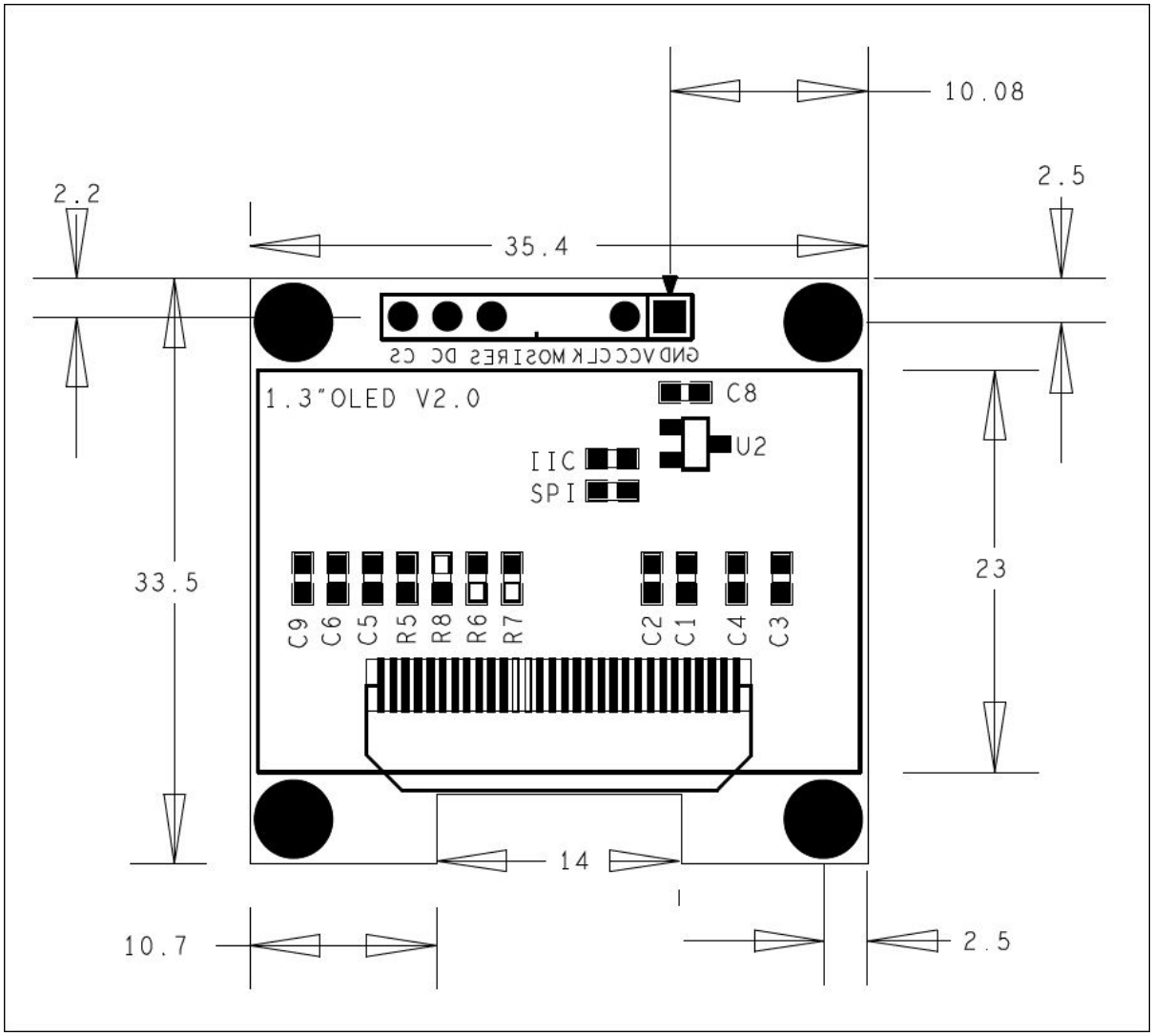
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC_IN	Power Supply
3 4	D0 D1	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.
5	RES	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
6	D/C	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input atD7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
7	CS	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage for Logic	VDD		1.62	2.8	3.3	V
Operating Current	ICC	Note 1		23	32	mA
Low Level Input Voltage	V_{IL}		0	-	$0.2xV_{DD}$	V
High Level Input Voltage	V_{IH}		$0.8xV_{DD}$	-	V_{DD}	V
Low Level Output Voltage	V_{OL}		0		$0.1xV_{DD}$	V
High Level Output Voltage	V_{OH}		$0.9xV_{DD}$		V_{DD}	V
Operating Temperature	TOP	Absolute Max	-40		85	℃
Storage Temperature	TST	Absolute Max	-40		85	℃

Note 1: VDD = 2.8V, VCC = 12V, IREF=910K 100% Display Area Turn on.

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles			Free		°
Response Time (25°C)	Tr + Tf				us
Brightness			100		cd/m²
Contrast Ratio	CR		2,000:1		
Lifetime		10,000			Hrs

7 Timing Characteristics

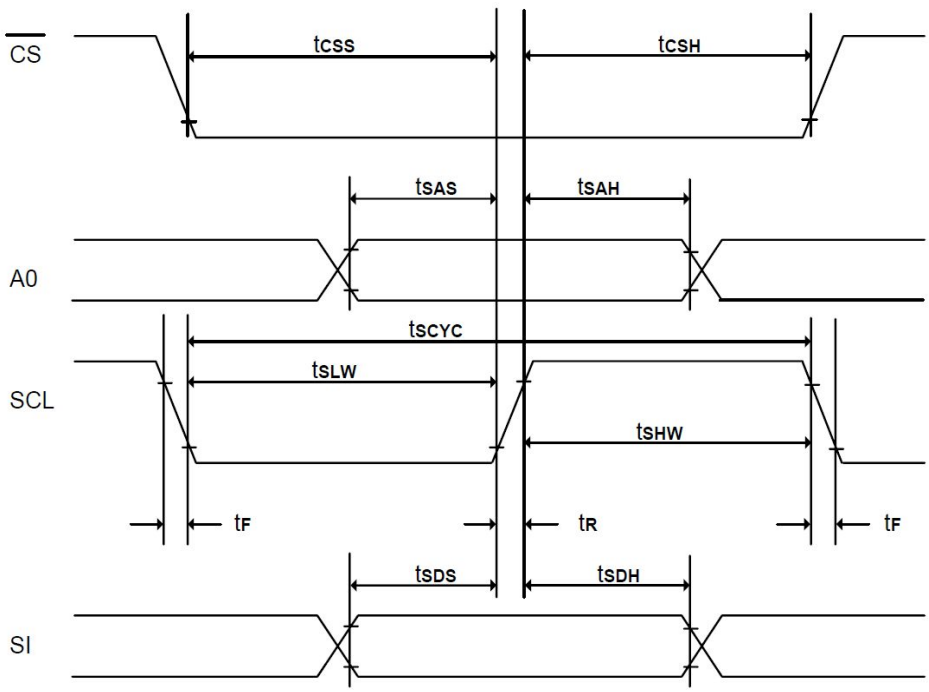
7.1 Serial Interface Timing Characteristics (4-wire SPI)

TA=25℃,VDD1=1.65-3.5V

Symbol	Item	Min	Typ	Max	Unit
t_{SCYCS}	Serial Clock Cycle	500	-	-	ns
t_{SAS}	Address Setup Time	300	-	-	ns
t_{SAH}	Address Hold Time	300	-	-	ns
t_{SDS}	Data Setup Time	200	-	-	ns
t_{SDH}	Data Hold Time	200	-	-	ns
t_{CSS}	Chip Select Setup Time	240	-	-	ns
t_{CSH}	Chip Select Hold Time	120	-	-	ns
t_{SHW}	Serial Clock H Pulse Width	200	-	-	ns
t_{SLW}	Serial Clock L Pulse Width	200	-	-	ns
t_R	Rise Time	-	-	30	ns
t_F	Fall Time	-	-	30	ns

TA=25℃,VDD1=2.4-3.5V

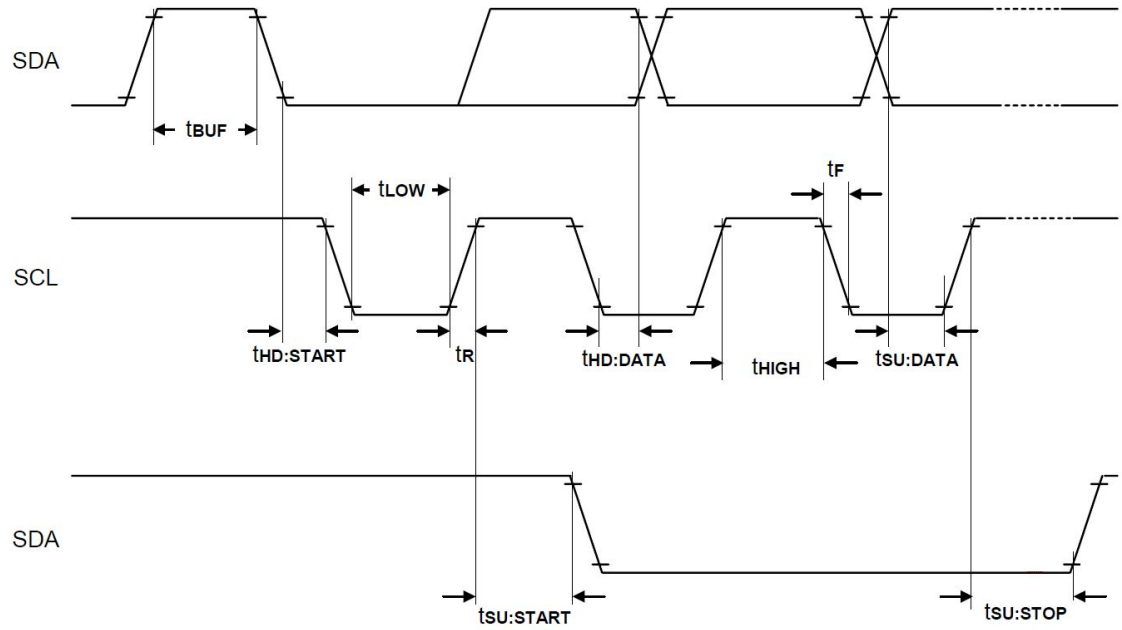
Symbol	Item	Min	Typ	Max	Unit
t_{SCYCS}	Serial Clock Cycle	250	-	-	ns
t_{SAS}	Address Setup Time	150	-	-	ns
t_{SAH}	Address Hold Time	150	-	-	ns
t_{SDS}	Data Setup Time	100	-	-	ns
t_{SDH}	Data Hold Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{SHW}	Serial Clock H Pulse Width	100	-	-	ns
t_{SLW}	Serial Clock L Pulse Width	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



7.2 I2C Interface Timing Characteristics

TA=25℃,VDD1=1.65-3.5V

Symbol	Item	Min	Typ	Max	Unit
fSCL	SCL Clock Frequency	DC	-	400	kHZ
t_{LOW}	SCL Clock Low Pulse Width	1.3	-	-	μs
t_{HIGH}	SCL Clock High Pulse Width	0.6	-	-	μs
$t_{SU:DATA}$	Data Setup Time	100	-	-	ns
$t_{HD:DATA}$	Data Hold Time	0	-	0.9	μs
t_R	SCL, SDA Rise Time	20+0.1Cb	-	300	ns
t_F	SCL, SDA Fall Time	20+0.1Cb	-	300	ns
Cb	Capacity Load on Each Bus Line	-	-	400	pF
$t_{SU:START}$	Setup Time for Re-START	0.6	-	-	μs
$t_{HD:START}$	START Hold time	0.6	-	-	μs
$t_{SU:STOP}$	Setup time for STOP	0.6	-	-	μs
t_{BUF}	Bus Free Times between STOP and START Condition	1.3		-	μs



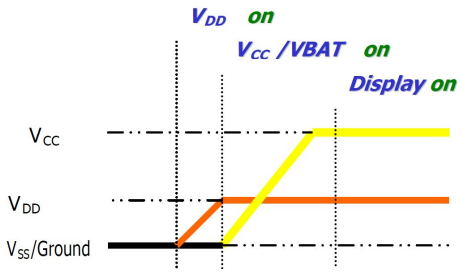
8 Functional Specification

8.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

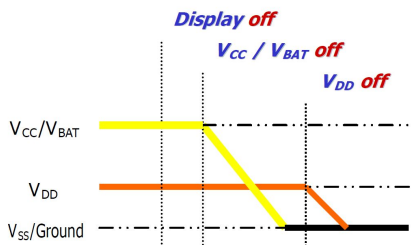
Power up Sequence

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/V_{BAT}
6. Delay 100ms(When V_{CC} is stable)
7. Send Display on command



Power down Sequence

1. Send Display off command
2. Power down V_{CC}/V_{BAT}
3. Delay 100ms (When V_{CC}/V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



8.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

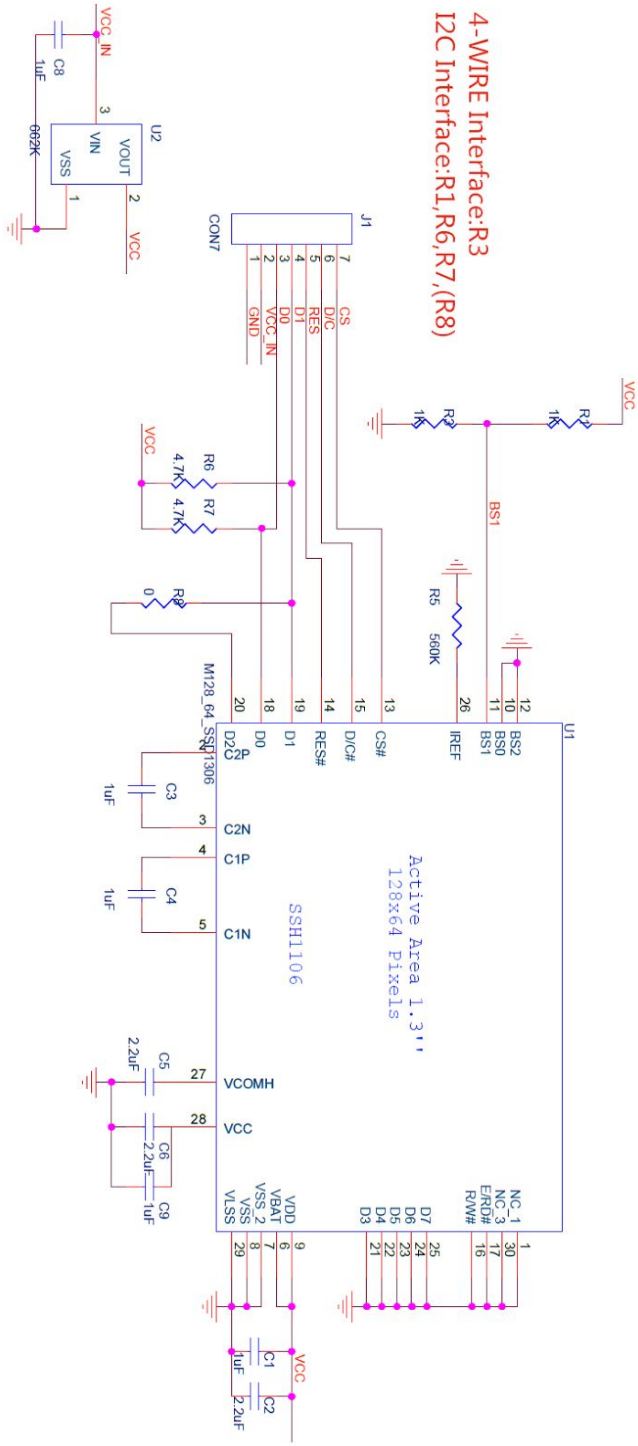
1. Display is OFF
2. 12864 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

9 Driver/Controller Information

Built-in SH1106 Controller:

https://drive.google.com/file/d/0B5lkVYnewKTGZDEtWU9JYWVmSms/view?usp=sharing

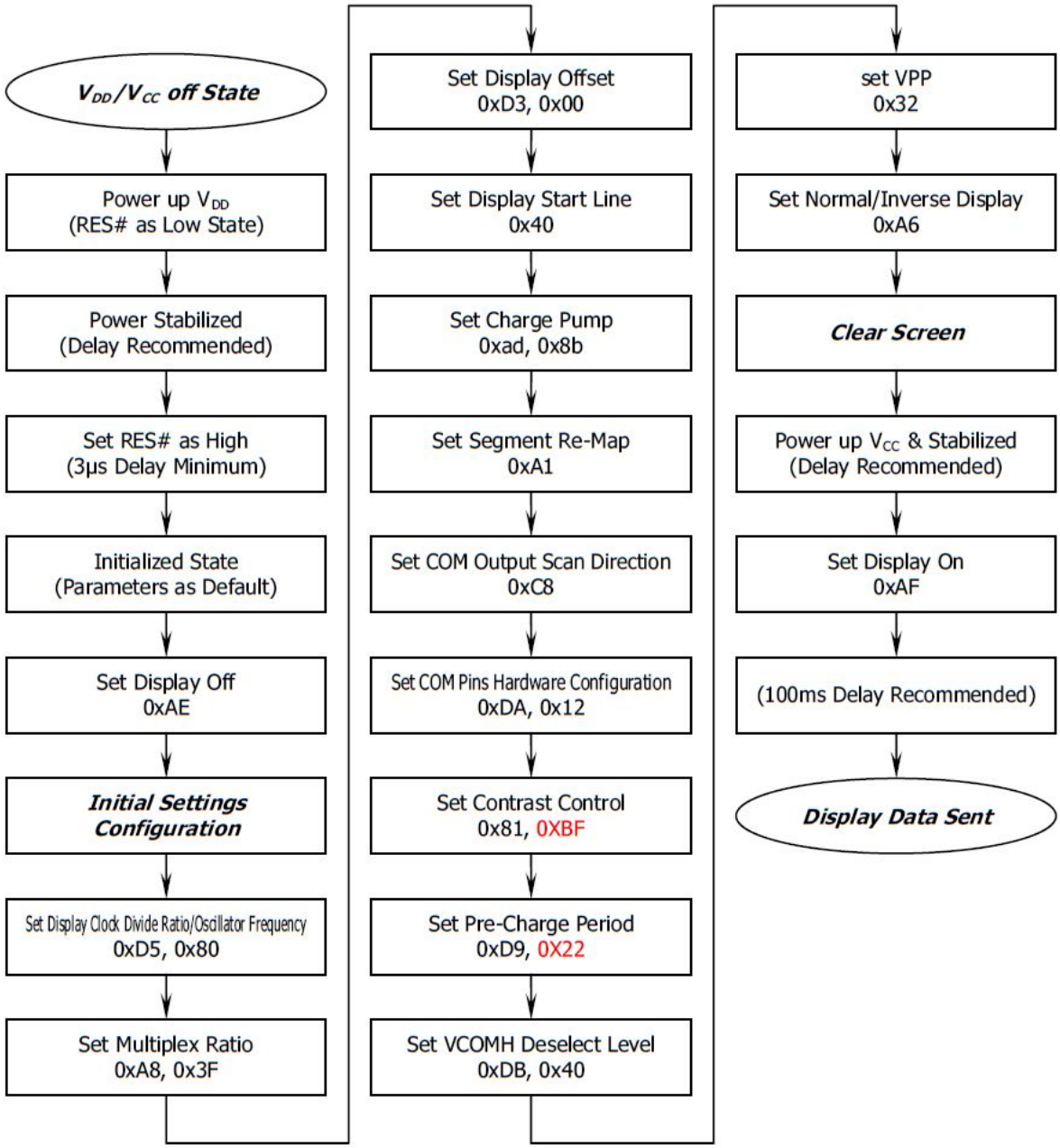
10 Module Schematic



11 Example Application

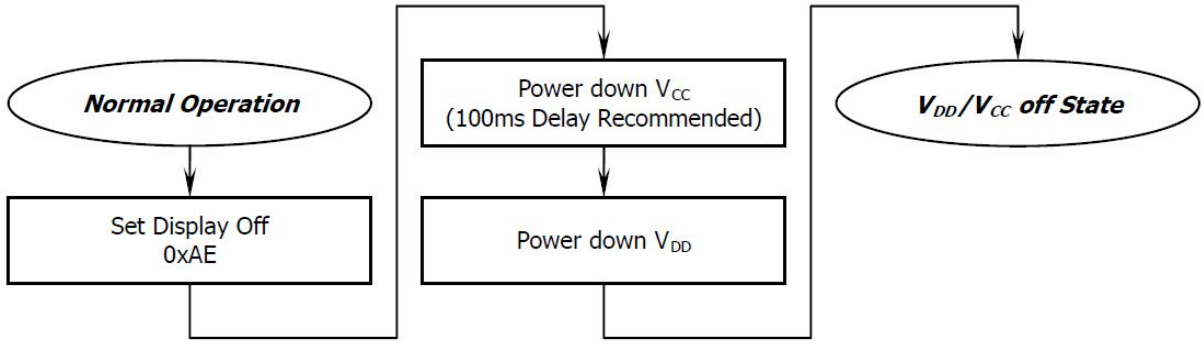
VCC Supplied Externally

<Power up Sequence>

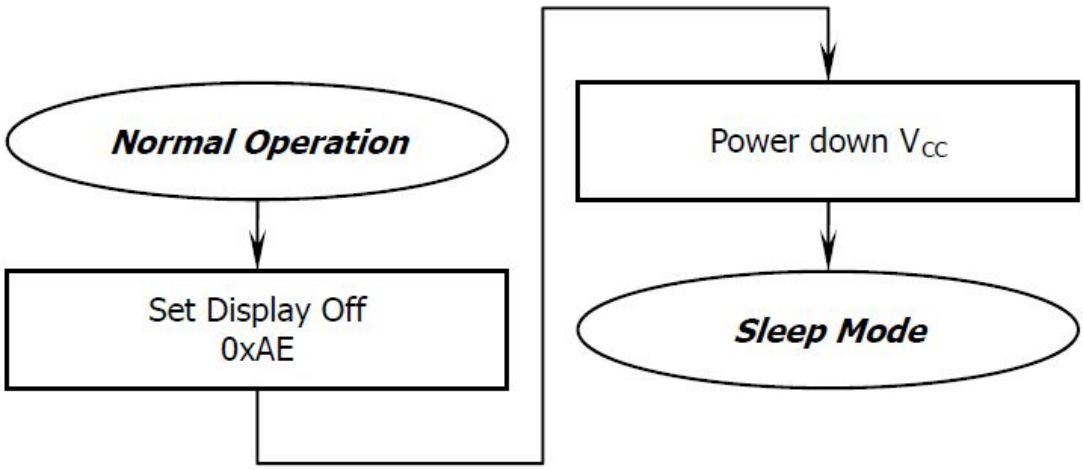


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

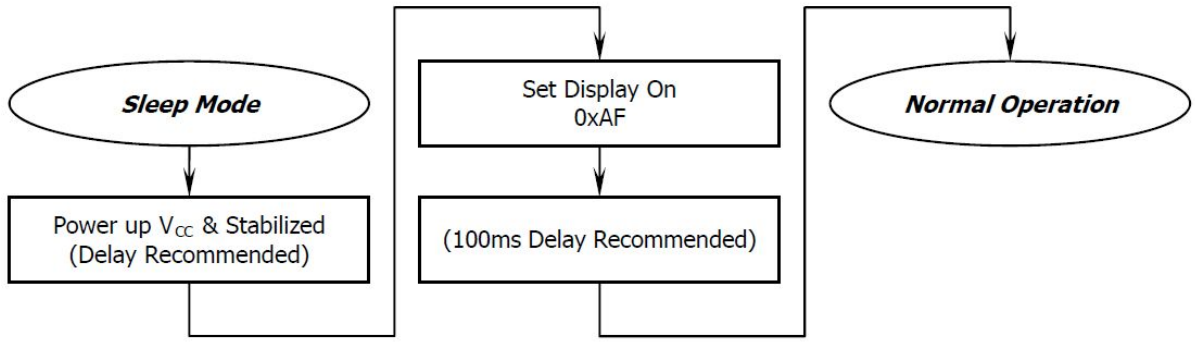
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting

```
{
        RES=1;
        delay(1000);
        RES=0;
        delay(1000);
        RES=1;
        delay(1000);
        write_i(0xAE);      /*display off*/
```

```
                write_i(0x02);       /*set lower column address*/
                write_i(0x10);      /*set higher column address*/

                write_i(0x40);      /*set display start line*/

                write_i(0xB0);      /*set page address*/

                write_i(0x81);       /*contract control*/
                write_i(0xBF);       /*128*/

                write_i(0xA1);       /*set segment remap*/

                write_i(0xA6);       /*normal / reverse*/

                write_i(0xA8);      /*multiplex ratio*/
                write_i(0x3F);       /*duty = 1/64*/

                write_i(0xad);       /*set charge pump enable*/
                write_i(0x8a);       /* 0x8a  VCC */

                write_i(0x32);       /*0X30---0X33 set VPP 8V */

                write_i(0xC8);       /*Com scan direction*/

                write_i(0xD3);       /*set display offset*/
                write_i(0x00);        /* 0x20 */

                write_i(0xD5);       /*set osc division*/
                write_i(0x80);

                write_i(0xD9);       /*set pre-charge period*/
                write_i(0x22);       /*0x22*/

                write_i(0xDA);       /*set COM pins*/
                write_i(0x12);

                write_i(0xdb);       /*set vcomh*/
                write_i(0x40);

                write_i(0xAF);        /*display ON*/
                }
void write_i(unsigned char ins)
{
        DC=0;
        CS=0;
        WR=1;
        P1=ins;       /*inst*/
        WR=0;
```

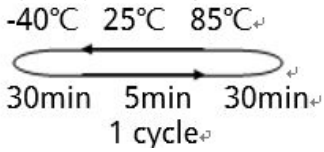
```
        WR=1;
        CS=1;
}

void write_d(unsigned char dat)
{
        DC=1;
        CS=0;
        WR=1;
        P1=dat;       /*data*/
        WR=0;
        WR=1;
        CS=1;
}
void delay(unsigned int i)
{
        while(i>0)
        {
        i--;
        }
}
```

12 Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Set Pump voltage value	0	1	0	0	0	1	1	0	0	Pump voltage value		This command is to control the DC-DC voltage output value. (POR=32H)
4. Set Display Start Line	0	1	0	0	1	Line address						Specifies RAM display line for COM0. (POR = 40H)
5. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
6. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
7. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
8. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
9 Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
Multiplex Ration Data Set	0	1	0	*	*	Multiplex Ratio						
10. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	1	0	1	D	

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
11. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
12. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
13. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
14. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H)
Display Offset Data Set	0	1	0	*	*	COMx						
15. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
16. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
17. Common Pads Hardware Configuration Mode Set	0	1	0	1	1	0	1	1	0	1	0	This command is to set the common signals pad configuration. (POR = 12H)
Sequential/Alternative Mode Set	0	1	0	0	0	0	D	0	0	1	0	
18. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM (β X V_{REF})								
19. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
20. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
21. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
22. Write Display Data	1	1	0	Write RAM data								
23. Read Status	0	0	1	BUSY	ON/ OFF	*	*	*	0	0	0	
24. Read Display Data	1	0	1	Read RAM data								

13 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 ℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40℃/85℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.
Note3: Test performed on product itself, not inside a container.

14 Warranty and Conditions

http://www.displaymodule.com/pages/faq