DisplayModule

DM-OLED118-655

1.18" 128 × 128 MONOCHROME GRAHIC OLED DISPLAY PANEL - MCU, SPI, I2C

Contents

1 Revision History

Date	Changes
2019-07-17	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.18	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome (White/Yellow/Blue)	Colors
Resolution	128 x 128	pixel
Controller IC	SSD1327ZB	-
Interface	6800/8080 MCU,SPI,I2C	-
Active Area	30.00×30.00	mm
Panel Dimension	36.98× 41.23 × 2.05	mm
Pixel Size	0.210 × 0.210	-
Pixel Pitch	0.235 × 0.235	mm
Drive Duty	1/128Duty	-
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

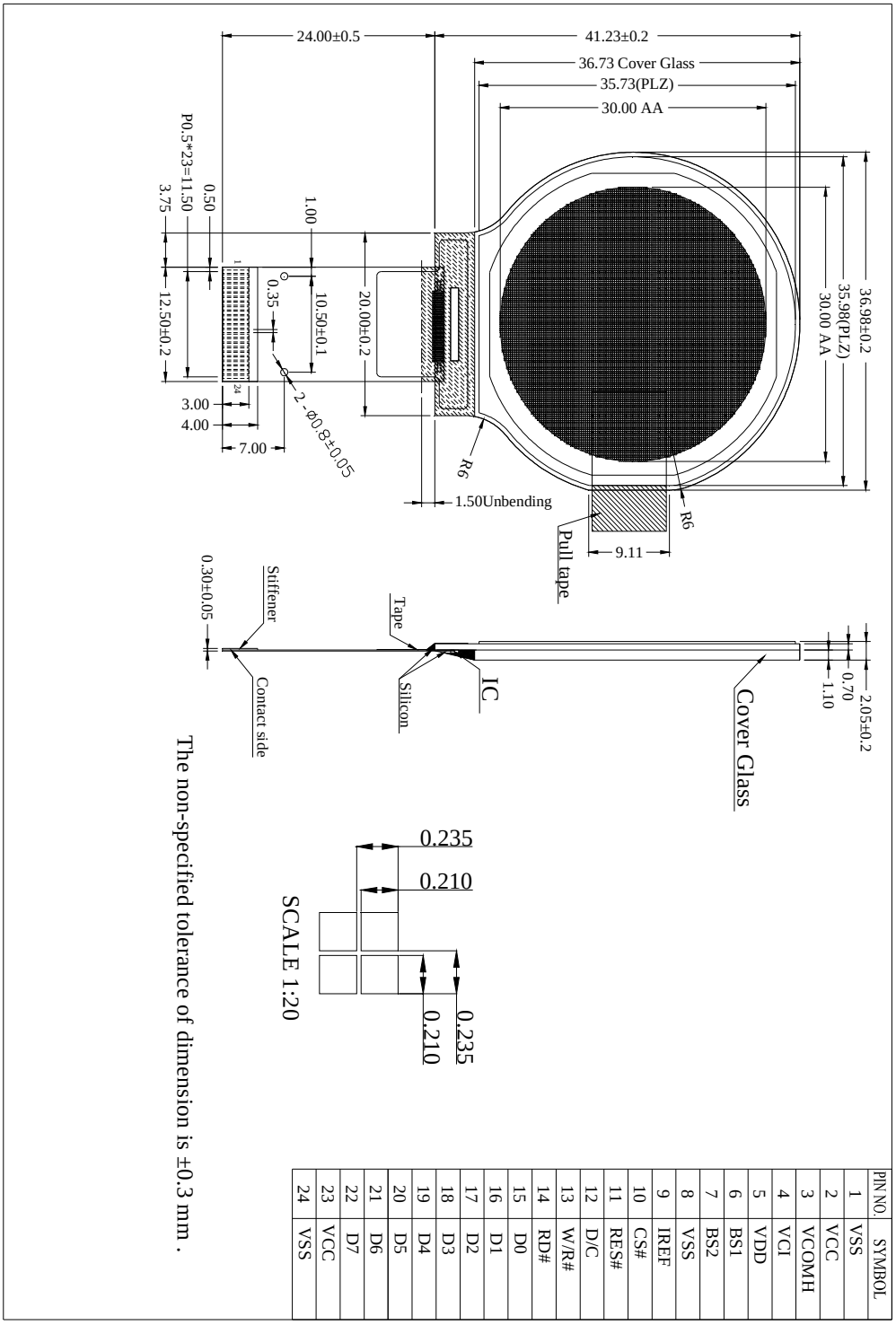
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1</td><td>VSS</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>2</td><td>VCC</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS. No external power supply is allowed to connect to this pin.</td></tr>
<tr><td>4</td><td>VCI</td><td>Low voltage power supply and power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source.
VCI must always set to be equivalent to or higher than VDD.</td></tr>
<tr><td>5</td><td>VDD</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>6</td><td>BS1</td><td rowspan="2">MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select.
Bus Interface selection<table><tr><td>BS[2:1]</td><td>Interface</td></tr><tr><td>00</td><td>4 line SPI</td></tr><tr><td>01</td><td>I2C</td></tr><tr><td>11</td><td>8-bit 8080 parallel</td></tr><tr><td>10</td><td>8-bit 6800 parallel</td></tr></table>Note (1) 0 is connected to VSS (2) 1 is connected to VCI</td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>9</td><td>IREF</td><td>This pin is the segment output current reference pin</td></tr>
<tr><td>10</td><td>CS#</td><td>This pin is the chip select input connecting to the MCU.
The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).</td></tr>
<tr><td>11</td><td>RES#</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>12</td><td>D/C</td><td>This pin is Data/Command control pin connecting to the MCU.
When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.
In I2C mode, this pin acts as SA0 for slave address selection.
When 3-wire serial interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>13</td><td>W/R#</td><td>This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.</td></tr>
<tr><td>14</td><td>RD#</td><td>This pin is MCU interface input.
When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.
Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
</table>

15	D0	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
16	D1	
17	D2	
18	D3	
19	D4	
20	D5	
21	D6	
22	D7	
23	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.
24	VSS	Ground pin.

Note: I=Input; O=Output; P=Power; I/O=Input / Output

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



PIN NO.	SYMBOL
1	VSS
2	VCC
3	VCOMH
4	VCI
5	VDD
6	BS1
7	BS2
8	VSS
9	IREF
10	CS#
11	RES#
12	D/C
13	W/R#
14	RD#
15	D0
16	D1
17	D2
18	D3
19	D4
20	D5
21	D6
22	D7
23	VCC
24	VSS

5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles	(V)θ	160	-	-	°	-
	(H)φ	160	-	-	°	-
Response Time	T rise	-	-	10	μs	-
	T fall	-	-	10	μs	-
C.I.E(White)	(x) (y)	0.26 0.30	0.28 0.32	0.30 0.34	-	CIE 1931
Contrast Ratio	CR	2000:1	-	-	-	Dark

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Operation Supply Voltage	V_{CI}	-0.3	4.0	V	Note1,2
Logic Supply Voltage	V_{DD}	-0.5	2.75	V	Note1,2
Display Supply Voltage	V_{CC}	-0.5	19	V	Note1,2
Operating Temperature	TOP	-40	+80	℃	-
Storage Temperature	TSTG	-40	+85	℃	-

Note1: All the above voltages are on the basis of “VSS = 0V”.

Note2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section6 “Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate

5.3 DC Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Remark
Logic Supply Voltage	V_{CI}	2.8	3.0	3.3	V	-
Display Supply Voltage	V_{CC}	14	14.5	15	V	-
Low Level Input Voltage	V_{IL}	0	-	0.2 x V_{CI}	V	-
High Level Input Voltage	V_{IH}	0.8 x V_{CI}	-	V_{CI}	V	-
Low Level Output Voltage	V_{OL}	0	-	0.1 x V_{CI}	V	-
High Level Output Voltage	V_{OH}	0.9 x V_{CI}	-	V_{CI}	V	-
50% Check Board operating Current		-	24	26	mA	V_{CC}=14.5V

Note1: The input digital voltage is the I/O reference voltage.

Note2: VDDIO usually ranges from 1.65V to 1.95 V. If VDDIO is changed, the remaining voltage needs to be changed to the same voltage as VDDIO.

5.4 AC Characteristics

5.4.1 6800-Series MCU Parallel Interface Timing Characteristics:

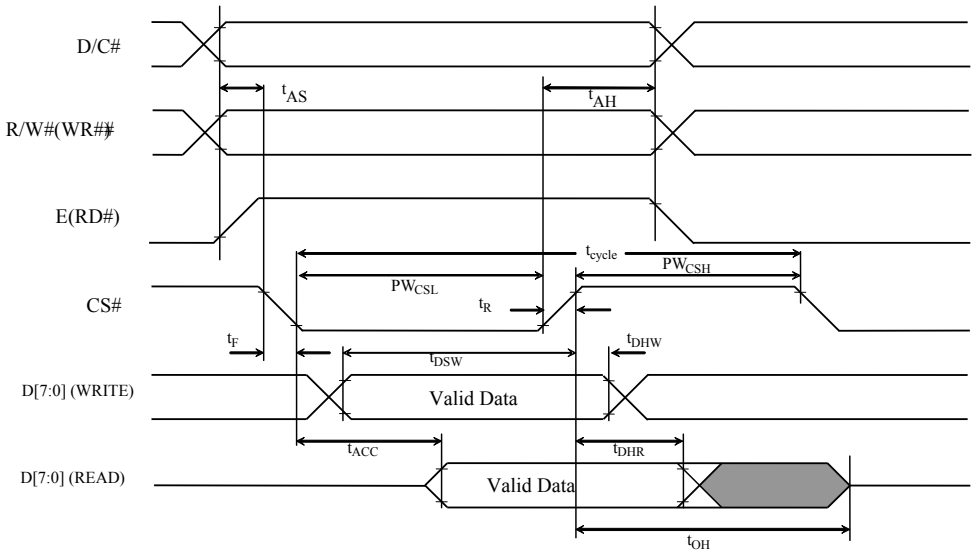
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	44	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	250	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{CI} -V_{SS} = 1.65V to 2.1V, T_A = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{CI} -V_{SS} = 2.1V to 3.5V, T_A = 25°C)

Figure 5-1 : 6800-series MCU parallel interface characteristics



5.4.2 8000-Series MCU Parallel Interface Timing Characteristics:

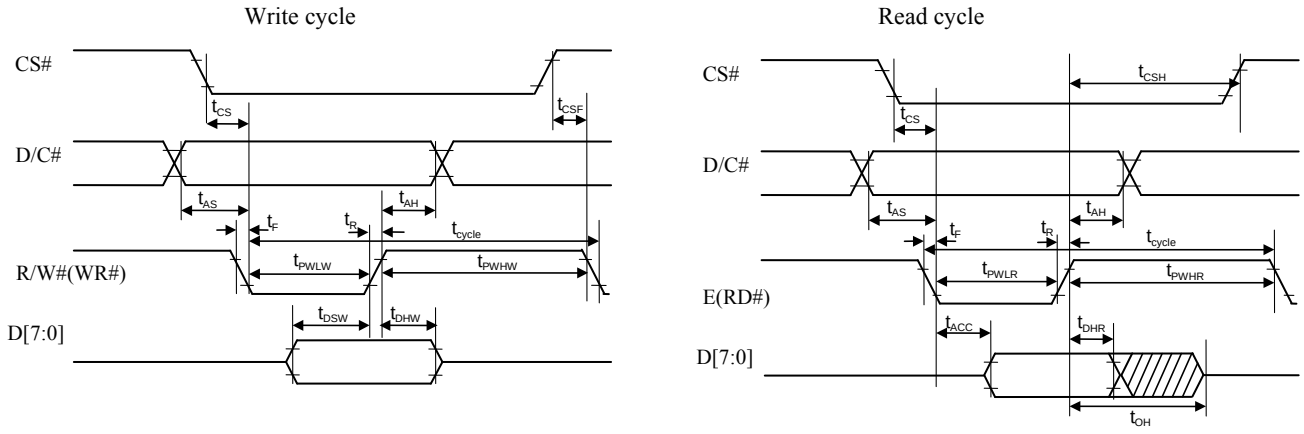
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	30	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	20	-	ns
t_{DHW}	Write Data Hold Time	42	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns
t_{CS}	Chip select setup time	0	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	ns
t_{CSF}	Chip select hold time	20	-	ns

* (V_{CI} -V_{SS} = 1.65V to 2.1V, T_A = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	18	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	14	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns
t_{CS}	Chip select setup time	0	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	ns
t_{CSF}	Chip select hold time	20	-	ns

* (V_{CI} -V_{SS} = 2.1V to 3.5V, T_A = 25°C)

Figure 5-2 : 8080-series MCU parallel interface characteristics



5.4.3 Serial Interface Timing Characteristics:4-wire Serial

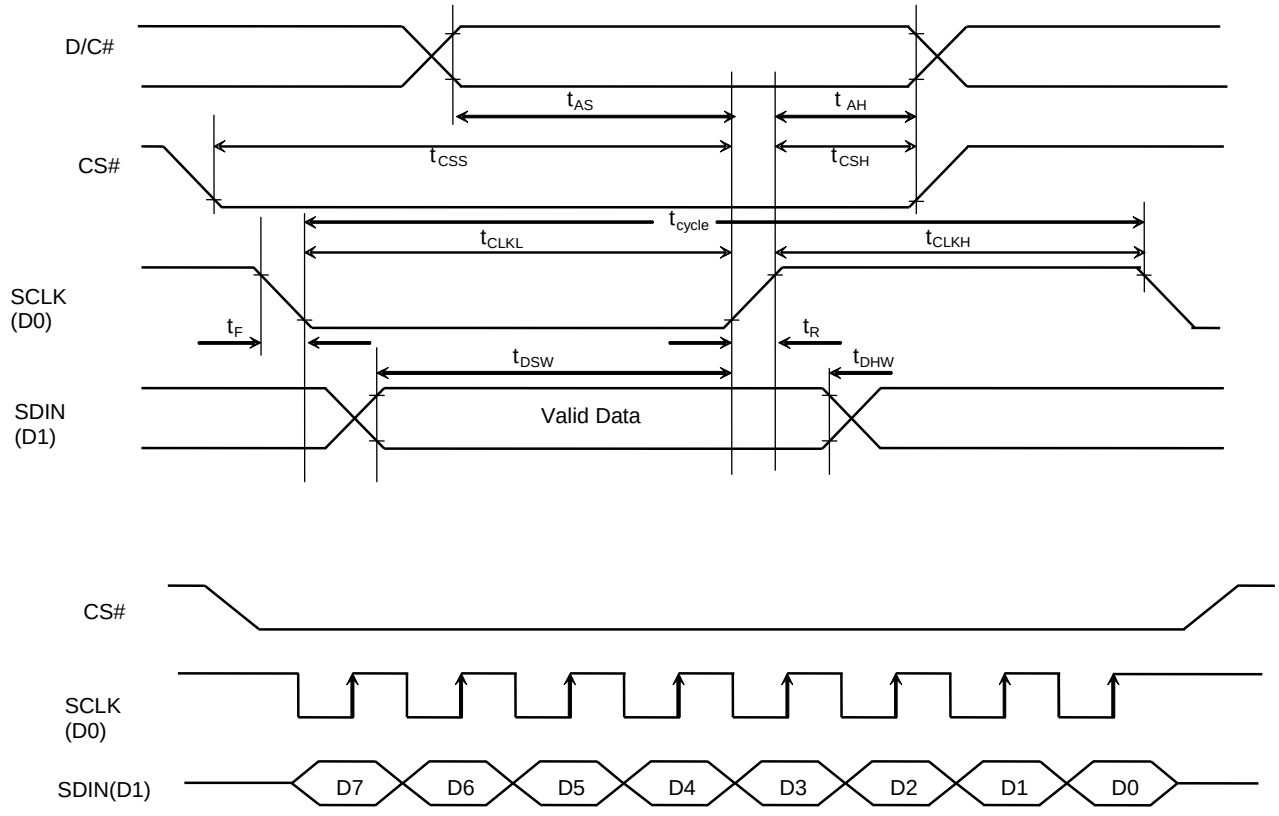
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	220	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	30	-	ns
t_{CLKL}	Clock Low Time	25	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{CI} -V_{SS} = 1.65V to 2.1V, T_A = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	160	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{CI} -V_{SS} = 2.1V to 3.5V, T_A = 25°C)

Figure 5-3 : Serial interface characteristics (4-wire SPI)

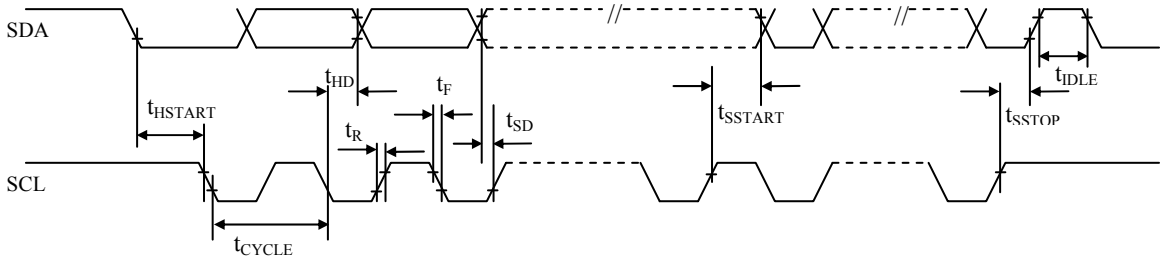


5.4.4 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	µs
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	ns
t_{SD}	Data Setup Time	10	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	µs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	µs
t_R	Rise Time	-	300	ns
t_F	Fall Time	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	µs

* (V_{CI} -V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Figure 5-4 : I²C interface Timing characteristics



6 Power ON/OFF Timing Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1327 (assume internal V_{DD} is used).

Power ON sequence:

1.Power ON V_{CI}.

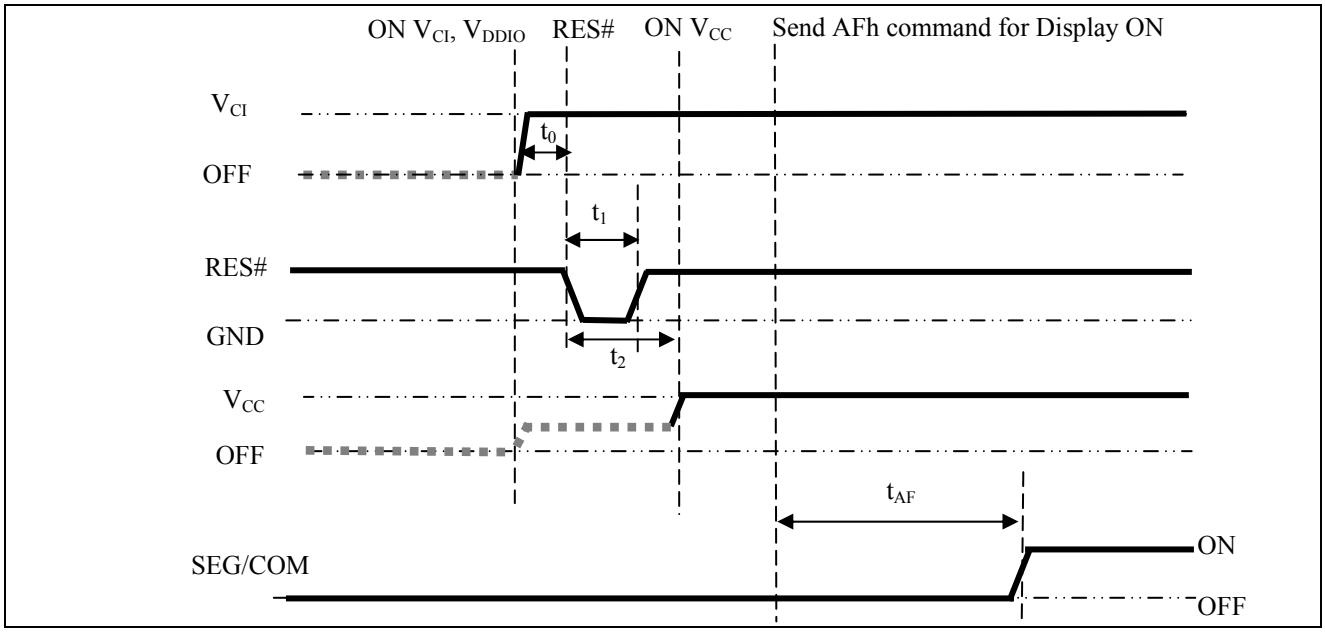
2.After V_{CI} becomes stable, set wait time at least 1ms (t0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) (4) and then HIGH (logic high).

3.After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.(1)

4.After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).

5. After V_{CI} become stable, wait for at least 300ms to send command.

Figure 6-1 : The Power ON sequence.



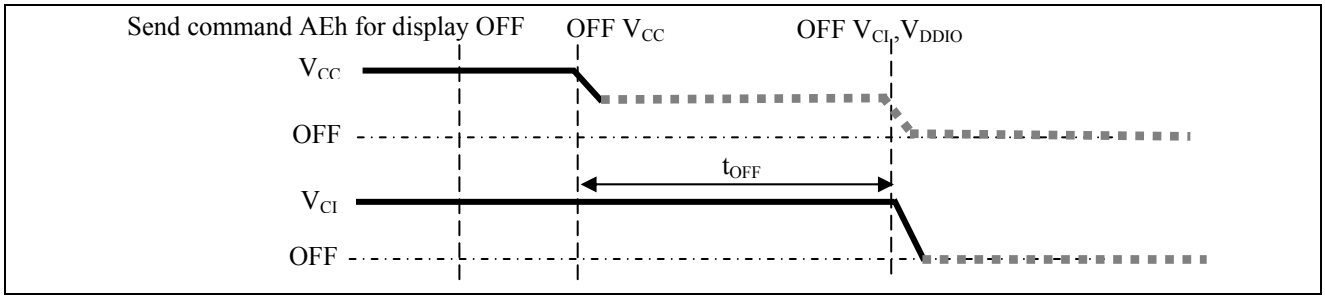
Power OFF sequence:

1. Send command AEh for display OFF.

2. Power OFF V_{CC}.(1), (2),(3)

3. Wait for t_{OFF}. Power OFF V_{CI}. (where Minimum t_{OFF}=0ms(5), Typical t_{OFF}=100ms)

Figure 6-2 : The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 6-1 and Figure 6-2.

(2) V_{CC} should be kept float (disable) when it is OFF.

(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) V_{CI} should not be Power OFF before V_{CC} Power OFF.

7 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	80°C 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40°C 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 240hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-40°C/80°C 100cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

8 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"