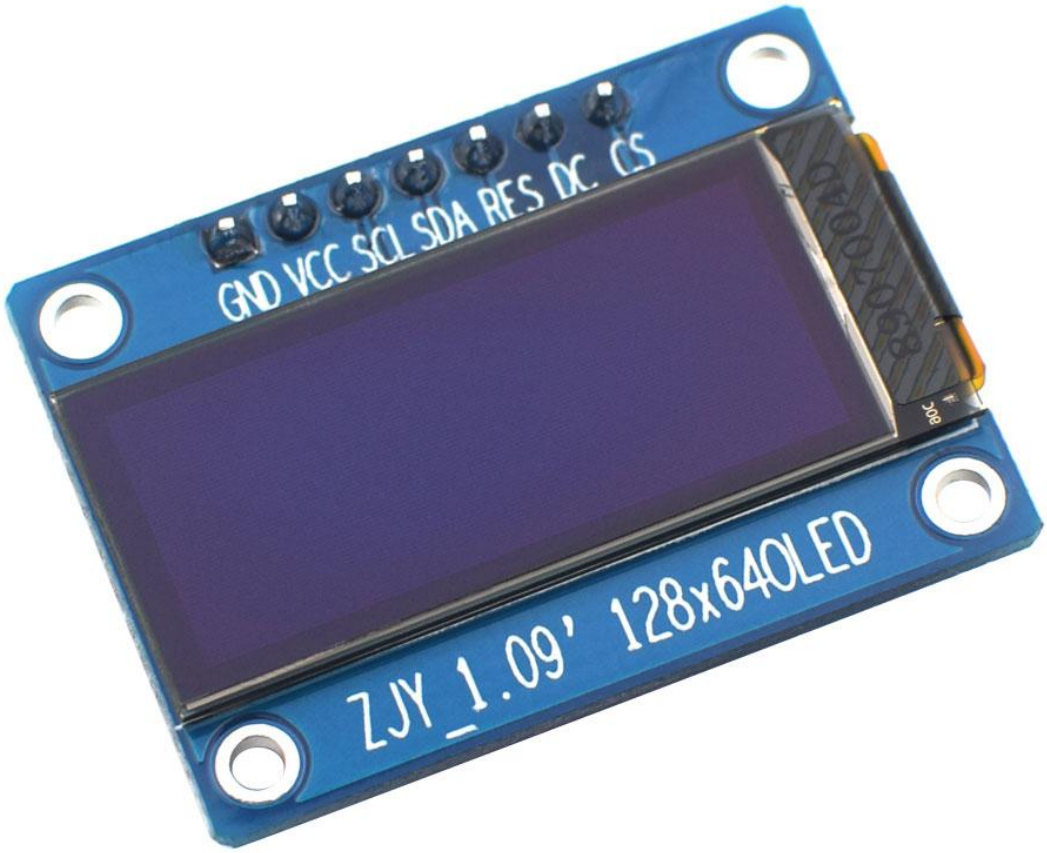
DisplayModule



DM-OLED11-662

1.09" 64 × 128 MONOCHROME GRAPHIC OLED DISPLAY MODULE - SPI

Contents

1 Revision History

Date	Changes
2020-02-26	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.09	inch
Display Mode	Passive Matrix OLED	-
Display Color	Monochrome (White)	Colors
Drive Duty	1/128 Duty	
Resolution	64 x 128	pixel
Controller IC	CH1115 (Compatible SSD1306)	-
Interface	4 wire SPI	-
Active Area	10.86 x 25.58	mm
Panel Dimension	14 x 31.96 x 1.22	mm
Module Dimension	24 x 33 x 2.42	mm
Pixel Pitch	0.17 x 0.20	mm
Pixel Size	0.15 x 0.18	mm
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

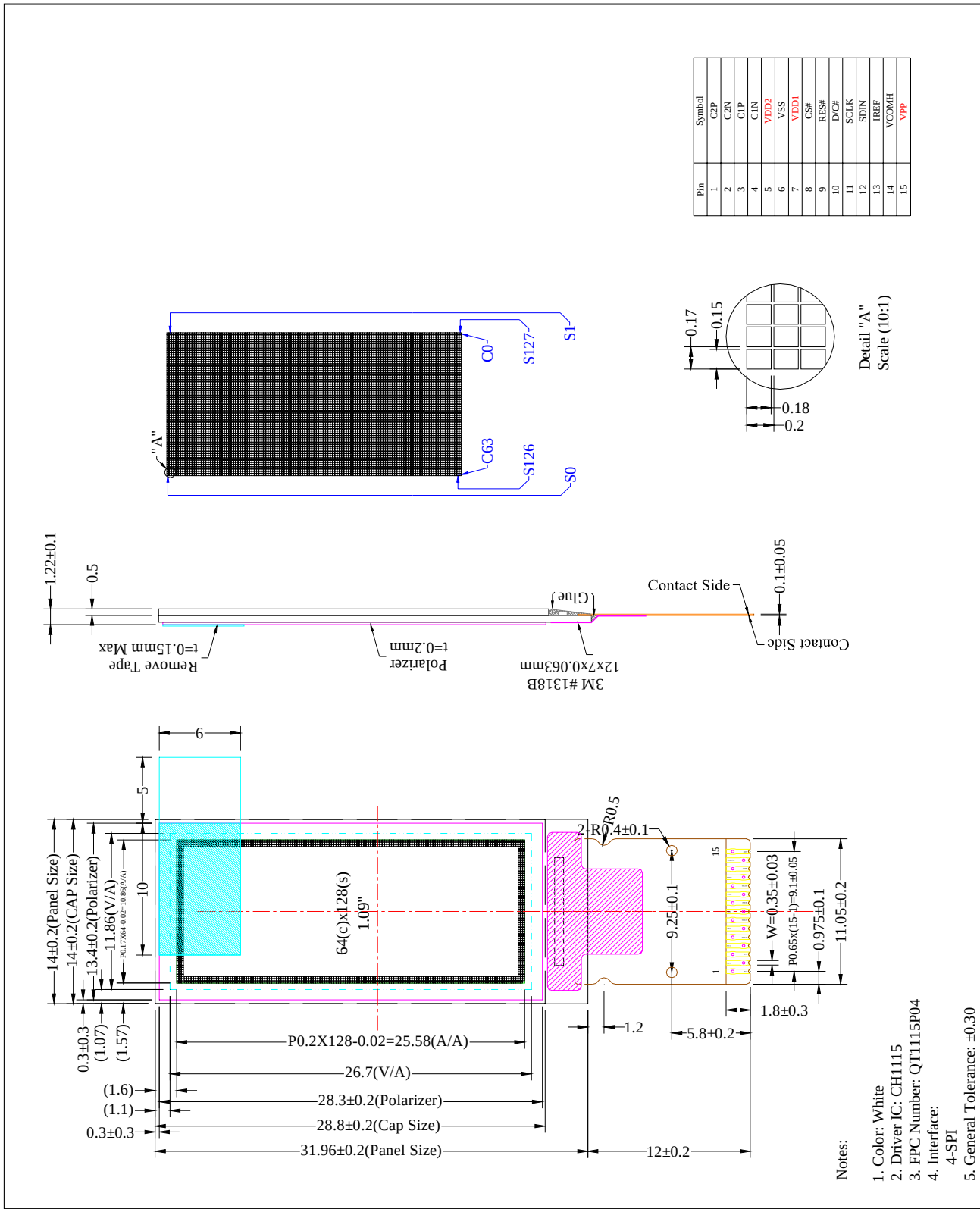
Pin No.	Symbol	Function Description
3 / 4 1 / 2	C1P / C1N C2P / C2N	**Positive Terminal of the Flying Inverting Capacitor** **Negative Terminal of the Flying Boost Capacitor** The charge-pump capacitors are required between the terminals.They must be floated when the converter is not used.
5	VDD12	**Power Supply for DC/DC Converter Circuit** This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used.It should be connected to Voplwhen the converter is not used.
6	VSS	**Ground of Logic Circuit** This is a ground pin.It acts as a reference for the logic pins.It must bel connected to external ground.
7	VDD1	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
8	CS#	**Chip Select** This pin is the chip select input.The chip is enabled for MCU communication only when CS# is pulled low.
9	RES#	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
10	D/C#	**Data/Command Control** This pin is Data/Command control pin. When the pin is pulled high, the input at D7~DO is treated as display data. When the pin is pulled low, the input at D7-Do will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I'C mode, this pin acts as SA0 for slavel aDD1ress selection. For detail relationship to MCU interface signals, please refer to the Timingl Characteristics Diagrams.
11	SCLK	**Serial Clock Input Singal** The transmission if information in the bus is following a clock signal.Each transmission of data bit is taken place during a single clock period of this pin.
12	SDIN	**Serial Clock Input Singal** The transmission if information in the bus is following a clock signal.Each transmission of data bit is taken place during a single clock period of this pin.
13	IRRF	**Current Reference for Brightness Adjustment** This pin is segment current reference pin.A resistor should be connected between this pin and Vss.Set the current at 12.5uA maximum.
14	VCOMH	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals.A capacitor should be connected between this pin and Vss.
15	VPP	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip.A stabilization capacitorl should be connected between this pin and Vss when the converter is used.It must be connected to external source when the converter is not used.

3.2 Module Pin Description

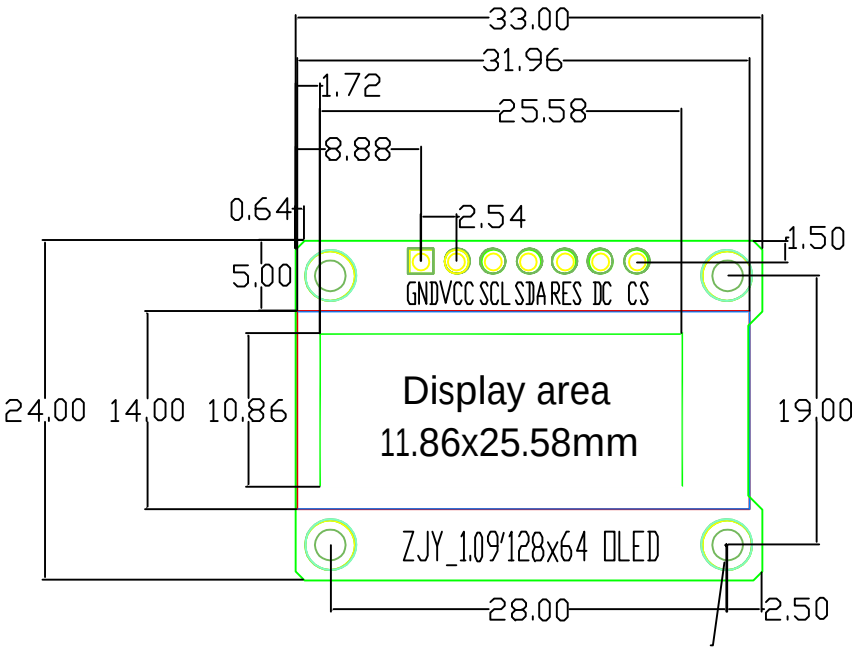
Pin No.	Symbol	Function Description
1	GND	Power Ground
2	VCC	3.3V~5.5V
3	SCL	The SPI clock line
4	SDA	SPI data line
5	RES	Display reset pin
6	DC	SPI data/command selection pin
7	CS	SPI Chip Select,The low level is effective, if do not want to use must be grounded

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



hole diameter 2mm,distance to edge of plate 2.5 mm

5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles		-	Free	-	°	-
C.I.E. (White)	(x) (y)	0.23 0.25	0.27 0.29	0.31 0.33	-	C.I.E.1931
Luminance (V_{PP} Supplied Externally)	L_{br}	100	-	-	cd/m²	-
Luminance (V_{PP} Generated by Internal DC/DC)	L_{br}	80	100	-	cd/m²	-
Dark room Contrast Ratio	CR	-	2000:1	-	-	-

Optical measurement taken at V_{DD1} = 2.8V, V_{PP} = 8.0V & 7.4V .

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Display Supply Voltage	V_{PP}	-0.3	14.5	V	Note1,2
Logic Supply Voltage	V_{DD1}	-0.3	3.6	V	Note1,2
DC/DC Supply Voltage	V_{DD12}	-0.3	4.8	V	Note1,2
Operating Temperature	TOP	-40	85	℃	-
Storage Temperature	TSTG	-40	85	℃	Note3
Life Time (90 cd/m^2)		10,000	-	hour	Note4
Life Time (70 cd/m^2)		30,000	-	hour	Note4
Life Time (50 cd/m^2)		50,000	-	hour	Note4

Note (1): All of the voltages are on the basis of"V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may oPPur. Also, for normal operations, it is desirable to use this module under the conditions aPPording to Section 5. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can oPPur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{PP} = 7.5V, T a = 25°C, 50% Checkerboard.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the aPPelerated operation at high temperature conditions.

5.3 DC Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Remark
Logic Supply Voltage	V_{DD1}	1.65	2.8	3.5	V	-
Display Supply Voltage (Supplied Externally)	V_{PP}	7.0	7.5	8.0	V	Note 1; (Internal DC/DC Disable)
DC/DC Supply Voltage	V_{DD12}	3.5	-	4.75	V	Internal DC/DC Enable
Display Supply Voltage (Generated by Internal DC/DC)	V_{PP}	-	7.4	-	V	Note 1; (Internal DC/DC Disable)
Low Level Input Voltage	V_{IL}	0	-	0.2 x V_{DD1}	V	I_{OUT}=100µA, 3.3MHz
High Level Input Voltage	V_{IH}	0.8 x V_{DD1}	-	V_{DD1}	V	I_{OUT}=100µA, 3.3MHz
Low Level Output Voltage	V_{OL}	0	-	0.1 x V_{DD1}	V	I_{OUT}=100µA, 3.3MHz
High Level Output Voltage	V_{OH}	0.9 x V_{DD1}	-	V_{DD}	V	I_{OUT}=100µA, 3.3MHz
V_{DD1} Operating Current	I_{DD1}	-	160	220	µA	-
V_{PP} Operating Current (V_{PP} Supplied Externally)	I_{PP}	-	-	-	mA	Note 2
V_{DD2} Operating Current (V_{PP} Generated by Internal DC/DC)	I_{DD2}	-	23.0	28.0	mA	Note 3
V_{PP} Sleep Mode Current	$I_{PP, SLEEP}$	-	2	5	µA	-
V_{DD} Sleep Mode Current	$I_{DD1, SLEEP}$	-	1	5	µA	-

Note 1: Brightness (L_{br}) and Supply Voltage for Display (V_{PP}) are subject to the change of the panel characteristics and the customer's request.

Note 2: V_{DD1} = 2.8V, V PP = 7.5V, 100% Display Area Turn on.

Note 3: V_{DD1} = 2.8V, V PP = 7.4V, 100% Display Area Turn on.

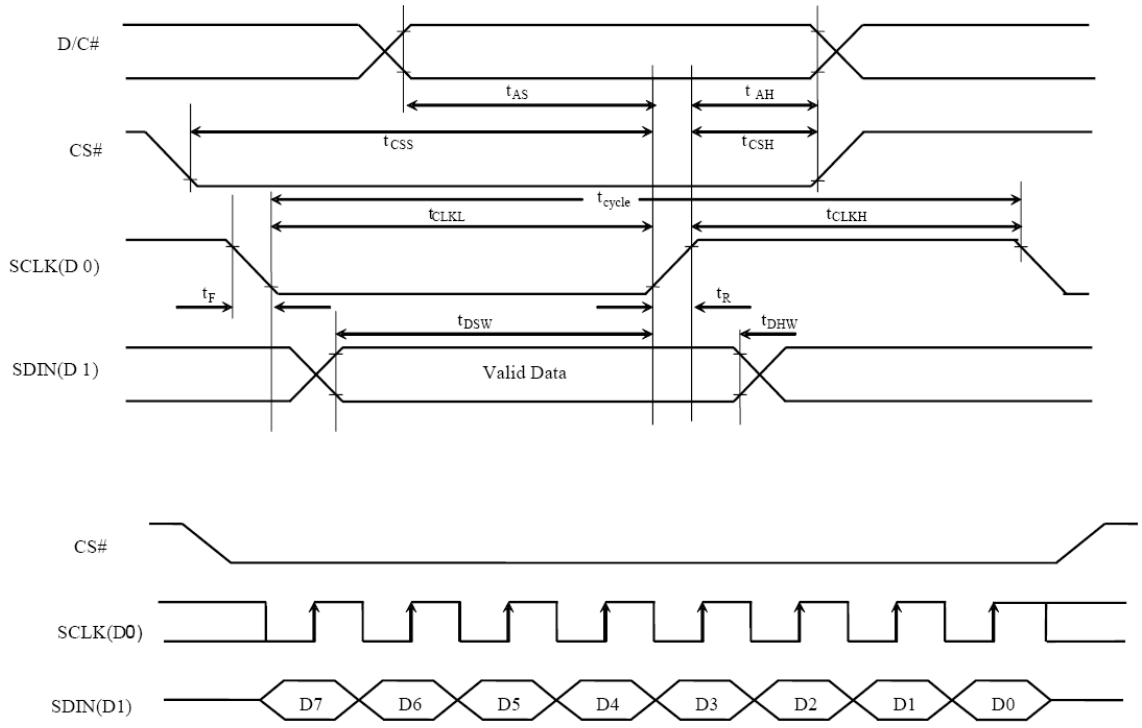
5.4 AC Characteristics

5.4.1 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD1} -V_{SS} = 1.65V to 3.3V, Ta = 25°C)

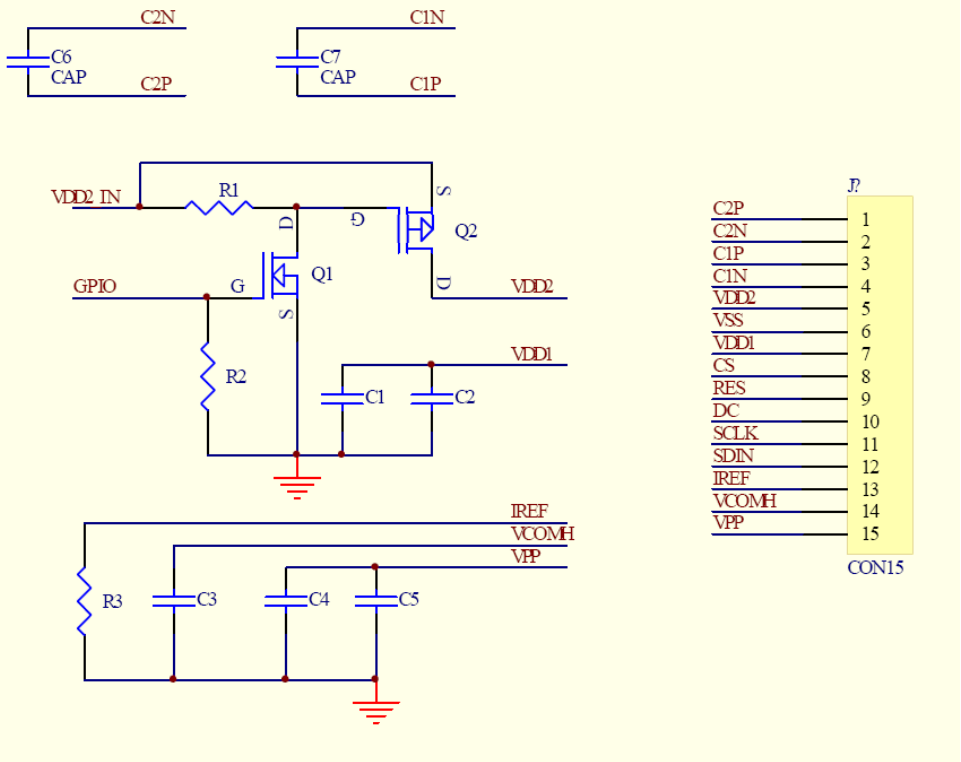
Serial interface characteristics



5.5 Application circuit reference

5.5.1 4-wire Serial Interface with Internal Charge Pump

Special Tips: When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current.



Recommended Components:

C6, C7:	1μF / 16V, X5R
C3:	2.2μF/16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
C1:	0.1μF /6.3V
C2:	4.7μF / 6.3V
R3:	620kΩ, R3 = (Voltage at IREF - VSS) / IREF
R1, R2:	47kΩ
Q1:	FDN338P
Q2:	FDN335N

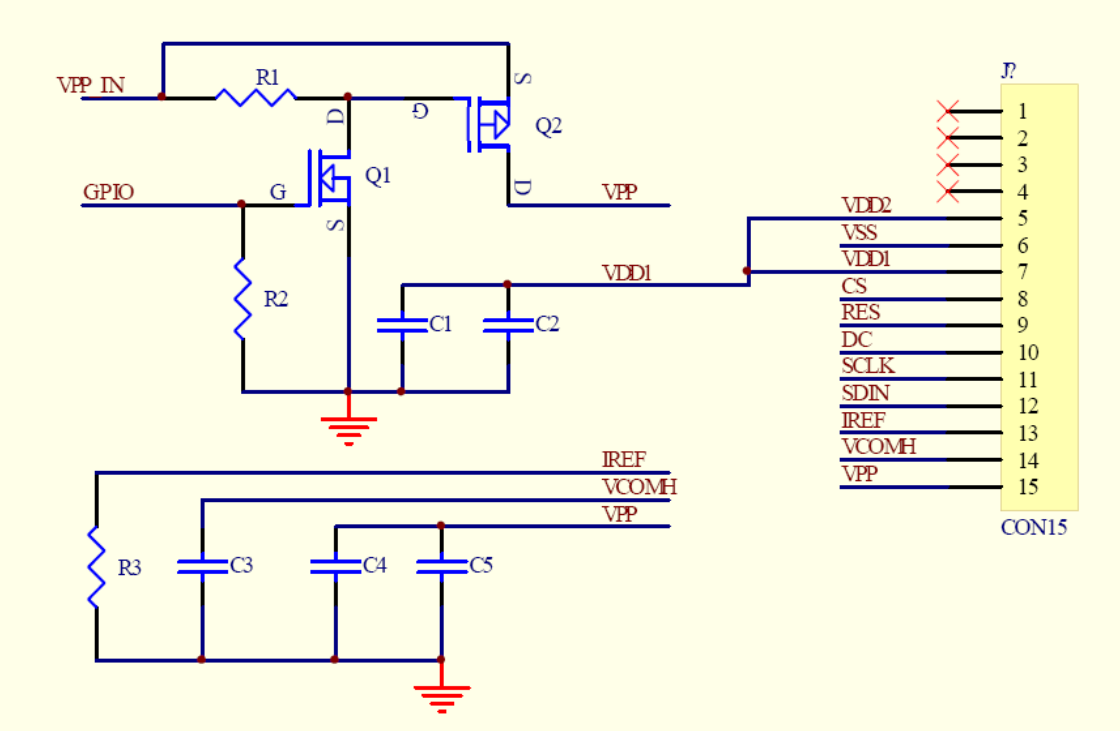
Notes:

VDD1:1.65~3.3V, it should be equal to MPU I/O voltage.

VDD2_in: 3.5~4.75V

5.5.2 4-wire Serial Interface with external VPP

Special Tips: When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current.



Recommended Components:

C3: 2.2μF/16V, X7R

C4: 4.7μF / 16V, X7R

C5: 0.1μF / 16V, X7R

C1: 0.1μF /6.3V

C2: 4.7μF / 6.3V

R3: 620kΩ, R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

VDD1: 1.65~3.3V, it should be equal to MPU I/O voltage.

VPP: 7.0~8.0V

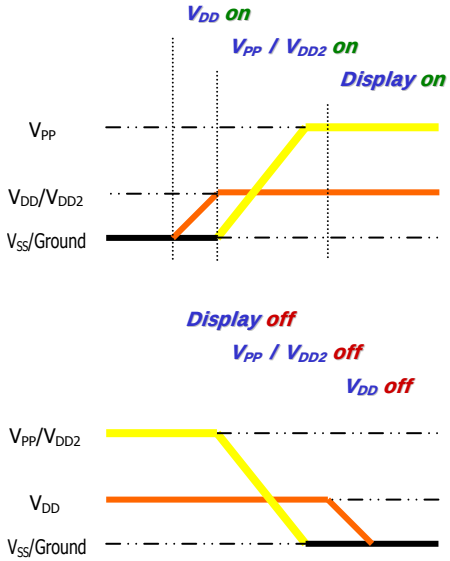
6 Functional Specification

6.1 Commands

Refer to the Technical Manual for the CH1115.

6.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.



6.2.1 Power up Sequence:

1. Power up V_{DD1}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{PP} / V_{DD2}
6. Delay 100ms (When V_{PP} is stable)
7. Send Display on command

6.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{PP} / V_{DD2}
3. Delay 100ms
4. (When V_{PP} / V_{DD2} is reach 0 and panel is completely discharges)
5. Power down V_{DD1}

Note :

1) Since an ESD protection circuit is connected between V_{DD1} and V_{PP} inside the driver IC, V_{PP} becomes lower than V_{DD} whenever V_{DD1} is ON and V_{PP} is OFF.
2) V_{PP} / V_{DD2} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD1}, V_{PP}, V_{DD2}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{PP} / V_{DD2} power down.

6.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

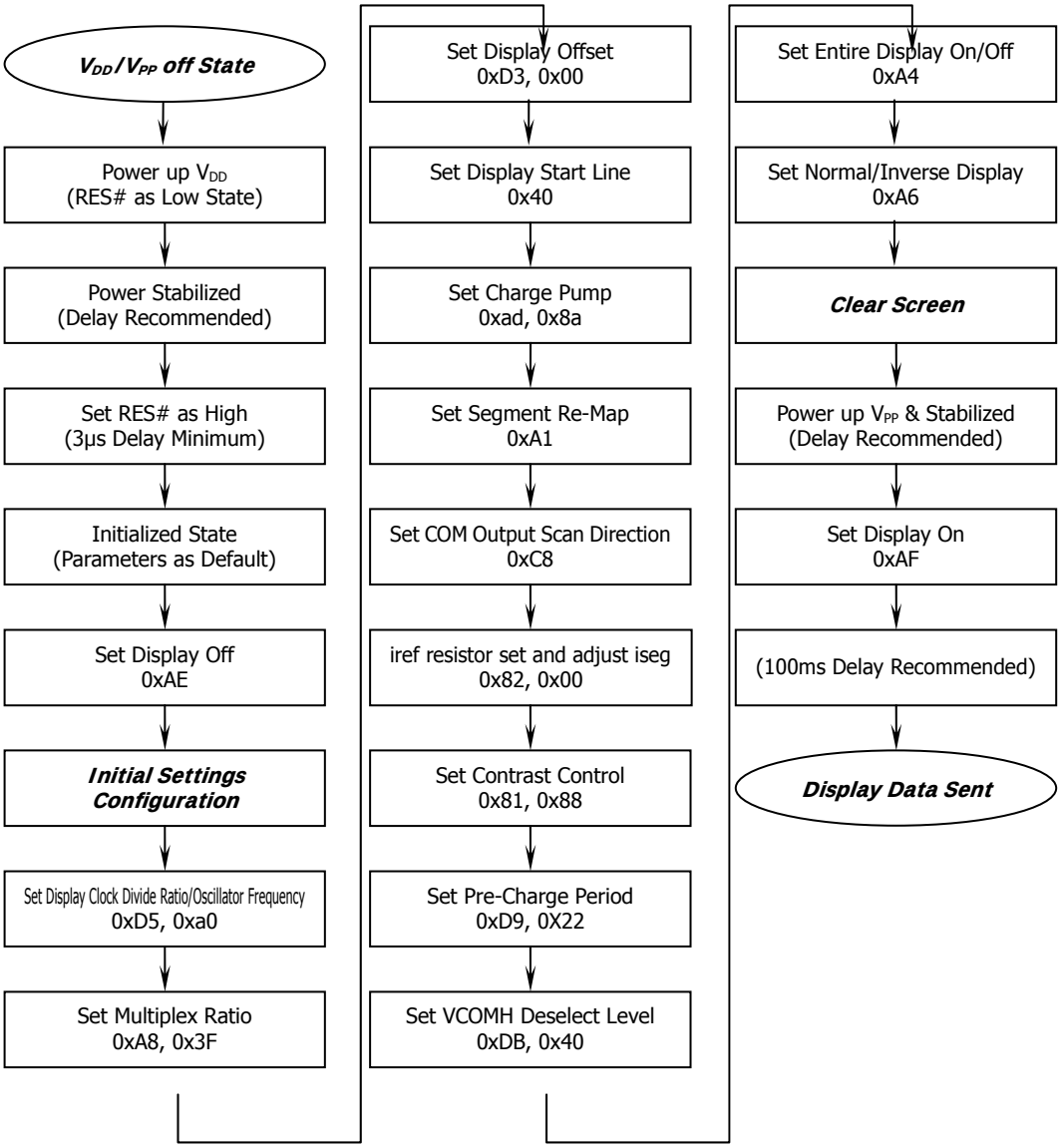
1. Display is OFF. 1.Common and Segment are in high impedance state.
2. 128 x 64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column aDD1ress 00h and COM0 mapped to row aDD1ress 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM aDD1ress 0
6. Column aDD1ress counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

6.4 Actual Application Example

Command usage and explanation of an actual example

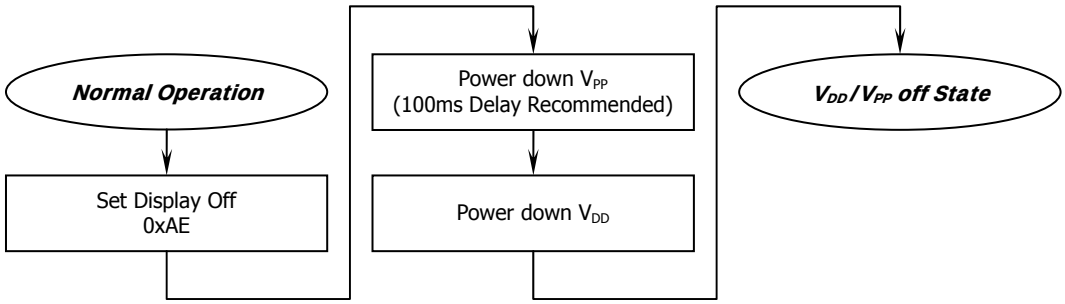
6.4.1 V_{PP} Supplied Externally

Power up Sequence

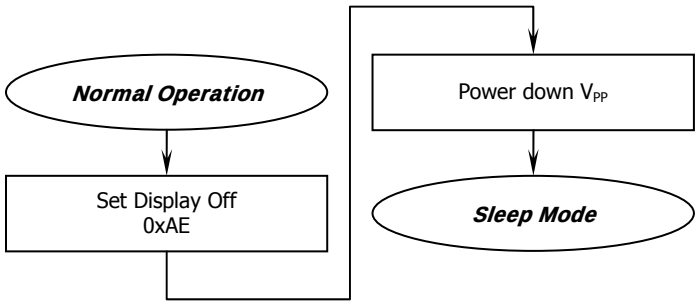


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

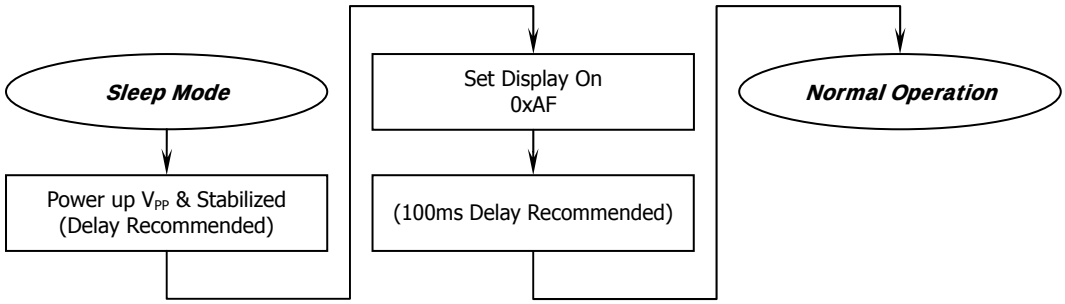
Power down Sequence



Entering Sleep Mode



Exiting Sleep Mode



External setting

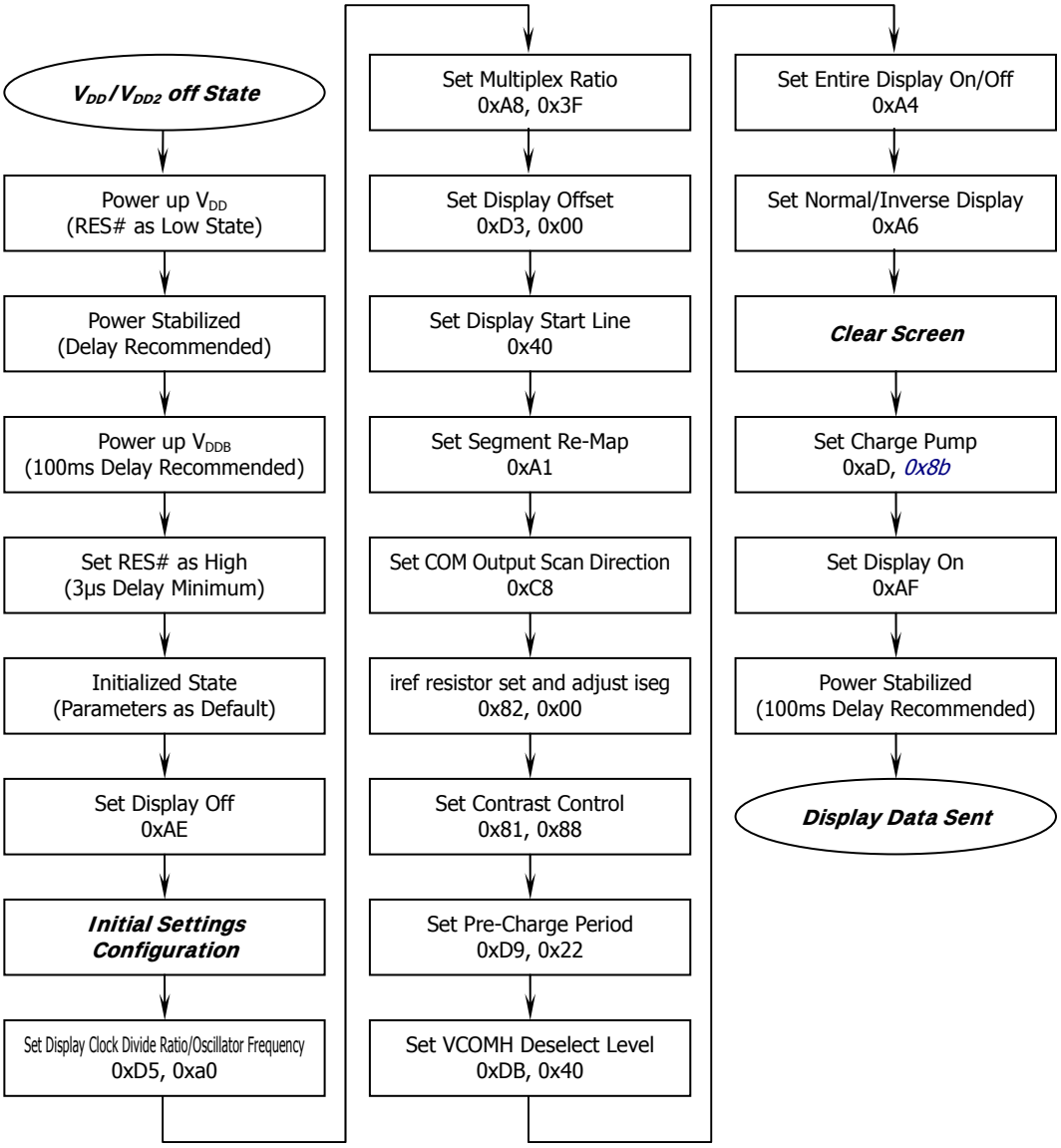
```
{
        RES=1;
        delay(1000);
        RES=0;
        delay(1000);
        RES=1;
        delay(1000);

        write_i(0xAE);   /*display off*/
        write_i(0x00);   /*set lower column address*/
        write_i(0x10);   /*set higher column address*/
        write_i(0xB0);   /*set page address*/
```

```
        write_i(0x40);    /*set display start lines*/
        write_i(0x81);    /*contract control*/
        write_i(0x88);    /*4d*/
        write_i(0x82);    /* iref resistor set and adjust ISEG*/
        write_i(0x00);
        write_i(0xA1);    /*set segment remap       0xA0*/
        write_i(0xA2);    /*set seg pads hardware configuration*/
        write_i(0xA4);    /*Disable Entire Display On (0xA4/0xA5)*/
        write_i(0xA6);    /*normal / reverse*/
        write_i(0xA8);    /*multiplex ratio*/
        write_i(0x3F);    /*duty = 1/64*/
        write_i(0xC8);    /*Com scan direction      0XC0*/
        write_i(0xD3);    /*set display offset*/
        write_i(0x00);    /*          */
        write_i(0xD5);    /*set osc division*/
        write_i(0xa0);
        write_i(0xD9);    /*set pre-charge period*/
        write_i(0x22);
        write_i(0xdb);    /*set vcomh*/
        write_i(0x40);
        write_i(0x31);    /* Set pump 7.4v */
        write_i(0xad);    /*set charge pump enable*/
        write_i(0x8a);    /*Set DC-DC enable (0x8a=disable; 0x8b=enable) */
        write_i(0xAF);    /*display ON*/
}

void write_i(unsigned char ins)
{
        unsigned char m,da;
        unsigned int j;
        DC=0;
        CS=0;
        da=ins;
        for(j=0;j<8;j++)
        {
                m=da;
                SCL=0;
                m=m&0x80;
                if(m==0x80)
                {
                        SDA=1;
                }
                else
                {
                        SDA=0;
                }
                da=da<<1;
                SCL=1;
        }
        CS=1;
```

```
}

void write_d(unsigned char dat)
        {
        unsigned char m,da;
        unsigned int j;
        DC=1;
        CS=0;
        da=dat;
        for(j=0;j<8;j++)
        {
                m=da;
                SCL=0;
                m=m&0x80;
                if(m==0x80)
                {
                        SDA=1;
                }
        else
                {
                        SDA=0;
                }
                da=da<<1;
                SCL=1;
        }
        CS=1;
}

void delay(unsigned int i)
{
        while(i>0)
        {
                i--;
        }
}
```

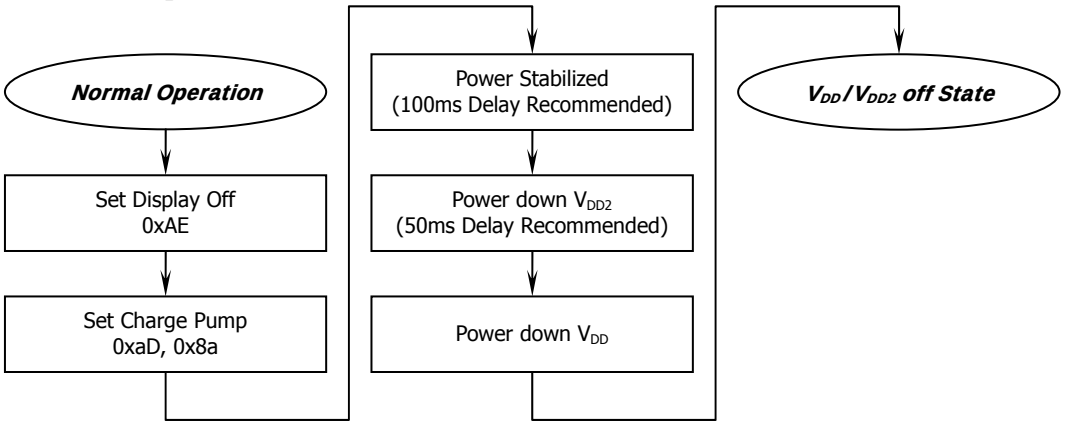
6.4.2 V_{PP} Generated by Internal DC/DC Circuit

Power up Sequence

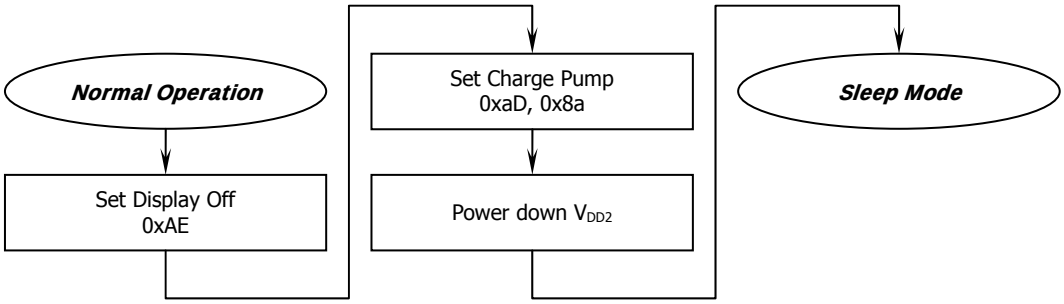


If the noise is aPPidentally oPPurred at the displaying window during the operation, please reset the display in order to recover the display function.

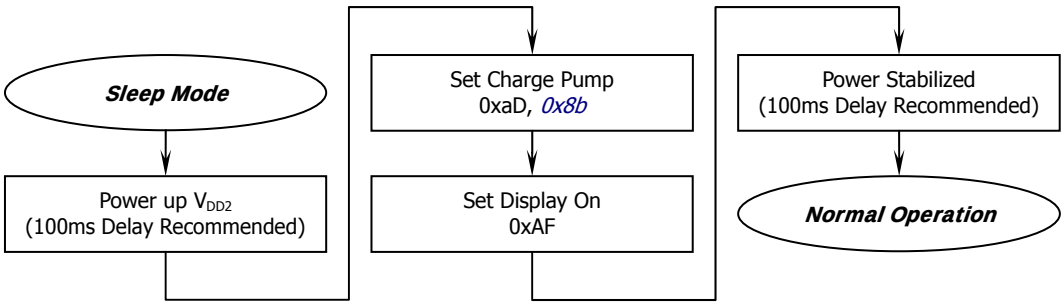
Power down Sequence



Entering Sleep Mode



Exiting Sleep Mode



Internal setting（Charge pump）

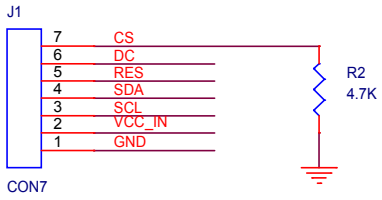
```
{
        RES=1;
        delay(1000);
        RES=0;
        delay(1000);
        RES=1;
        delay(1000);

        write_i(0xAE);   /*display off*/
        write_i(0x00);   /*set lower column address*/
        write_i(0x10);   /*set higher column address*/
        write_i(0xB0);   /*set page address*/
```

```
        write_i(0x40);    /*set display start lines*/
        write_i(0x81);    /*contract control*/
        write_i(0x88);    /*4d*/
        write_i(0x82);    /* iref resistor set and adjust ISEG*/
        write_i(0x00);
        write_i(0xA1);    /*set segment remap       0xA0*/
        write_i(0xA2);    /*set seg pads hardware configuration*/
        write_i(0xA4);    /*Disable Entire Display On (0xA4/0xA5)*/
        write_i(0xA6);    /*normal / reverse*/
        write_i(0xA8);    /*multiplex ratio*/
        write_i(0x3F);    /*duty = 1/64*/
        write_i(0xC8);    /*Com scan direction      0XC0*/
        write_i(0xD3);    /*set display offset*/
        write_i(0x00);    /*          */
        write_i(0xD5);    /*set osc division*/
        write_i(0xa0);
        write_i(0xD9);    /*set pre-charge period*/
        write_i(0x22);
        write_i(0xdb);    /*set vcomh*/
        write_i(0x40);
        write_i(0x31);    /* Set pump 7.4v */
        write_i(0xad);    /*set charge pump enable*/
        write_i(0x8a);    /*Set DC-DC enable (0x8a=disable; 0x8b=enable) */
        write_i(0xAF);    /*display ON*/
}
void write_i(unsigned char ins)
{
        unsigned char m,da;
        unsigned int j;
        DC=0;
        CS=0;
        da=ins;
        for(j=0;j<8;j++)
        {
                m=da;
                SCL=0;
                m=m&0x80;
                if(m==0x80)
                {
                        SDA=1;
                }
                else
                {
                        SDA=0;
                }
                da=da<<1;
                SCL=1;
        }
        CS=1;
}
```

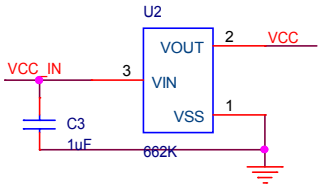
```
void write_d(unsigned char dat)
	{
	unsigned char m,da;
	unsigned int j;
	DC=1;
	CS=0;
	da=dat;
	for(j=0;j<8;j++)
	{
		m=da;
		SCL=0;
		m=m&0x80;
		if(m==0x80)
		{
			SDA=1;
		}
	else
		{
			SDA=0;
		}
		da=da<<1;
		SCL=1;
	}
	CS=1;
}

void delay(unsigned int i)
{
	while(i>0)
	{
		i--;
	}
}
```

7 Module Schematic

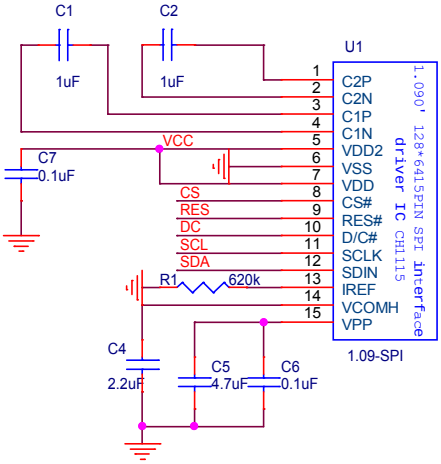
Drive IC:CH1115 compatible with SSD1306



OLED external interface circuit; The communication interface is SPI



3.3V voltage stabilizing circuit.
If 3.3V power supply is used,the regulator tube can beremoved; Directly connect to 3.3V power.

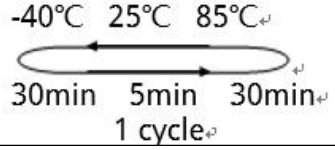


OLED bare screen peripheral circuit
Special attention; Since this screen driver chip supports internal boost, we can directly supply a power supply can be; No need for external high voltage power supply.
When using internal boost, the 15-pin VPP does not need to be connected to the power supply. Connect the capacitor directly to the ground; When you want to use external power supply, please note that the VPP needs a power supply of around 7.5V instead of 3.3V.

Interface Definition:

1>GND: Ground
2>VCC: Power Supply 3.3V～5V
3>SCL: OLED SPI clock line
4>SDA: OLED SPI data line
5>RES: After the OLED is energized, the low level is reset once, and then the high level is maintained all the time
6>DC : Data/command control line
7>CS : OLED SPI Chip Select;The low level is effective.

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85℃ 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40℃ 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 ℃ 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 120hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40℃/85℃ 24 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"