DisplayModule

DM-OLED104-664

1.04” 128 X 32 MONOCHROME GRAPHIC OLED DISPLAY MODULE - SPI,I2C

Contents

1 Revision History

Date	Changes
2020-11-26	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	1.04’	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome	Colors
Resolution	128 x 32	pixel
Controller IC	SSD1306	-
Duty	1/32	duty
Interface	8-bit 68XX/80XX Parallel,3-/4-wire SPI,I2C	-
Active Area	25.58 x 6.38	mm
Module Dimension	29.8 x 26.5 x 1.30	mm
Weight	TBD	g

3 Pin Description

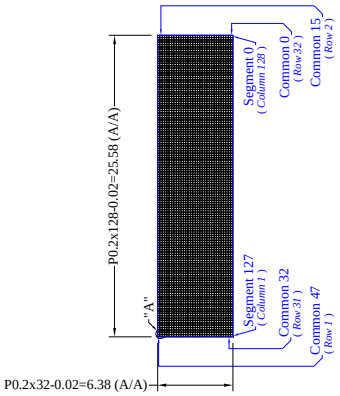
3.1 Panel Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1,30</td><td>N.C.(GND)</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins.
These pins must be connected to external ground as the ESD protection circuit.</td></tr>
<tr><td>2/3
4/5</td><td>C2P/C2N
C1P/C1N</td><td>Negative Terminal of the Flying Boost Capacitor
Positive Terminal of the Flying Inverting Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>6</td><td>VDDB</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter.
It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.</td></tr>
<tr><td>7</td><td>NC</td><td>Reserved Pin
The N.C. pin between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>9</td><td>VDD</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>10
11
12</td><td>BS0
BS1
BS2</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th><th>BS2</th></tr>
<tr><td>I2C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68xx parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80xx parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>13</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>14</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>15</td><td>D/C#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at</td></tr>
</table>

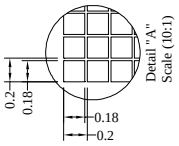
		SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
16	R/W#	**Read/Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
17	E/RD#	**Read/Write Enable or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
18-25	D0~D7	**Host Data Input/ Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
26	IREF	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5μA maximum.
27	VCOMH	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
28	VCC	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
29	VLSS	**Ground of Analog Circuit** This is an analog ground pin, It should be connected to Vss externally.

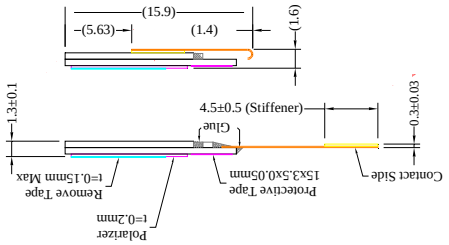
4 Mechanical Drawing

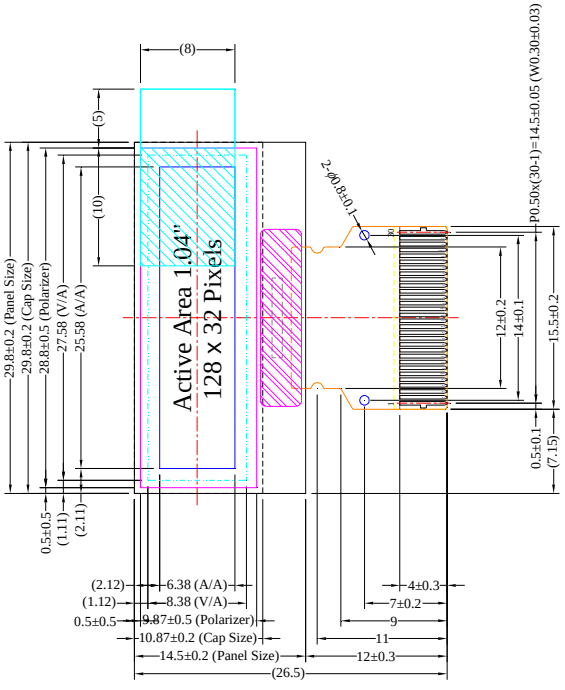
4.1 Panel Mechanical Drawing



Pin	Symbol
1	N.C. (GND)
2	C2P
3	C2N
4	C1P
5	C1N
6	VBAT
7	N.C.
8	VSS
9	VDD
10	BS0
11	BS1
12	BS2
13	CS#
14	RES#
15	D/C#
16	R/W#
17	E/RD#
18	D0
19	D1
20	D2
21	D3
22	D4
23	D5
24	D6
25	D7
26	IREF
27	VCOMH
28	VCC
29	VLSS
30	N.C. (GND)







Notes:

1. Color: White
2. Driver IC: SSD1306
3. FPC Number: UT-0206-P15
4. Interface:
   8-bit 68XX/80XX Parallel, 3-/4-wire SPI, I2C
5. General Tolerance: ±0.30
6. The total thickness (1.40 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 1.65 Max.

5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage for Logic	VDD		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	VCC	Internal DC/DC Disable	7.0	7.5	8.0	V
Supply Voltage for DC/DC	VDDB	Internal DC/DC Enable	3.0	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	VCC	Internal DC/DC Enable	7.0	7.5	8.0	V
Operating Current	IDD		-	180	300	uA
Low Level Input Voltage	V_{IL}		0	-	$0.2xV_{DD}$	V
High Level Input Voltage	V_{IH}		$0.8xV_{DD}$	-	V_{DD}	V
Low Level Output Voltage	V_{OL}		0		$0.1xV_{DD}$	V
High Level Output Voltage	V_{OH}		$0.9xV_{DD}$		V_{DD}	V
Operating Temperature	TOP	Absolute Max	-40		70	℃
Storage Temperature	TST	Absolute Max	-40		80	℃

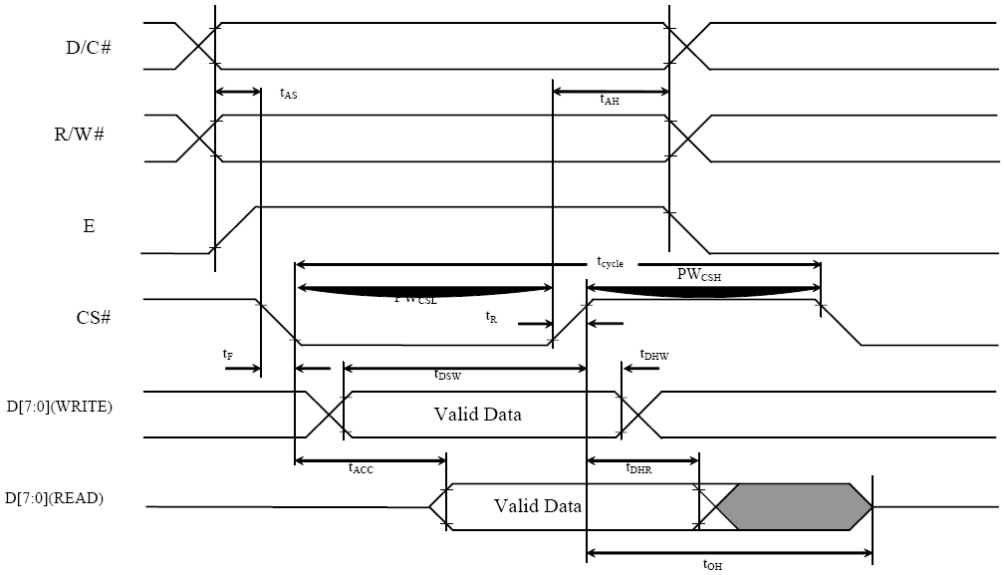
6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles		-	Free	-	degree
Brightness (Vcc generated by internal DC/DC)	L_{br}	80	100	-	cd/m²
C.I.E (White)	(x) (y)	0.25 0.27	0.29 0.31	0.33 0.35	
Contrast Ratio	CR	-	>10000:1	-	
Lifetime		10,000			Hrs

7 Timing Characteristics

7.1 68XX-Series MPU Parallel Interface Timing Characteristics:

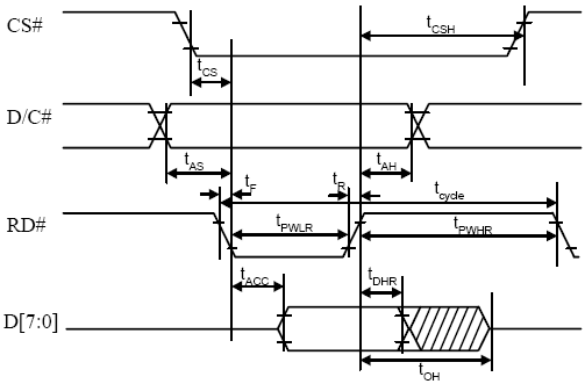
Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0			ns
t_{DSW}	Write Data Setup Time	40			ns
t_{DHW}	Write Data Hold Time	7			ns
t_{DHR}	Read Data Hold Time	20			ns
t_{OH}	Output Disable Time	-		70	ns
t_{ACC}	Access Time	-		140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	-	ns
	Chip Selected Low Pulse width (Write)	60	-	-	ns
PW_{CSH}	Chip Selected High Pulse Width (Read)	60	-	-	ns
	Chip Selected High Pulse Width (Write)				
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



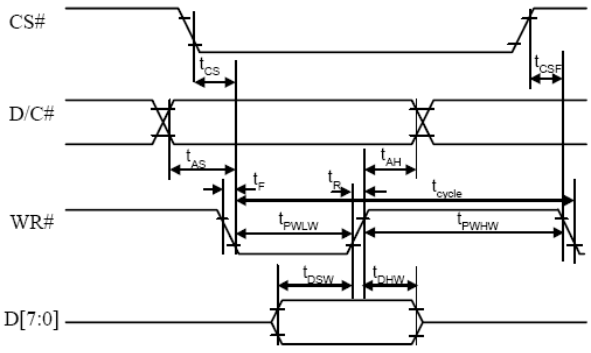
7.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0			ns
t_{DSW}	Write Data Setup Time	40			ns
t_{DHW}	Write Data Hold Time	7			ns
t_{DHR}	Read Data Hold Time	20			ns
t_{OH}	Output Disable Time	-		70	ns
t_{ACC}	Access Time	-		140	ns
t_{pwlr}	Read Low Time	120			ns
t_{pwlw}	Write Low Time	60			ns
t_{pwhr}	Read High Time	60			ns
t_{pwhw}	Write High Time	60			ns
t_{CS}	Chip Setup Time	0			ns
t_{CSL}	Chip Select Hold Time to Read Signal	0			ns
t_{CSH}	Chip Selecte Hold Time	20			ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

*(VDD-VSS=1.65V to 3.3V,Ta = 25° C)



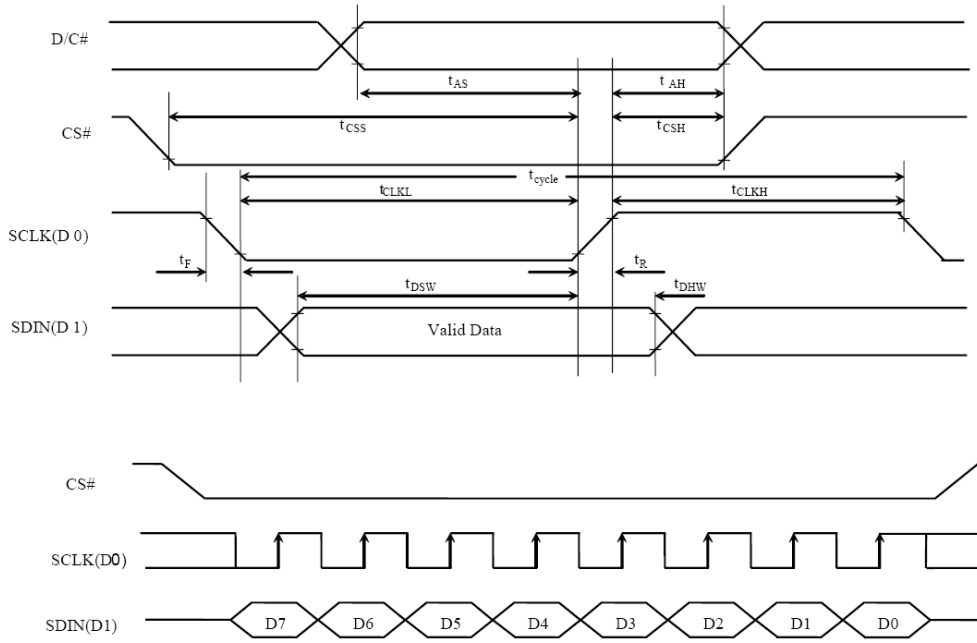
(***Read Timing***)



(***Write Timing***)

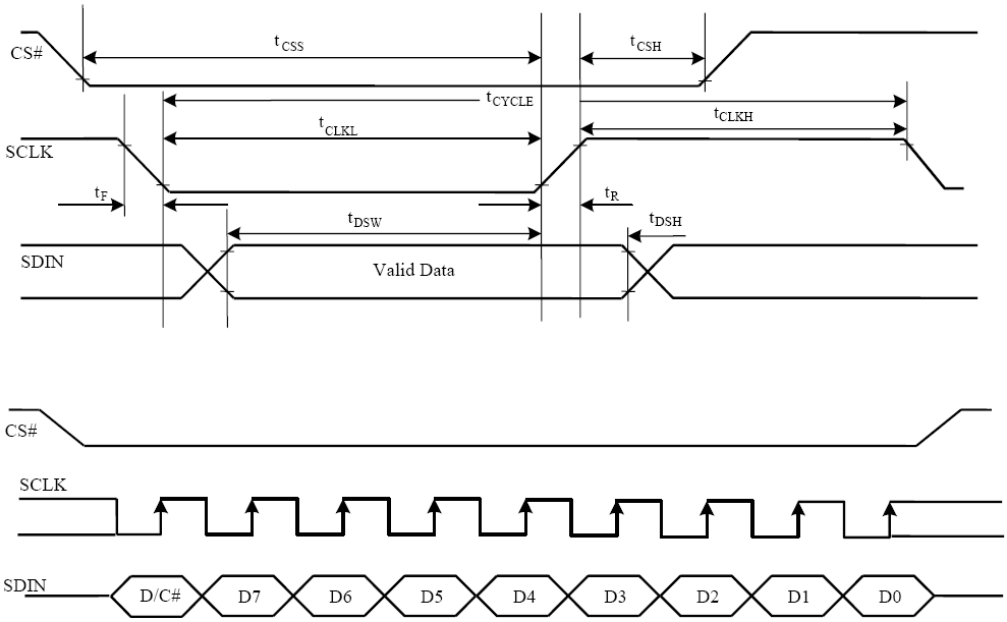
7.3 Serial Interface Timing Characteristics:(4-wire SPI)

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15			ns
t_{DSW}	Write Data Setup Time	15			ns
t_{DHW}	Write Data Hold Time	15			ns
t_{CSS}	Chip Select Setup Time	20			ns
t_{CSH}	Chip Select Hold Time	10			ns
t_{CLKL}	Clock Low Time	20			ns
t_{CLKH}	Clock High Time	20			ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



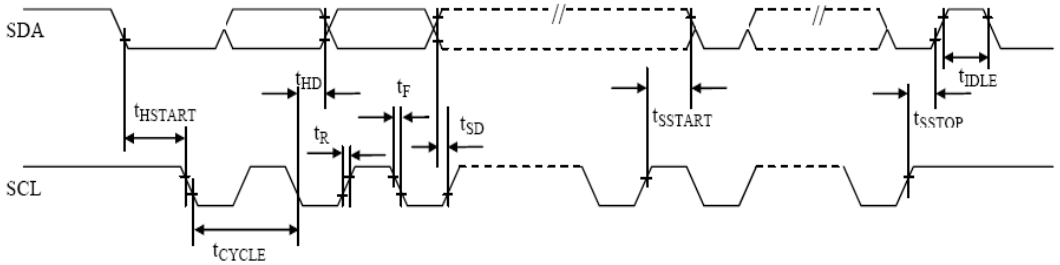
7.4 Serial Interface Timing Characteristics:(3-wire SPI)

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{DSW}	Write Data Setup Time	15			ns
t_{DHW}	Write Data Hold Time	15			ns
t_{CSS}	Chip Select Setup Time	20			ns
t_{CSH}	Chip Select Hold Time	10			ns
t_{CLKL}	Clock Low Time	20			ns
t_{CLKH}	Clock High Time	20			ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



7.5 I2C Interface Timing Characteristics:

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start Condition Hold Time	0.6		-	us
t_{HD}	Data Hold Time(for"SDA_{OUT}"Pin)	0		-	ns
	Data Hold Time(for"SDA_{IN}"Pin)	300			
t_{SD}	Data Setup Time	100		-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6		-	us
t_{SSTOP}	Stop Condition Setup Time	0.6			us
t_R	Rise Time for Data and Clock Pin	-	-	300	ns
t_F	Fall Time for Data and Clock Pin	-	-	300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3			us



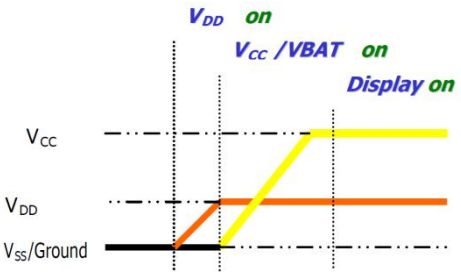
8 Functional Specification

8.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

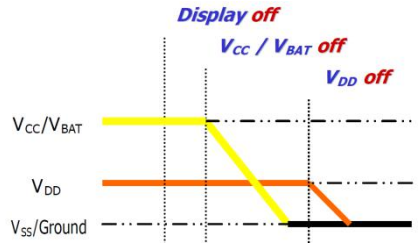
Power up Sequence

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/V_{bat}
6. Delay 100ms(When V_{CC} is stable)
7. Send Display on command



Power down Sequence

1. Send Display off command
2. Power down V_{CC}/V_{BAT}
3. Delay 100ms
   (When V_{CC}/V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



8.2 Reset Circuit

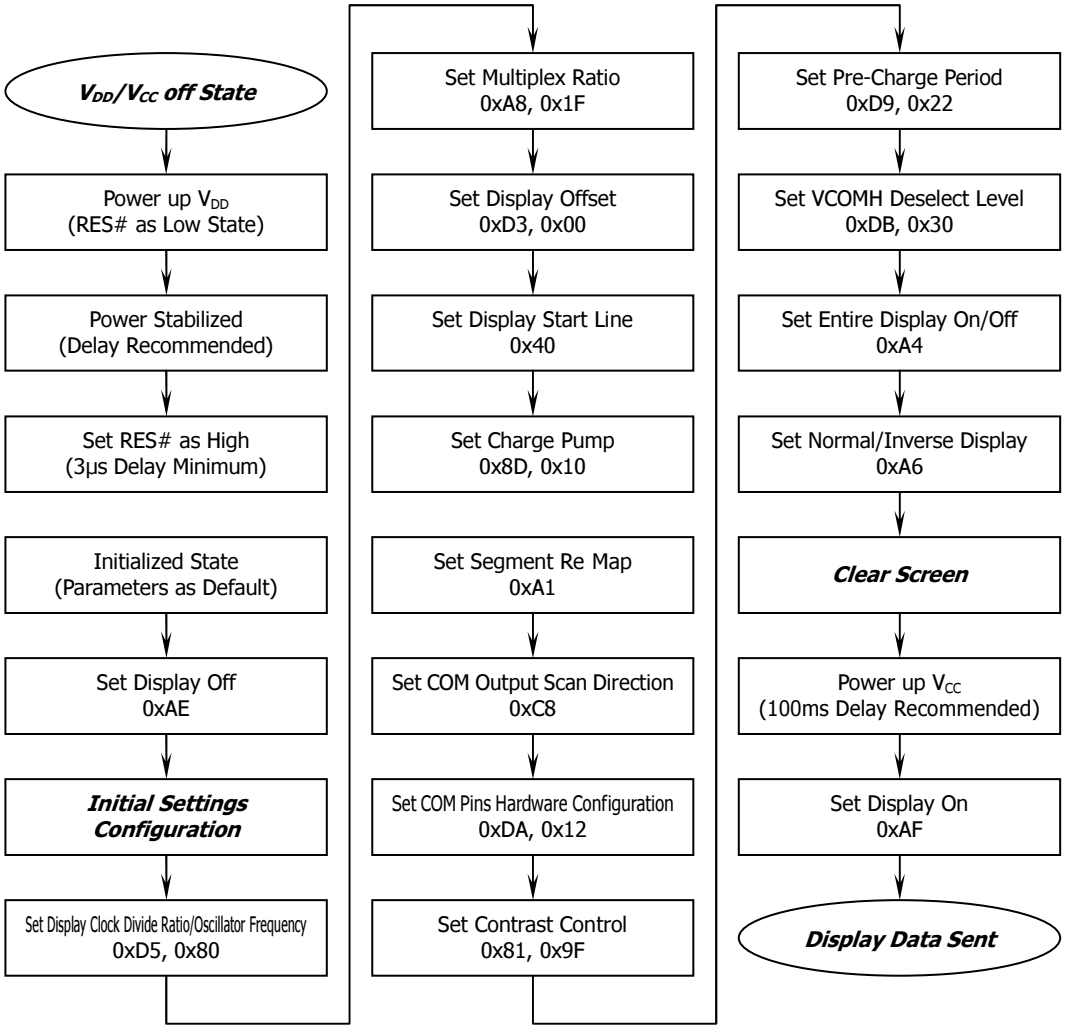
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128x64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

9 Example Application

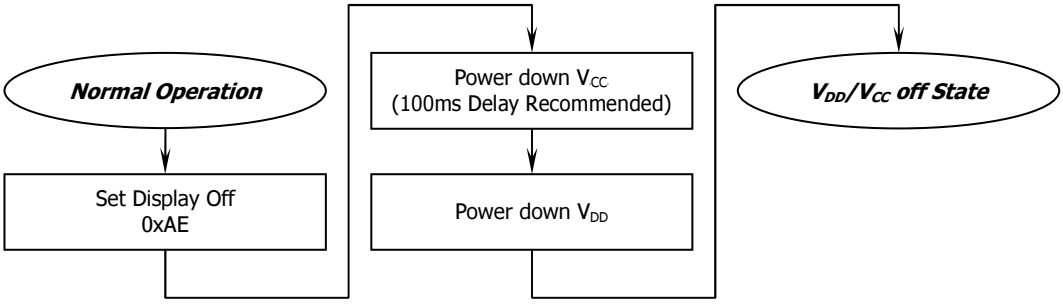
VCC Supplied Externally

<Power up Sequence>

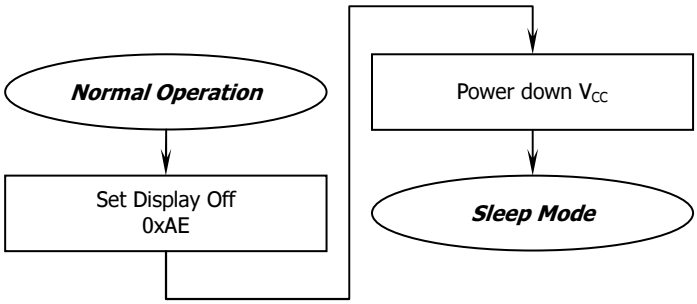


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

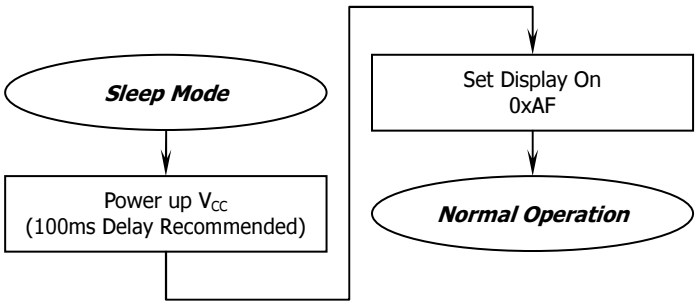
<Power down Sequence>



<Entering Sleep Mode>

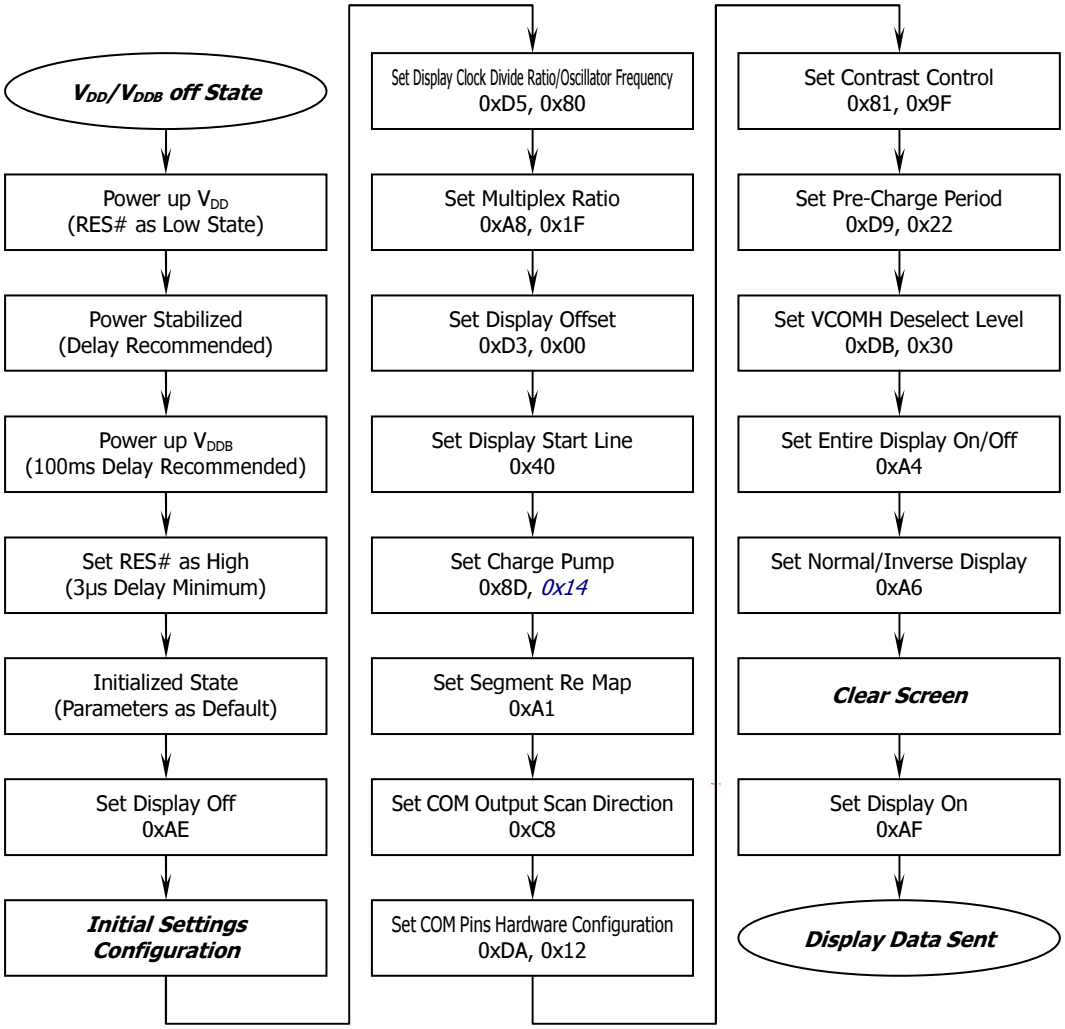


<Exiting Sleep Mode>



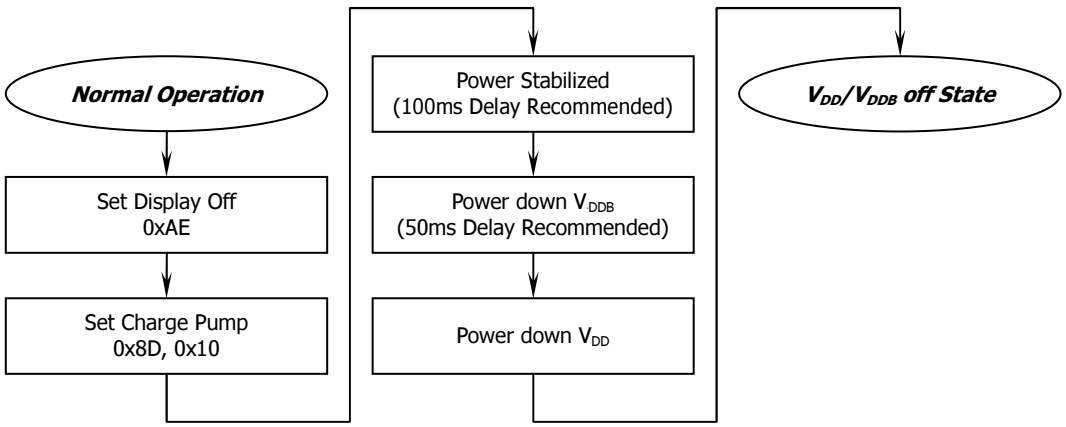
VCC Generated by Internal DC/DC Circuit

<Power up Sequence>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



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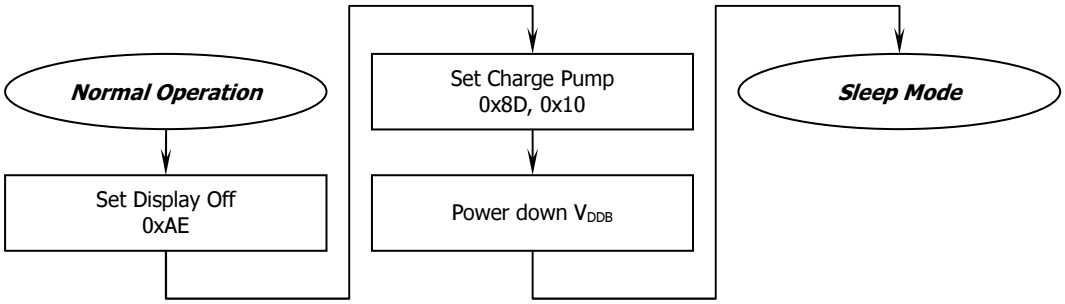

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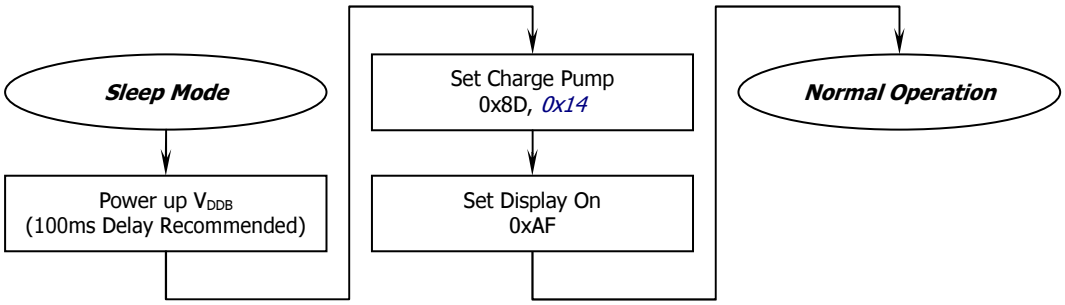
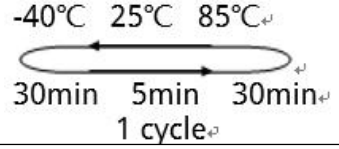


10 Command Table

Please check Driver IC datasheet

11 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85°C 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85°C 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 °C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40°C/85°C 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container.

12 Warranty and Conditions

http://www.displaymodule.com/pages/faq