DisplayModule

DM-OLED096-658

0.96" 64 × 128 MONOCHROME GRAPHIC OLED DISPLAY MODULE - SPI

Contents

1 Revision History

Date	Changes
2019-08-08	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	0.96	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome(White)	Colors
Resolution	64 x 128	pixel
Controller IC	SH1107	-
Interface	SPI	-
Active Area	10.86 ×21.74	mm
Module Dimension	14 × 28 × 1.22	mm
Pixel Size	0.15 × 0.15	mm
Pixel Pitch	0.17 × 0.17	mm
Drive Duty	1/128Duty	-
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

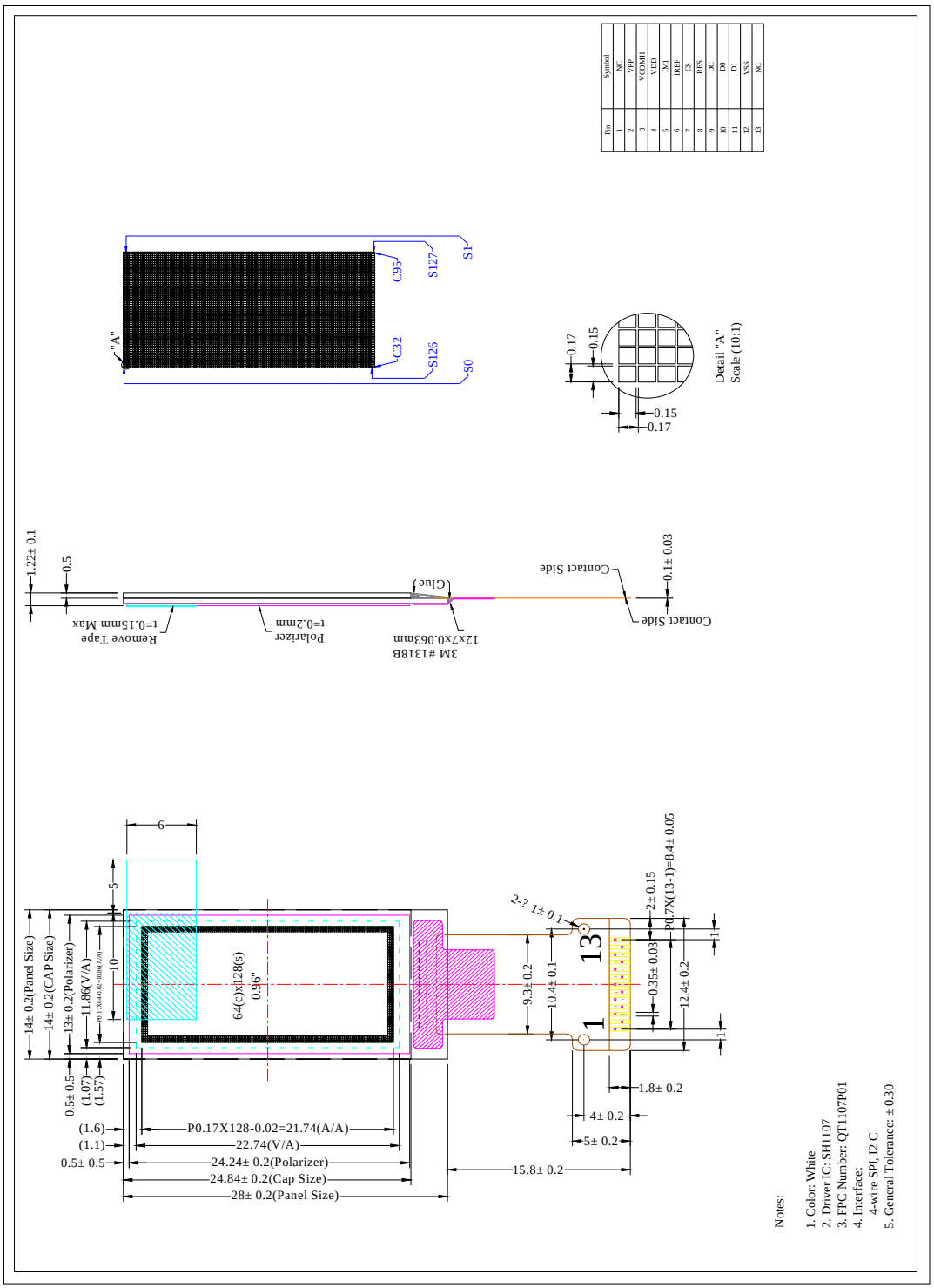
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1,13</td><td>NC</td><td>Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>2</td><td>VPP</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. It must be supplied externally.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>4</td><td>VDD</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>5</td><td>IM1</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>IM1</td></tr>
<tr><td>4-wire SPI</td><td>0</td></tr>
<tr><td>I²C</td><td>1</td></tr>
</table></td></tr>
<tr><td>6</td><td>IREF</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5 A maximum.</td></tr>
<tr><td>7</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>8</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>9</td><td>A0</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SI will be interpreted as data. When it is pulled low, the data at SI will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>10,11</td><td>D0,D1</td><td>Serial Data Input/Output and clock
When serial mode is selected, D1 will be the serial data input SI and D0 will be the serial clock input SCL.
When I 2 C mode is selected, D1 be the serial data input SDA and D0 is the serial clock input, SCL.</td></tr>
<tr><td>12</td><td>VSS</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
</table>

3.2 Module Pin Description

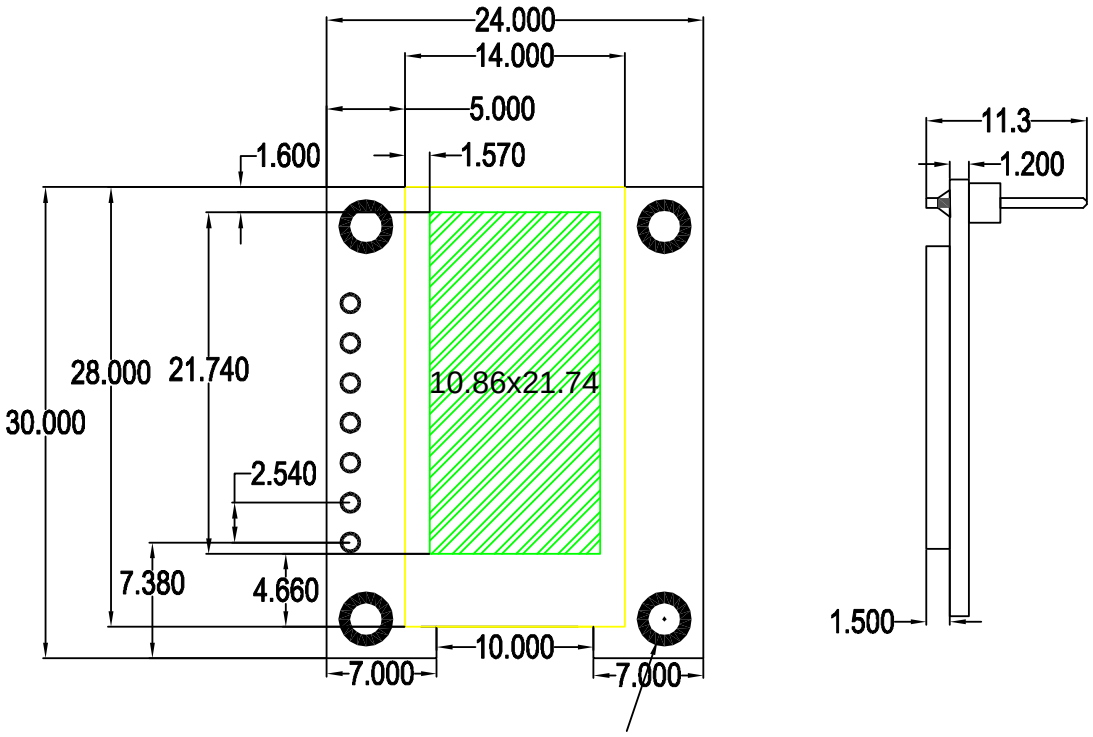
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC	Power Supply 3.3V~5V
3	SCL	When SPI interface, is SPI clock line(default); When IIC interface, is the IIC clock line.
4	SDA	When SPI interface, is SPI data line(default); When IIC interface, is IIC data line.
5	RES	OLED reset Pin OLED needs to be reset once powered on.
6	D/C	When SPI interface, is Data/Command control pin(default); When IIC interface, used to set the IIC address.
7	CS	OLED SPI Chip Select The low level is effective, if do not want to use must be grounded.

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



The distance from the center of the four holes to the plate edge is 2.5mm, with an inner diameter of 2mm and an outer diameter of 3.5mm

5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles	(V)θ	-	Free	-	°	-
C.I.E(White)	(x) (y)	0.25 0.27	0.29 0.31	0.33 0.35	-	CIE 1931
Brightness	L_{br}	120	160	-	cd/m²	V_{PP} Supplied Externally
Contrast Ratio	CR	-	>10000:1	-	-	Dark

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Display Supply Voltage	V_{PP}	7	16.5	V	Note1,2
Logic Supply Voltage	V_{DD}	-0.3	3.6	V	Note1,2
Operating Temperature	TOP	-40	70	℃	-
Storage Temperature	TSTG	-40	85	℃	Note3
Life Time (150 cd/m²)		10,000	-	hour	Note4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

Note 4: End of lifetime is specified as 50% of initial brightness reached. The reference average operation life time at room temperature is estimated by the accelerated at high temperature conditions.

5.3 DC Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Remark
Display Supply Voltage	V_{PP}	8.5	9.0	9.5	V	Note1
Logic Supply Voltage	V_{DD}	1.65	2.8	3.5	V	-
Low Level Input Voltage	V_{IL}	0	-	0.2 x V_{DD}	V	I_{OUT}=100μA, 3.3MHz
High Level Input Voltage	V_{IH}	0.8 x V_{DD}	-	V_{DD}	V	I_{OUT}=100μA, 3.3MHz
Low Level Output Voltage	V_{OL}	0	-	0.2 x V_{DD}	V	I_{OUT}=100μA, 3.3MHz
High Level Output Voltage	V_{OH}	0.8 x V_{DD}	-	V_{DD}	V	I_{OUT}=100μA, 3.3MHz
V_{PP} Operating Current	I_{PP}	-	11	16	mA	Note2
V_{CI} Operating Current	I_{DD}	-	55	100	μA	
V_{PP} Sleep Mode Current	$I_{PP, SLEEP}$	-	0.5	5	μA	
V_{DD} Sleep Mode Current	$I_{DD, SLEEP}$	-	0.1	5	μA	

Note1: Brightness (L_{br}) and Supply Voltage for Display (V_{PP}) are subject to the change of the panel characteristics and the customer's request.

Note2: V_{DD} = 2.8V, V_{PP} = 9.0V, 100% Display Area Turn on.

5.4 AC Characteristics

5.4.1 Serial Interface Timing Characteristics:4-wire Serial(default)

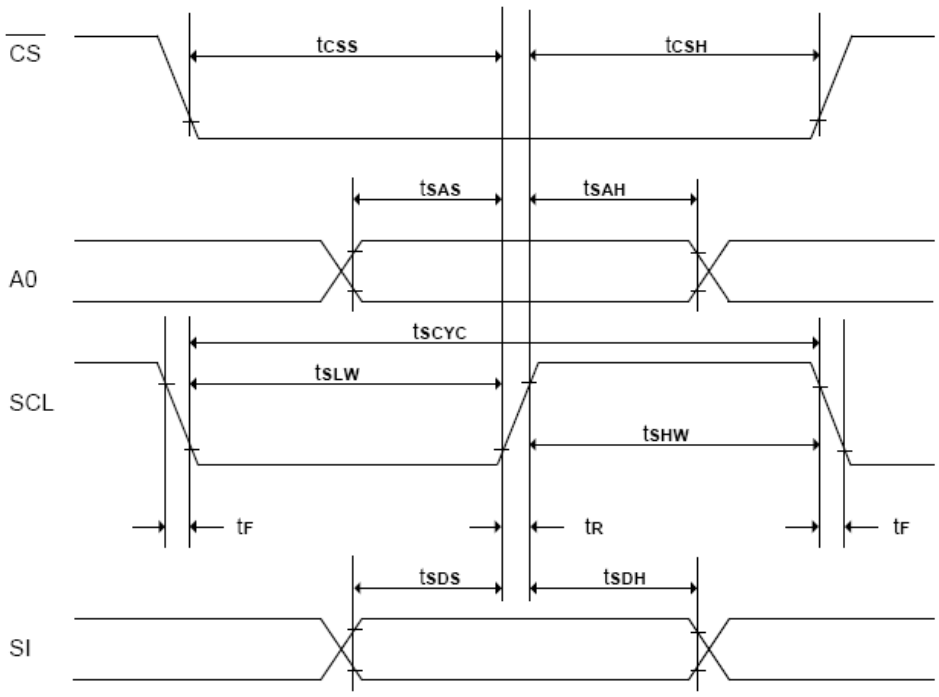
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	500	-	ns
t_{SAS}	Address Setup Time	300	-	ns
t_{SAH}	Address Hold Time	300	-	ns
t_{SDS}	Data Setup Time	200	-	ns
t_{SDH}	Data Hold Time	200	-	ns
t_{CSS}	Chip Select Setup Time	240	-	ns
t_{CSH}	Chip Select Hold Time	120	-	ns
t_{SHW}	Serial Clock H Pulse Width	200	-	ns
t_{SLW}	Serial Clock L Pulse Width	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

* (V_{DD} -V_{SS} = 1.65V to 2.4V, T_A = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{SAS}	Address Setup Time	150	-	ns
t_{SAH}	Address Hold Time	150	-	ns
t_{SDS}	Data Setup Time	100	-	ns
t_{SDH}	Data Hold Time	100	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{SHW}	Serial Clock H Pulse Width	100	-	ns
t_{SLW}	Serial Clock L Pulse Width	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} -V_{SS} = 2.4V to 3.5V, T_A = 25°C)

Figure 5-1 : Serial interface characteristics (4-wire SPI)

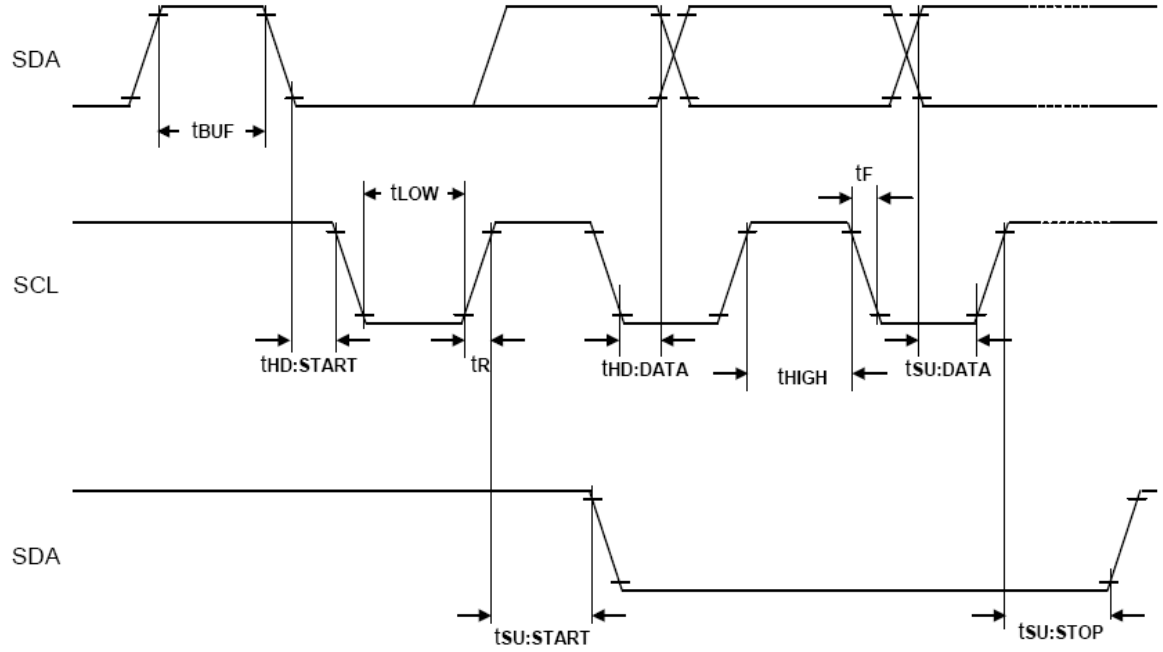


5.4.2 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
fscl	SCL clock frequency	DC	400	kHz
T_{LOW}	SCL clock Low pulse width	1.3	-	µs
T_{HIGH}	SCL clock H pulse width	0.6	-	µs
$T_{SU:DATA}$	data setup time	100	-	ns
$T_{HD:DATA}$	data hold time	0	0.9	µs
T_R	Rise Time	20+0.1Cb	300	ns
T_F	Fall Time	20+0.1Cb	300	ns
Cb	Capacity load on each bus line	-	400	pF
$T_{SU:START}$	Setup timefor re-START	0.6	-	µs
$T_{HD:START}$	START Hold time	0.6	-	µs
$T_{SU:STOP}$	Setup time for STOP	0.6	-	µs
T_{BUF}	Bus free times between STOP and START condition	1.3	-	µs

* (V_{CI} -V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Figure 5-2 : I²C interface Timing characteristics



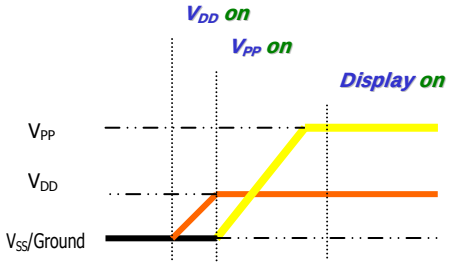
6 Functional Specification

6.1 Commands

Refer to the Technical Manual for the SH1107.

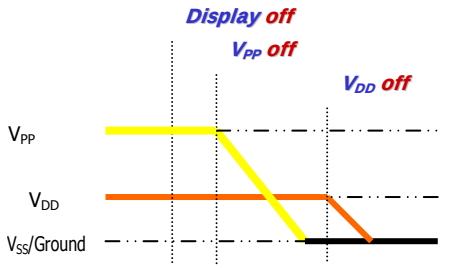
6.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.



6.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{PP}
6. Delay 100ms (When V_{PP} is stable)
7. Send Display on command



6.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
4. (When V_{PP} is reach 0 and panel is completely discharges)
5. Power down V_{DD}

Note 9:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{PP} becomes lower than V_{DD} whenever V_{DD} is ON and V_{PP} is OFF.
2) V_{PP} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{PP}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{PP} power down.

6.3 Reset Circuit

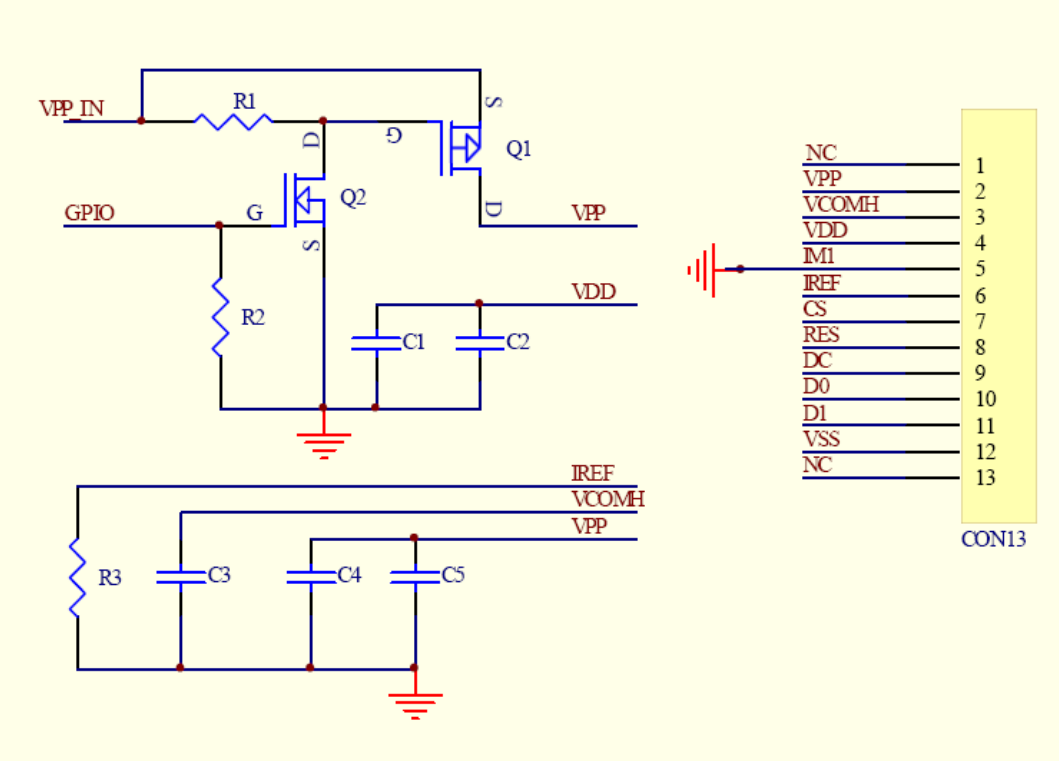
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF. 1.Common and Segment are in high impedance state.
2. 128 x 128 Display Mode
3. Normal segment and display data column and row address mapping (3.SEG0 is mapped to the top line of the display)
4. Shift register data clear in serial interface
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 80h
8. Internal DC-DC is selected

6.4 Application circuit reference

6.4.1 4-wire Serial Interface(default)

Special Tips: When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current.



Recommended Components:

C1: 0.1µF / 6.3V, X5R

C2: 4.7µF / 6.3V, X5R

C3: 2.2µF / 16V, X7R

C4: 4.7µF / 16V, X7R

C5: 0.1µF / 16V, X7R

R3: 560kΩ, R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ

Q1: FDN338P

Q2: FDN335N

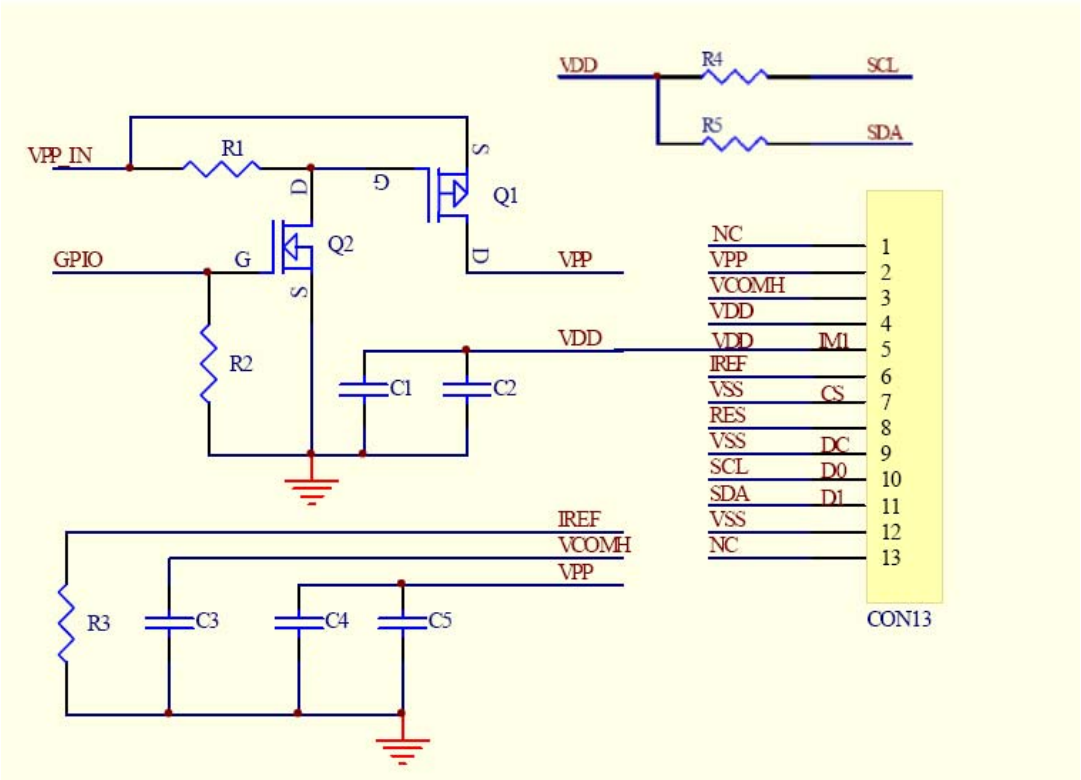
Notes:

VDD: 1.65~3.5V, it should be equal to MCU I/O voltage.

V_{PP_IN}: 8.5~9.5V

6.4.2 I_2C Interface

Special Tips: When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current.



Recommended Components:

C1: 0.1µF / 6.3V, X5R

C2: 4.7µF / 6.3V, X5R

C3: 4.7µF / 16V, X7R

C4: 4.7µF / 16V, X7R

C5: 0.1µF / 16V, X7R

R3: 560kΩ, R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ

R4, R5: 4.7kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

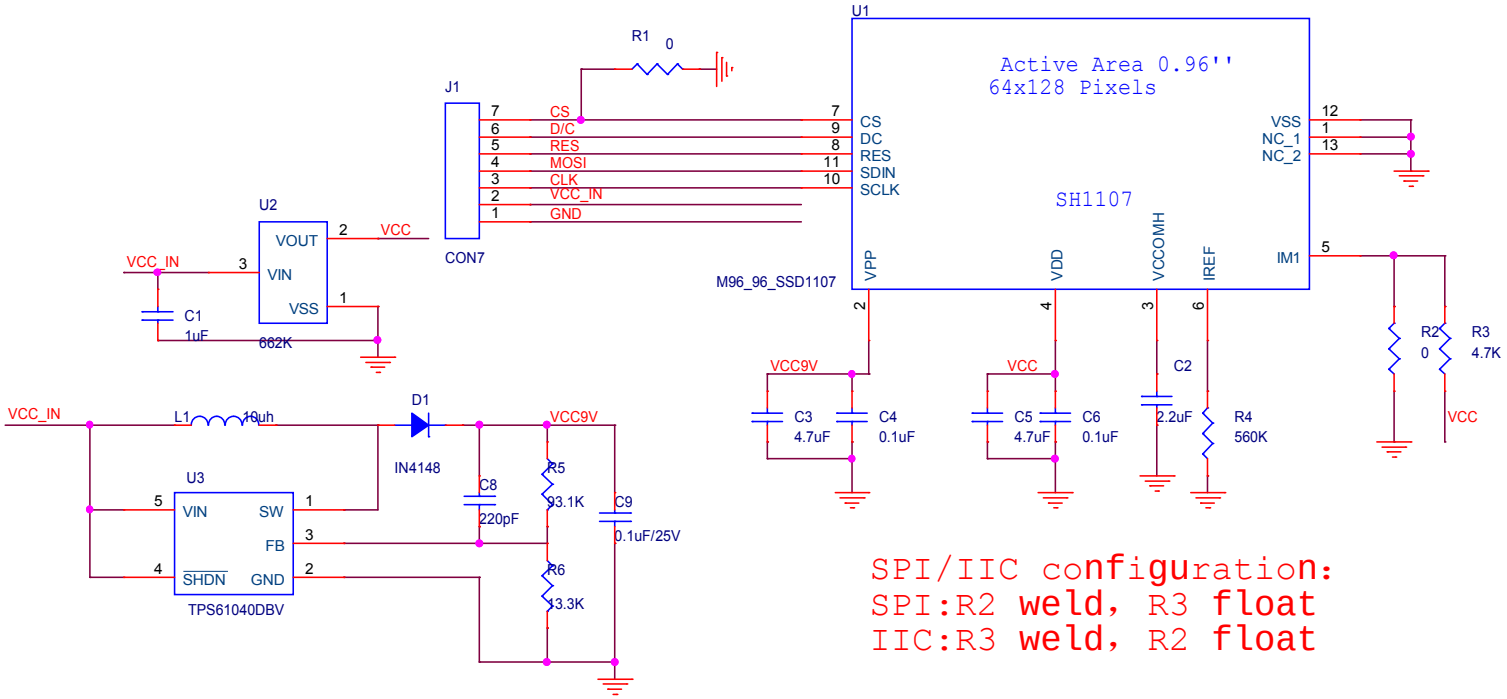
VDD: 1.65~3.5V, it should be equal to MCU I/O voltage.

V_{PP_IN}: 8.5~9.5V

6.5 reference code

```
void sh1107()
{       write_i(0xAE);  /*display off*/

        write_i(0x00);  /*set lower column address*/
        write_i(0x10);  /*set higher column address*/

        write_i(0xB0);  /*set page address*/

        write_i(0xdc);  /*set display start line*/
        write_i(0x00);

        write_i(0x81);  /*contract control*/
        write_i(0x2f);  /*128*/

        write_i(0x20);  /* Set Memory addressing mode (0x20/0x21) */

        write_i(0xA0);  /*set segment remap*/

        write_i(0xC0);  /*Com scan direction*/

        write_i(0xA4);  /*Disable Entire Display On (0xA4/0xA5)*/

        write_i(0xA6);  /*normal / reverse*/

        write_i(0xA8);  /*multiplex ratio*/
        write_i(0x3F);  /*duty = 1/64*/

        write_i(0xD3);  /*set display offset*/
        write_i(0x60);

        write_i(0xD5);  /*set osc division*/
        write_i(0x51);

        write_i(0xD9);  /*set pre-charge period*/
        write_i(0x22);

        write_i(0xdb);  /*set vcomh*/
        write_i(0x35);

        write_i(0xad);  /*set charge pump enable*/
        write_i(0x8a);  /*Set DC-DC enable (a=0:disable; a=1:enable)*/

        write_i(0xAF);  /*display ON*/
}
```

7 Module Schematic



SPI/IIC configuration:
SPI:R2 weld, R3 float
IIC:R3 weld, R2 float

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85°C 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40°C 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 240hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-40°C/80°C 24cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"