DisplayModule
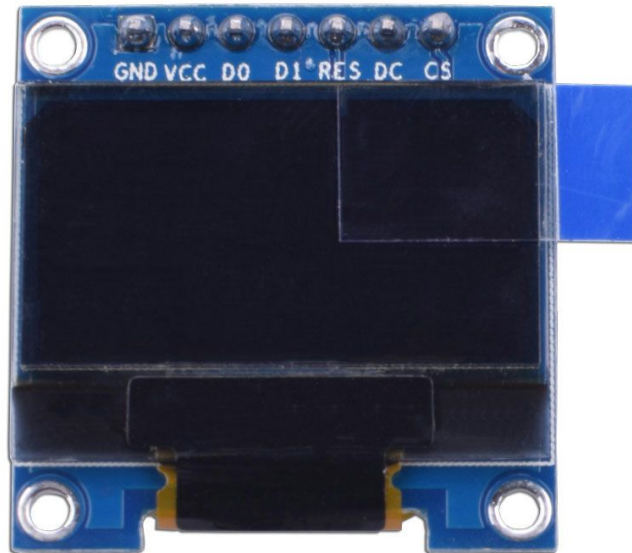

DM-OLED096-624
0.96" 128 X 64 WHITE GRAPHIC OLED DISPLAY MODULE WITH SPI, I2C INTERFACE

Contents

1   Revision History

Date	Changes
2015-12-28	First release

2   Main Features

Item	Specification	Unit
Diagonal Size	0.96"	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome (White)	Colors
Resolution	128 x 64	pixel
Controller IC	SSD1306	-
Duty	1/64	duty
Interface	SPI, I2C	-
Active Area	21.744 x 10.864	mm
Module Dimension	26.70 x 19.26 x 1.4	mm
Weight	1.54	g

3 Pin Description

3.1 Panel Pin Description

| Pin No.	Symbol	Function Description
1	NC(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.
2-3 4-5	C2P/C2N C1P/C1N	Negative Terminal of the Flying Boost Capacitor Positive Terminal of the Flying Inverting Capacitor The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
6	VDDB	Power Supply for DC/DC Converter Circuit This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.
7	NC	Reserved Pin The N.C. pin between function pins are reserved for compatible and flexible design.
8	VSS	Ground of Logic Circuit This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
9	VDD	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.
10 11 12	BS0 BS1 BS2	Communicating Protocol Select These pins are MCU interface selection input. See the following table: |	BS0	BS1	BS2
---	---	---	---
I2C	0	1	0
3-wire SPI	1	0	0
4-wire SPI	0	0	0
8-bit 68XX Parallel	0	0	1
8-bit 80XX Parallel	0	1	1	
13	CS#	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
14	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
15	D/C#	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.

|		For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
16	R/W#	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
17	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
18-25	D0-D7	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.
26	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5μA maximum.
27	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
28	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
29	VLSS	Ground of Analog Circuit This is an analog ground pin. It should be connected to VSS externally.
30	NC(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

3.2 Module Pin Description

Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC_IN	Power Supply (2.8~5.5V)
3-4	D0-D1	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.
5	RES	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
6	D/C	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
7	CS	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

4 Mechanical Drawing

4.1 Panel Mechanical Drawing
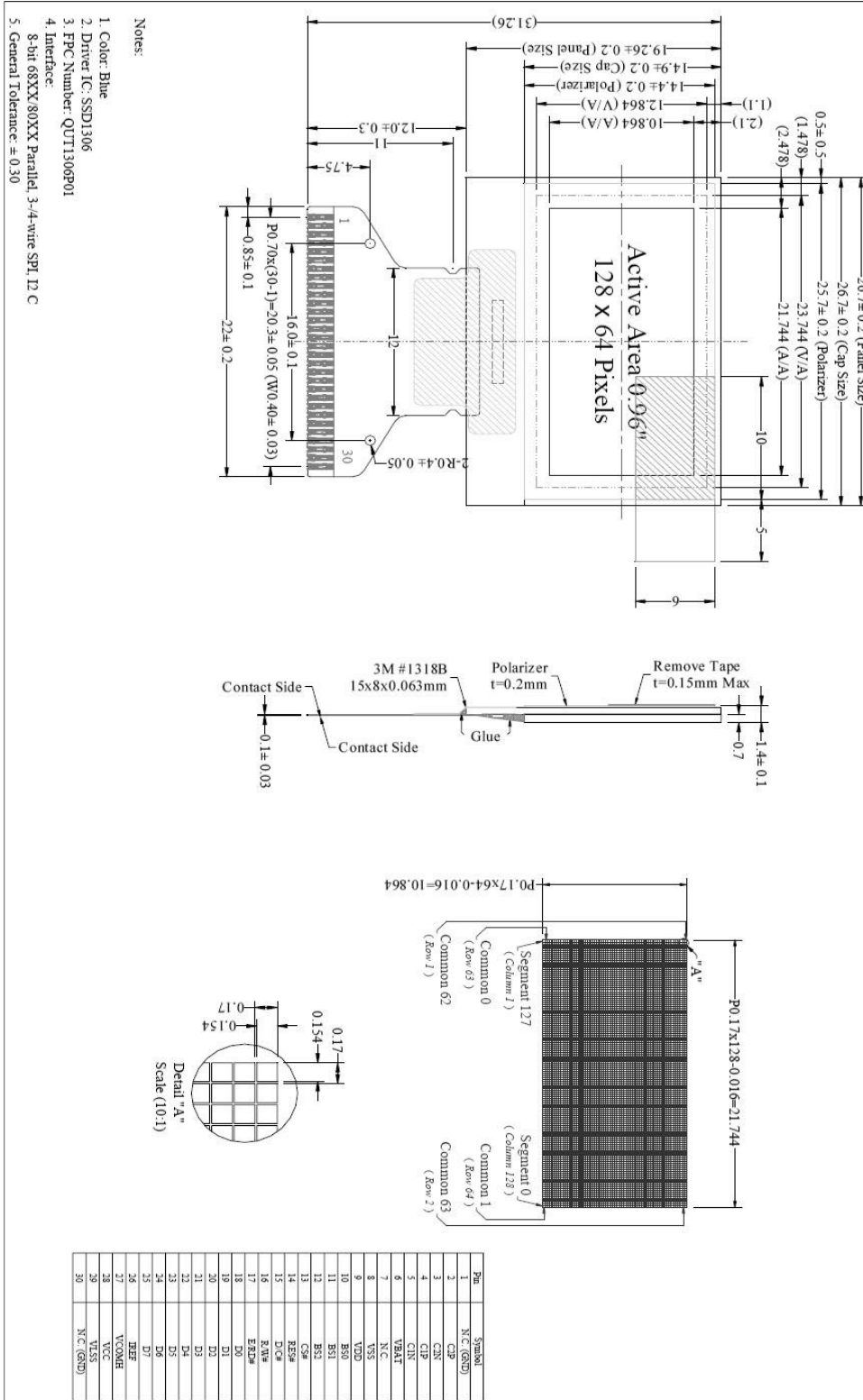
4.2   Module Mechanical Drawing
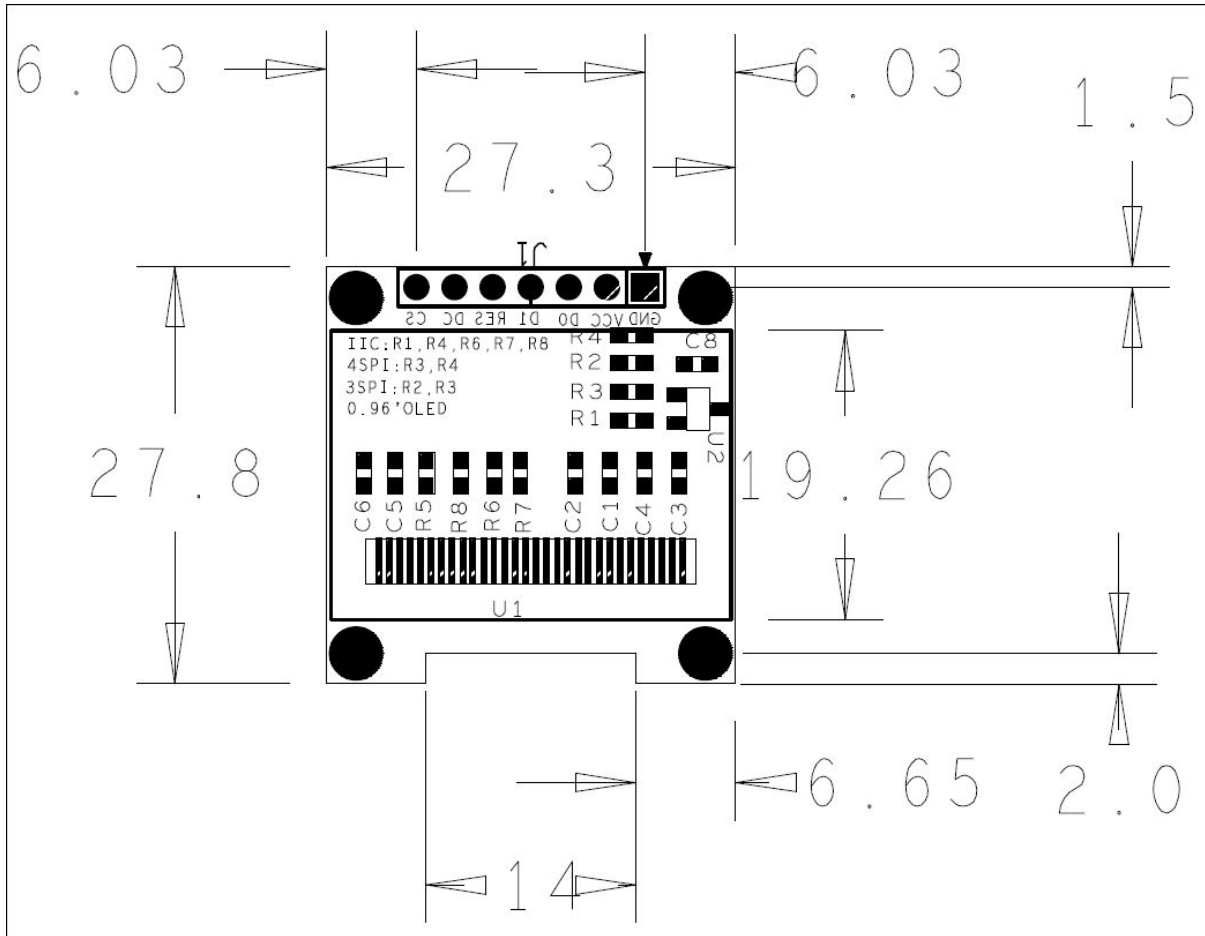
5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage for Logic	VDD		1.65	2.8	3.3	V
Operating Current	ICC	Note 1		12.3	15.4	mA
Low Level Input Voltage	V_{IL}		0	-	$0.2xV_{DD}$	V
High Level Input Voltage	V_{IH}		$0.8xV_{DD}$	-	V_{DD}	V
Low Level Output Voltage	V_{OL}		0		$0.1xV_{DD}$	V
High Level Output Voltage	V_{OH}		$0.9xV_{DD}$		V_{DD}	V
Operating Temperature	TOP	Absolute Max	-40		85	℃
Storage Temperature	TST	Absolute Max	-40		85	℃

Note 1: VDD = 2.8V, VCC = 12V, IREF=910K 100% Display Area Turn on.

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles			Free		°
Response Time (25°C)	Tr + Tf				us
Brightness			100	120	cd/m²
Contrast Ratio	CR		2,000:1		
Lifetime		10,000			Hrs

7 Timing Characteristics

7.1 Serial Interface Timing Characteristics (4-wire SPI)

TA=25℃,VDD-VSS=1.65-3.5V

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

7.2 Serial Interface Timing Characteristics (3-wire SPI)

TA=25℃,VDD-VSS=1.65-3.5V

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_{R}	Rise Time	-	-	40	ns
t_{F}	Fall Time	-	-	40	ns

7.3 I2C Interface Timing Characteristics

TA=25℃,VDD-VSS=1.65-3.5V

| Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	-	μs
t_{HD}	Data Hold Time (for "SDA$_{OUT}$" Pin)	0	-	-	ns
	Data Hold Time (for "SDA$_{IN}$" Pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start Condition)	0.6	-	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	-	μs
t_R	Rise Time for Data and Clock Pin	-	-	300	ns
t_F	Fall Time for Data and Clock Pin	-	-	300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	-	μs
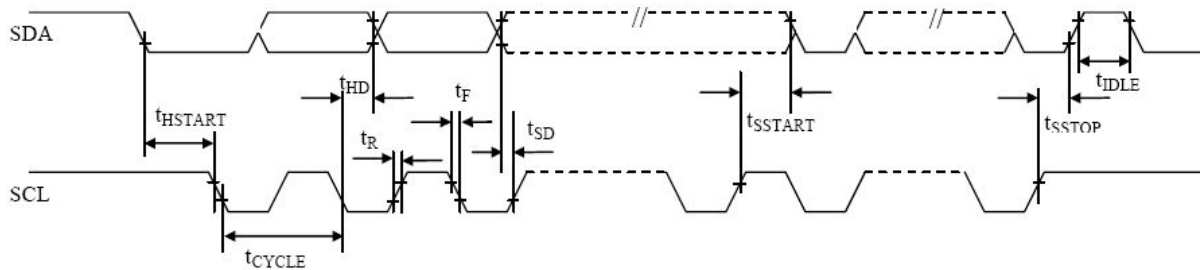
8 Functional Specification

8.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.
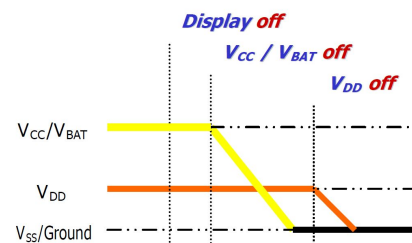
Power up Sequence

1. Power up V_{DD}/V_{BAT}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms(When V_{CC} is stable)
7. Send Display on command
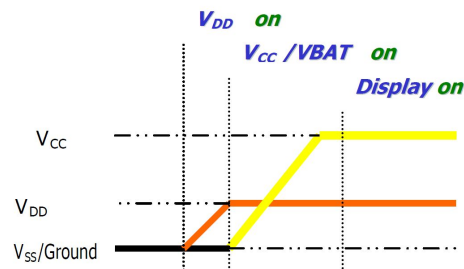
Power down Sequence

1. Send Display off command
2. Power down V_{CC}/V_{BAT}
3. Delay 100ms
   (When V_{CC}/V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}

8.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128x64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

9 Driver/Controller Information

Built-in SSD1306 Controller:

https://drive.google.com/file/d/0B5lkVYnewKTGYzhyWWp0clBMR1E/view?usp=sharing

10 Module Schematic

DisplayModule
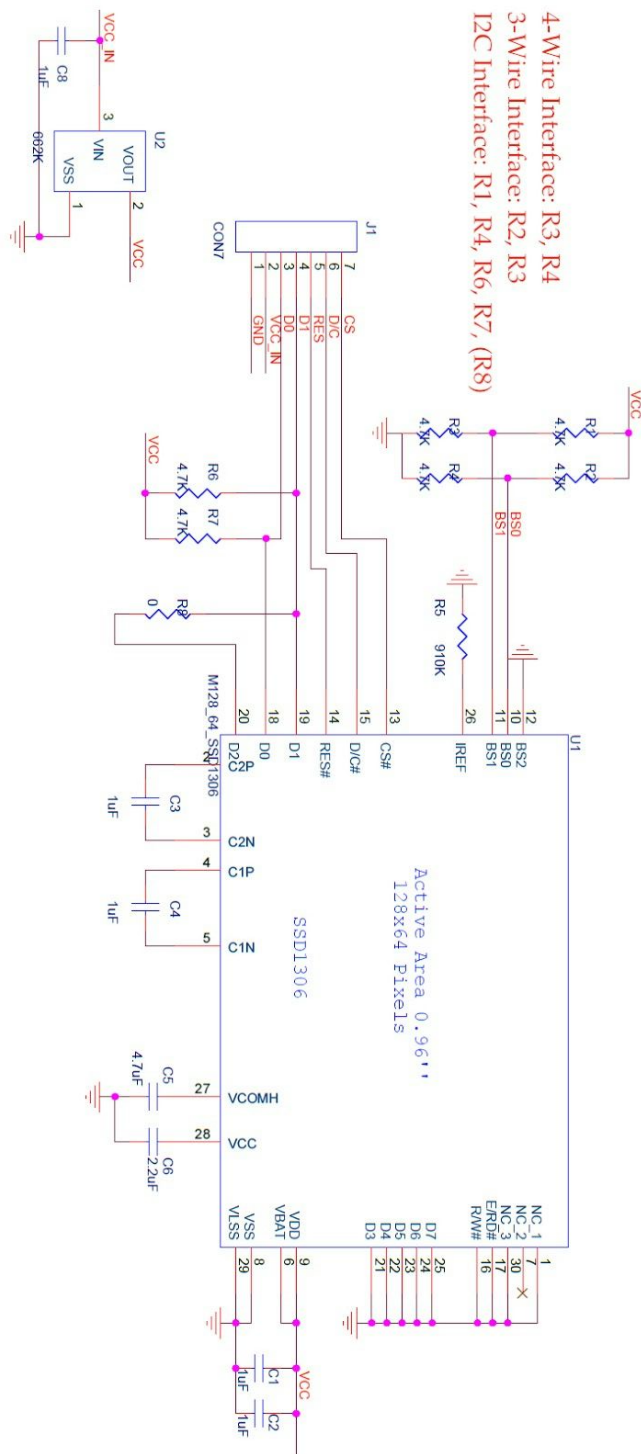
11 Example Application

VCC Supplied Externally

<Power up Sequence>
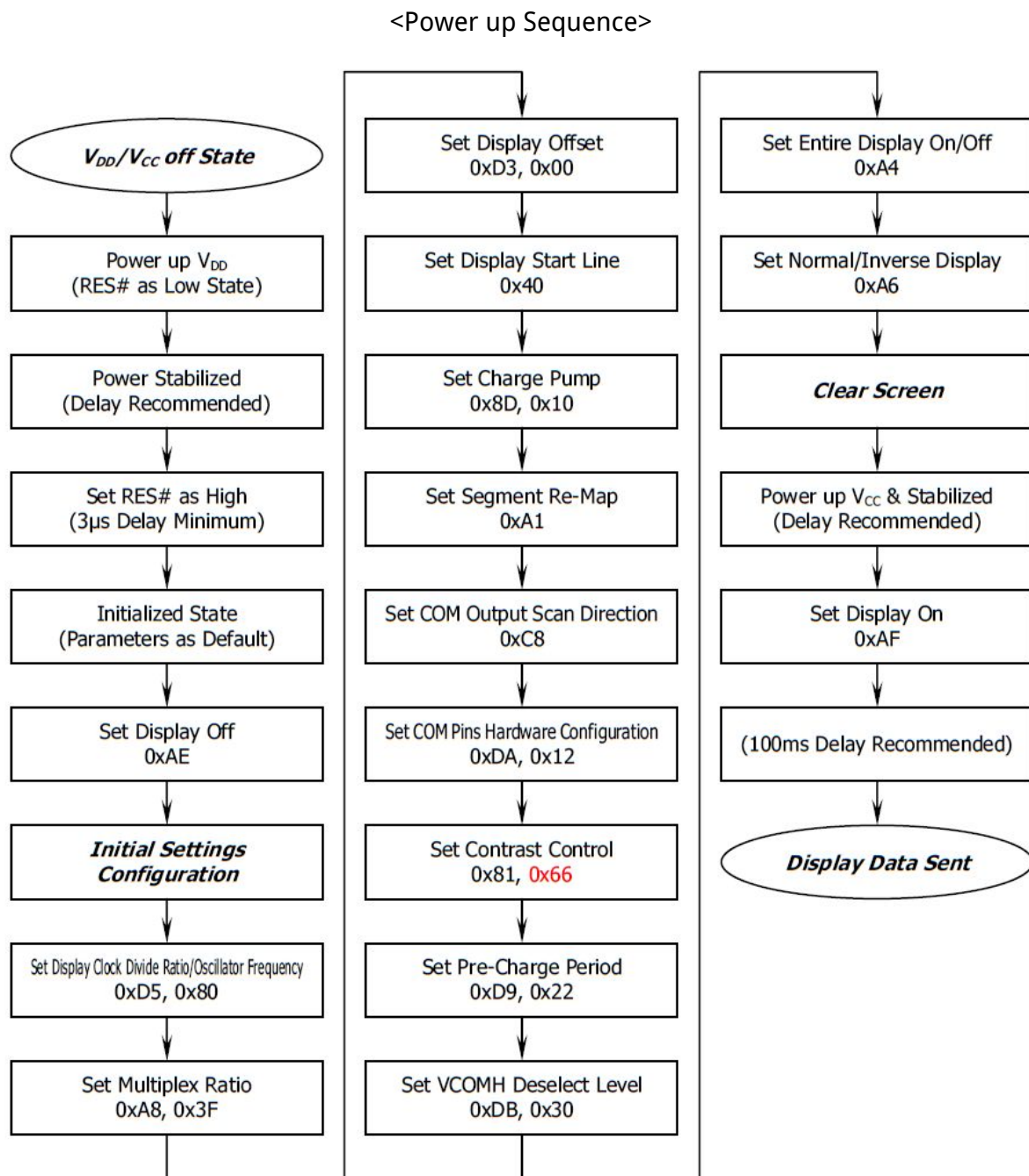
If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>

| Normal Operation | Power down V_{CC} (100ms Delay Recommended) | V_{DD}/V_{CC} off State |

Set Display Off 0xAE → Power down V_{DD}

<Entering Sleep Mode>

Normal Operation → Set Display Off 0xAE → Power down V_{CC} → **Sleep Mode**

<Exiting Sleep Mode>

Sleep Mode → Power up V_{CC} & Stabilized (Delay Recommended) → Set Display On 0xAF → (100ms Delay Recommended) → *Normal Operation*
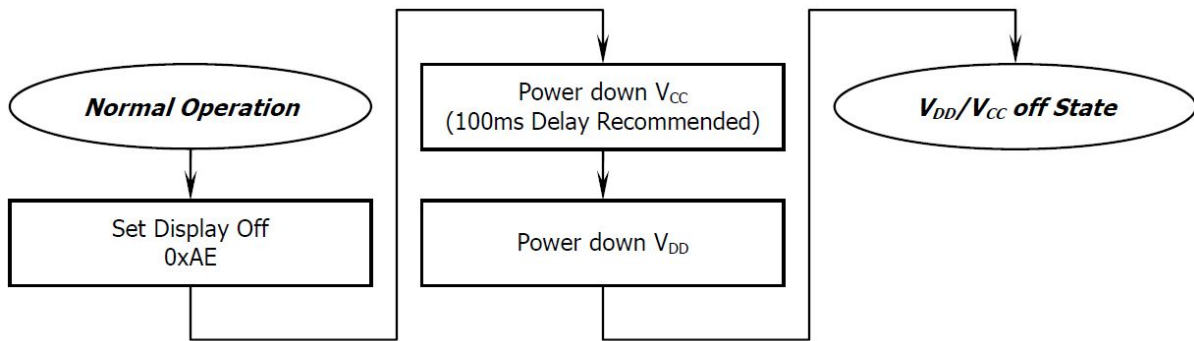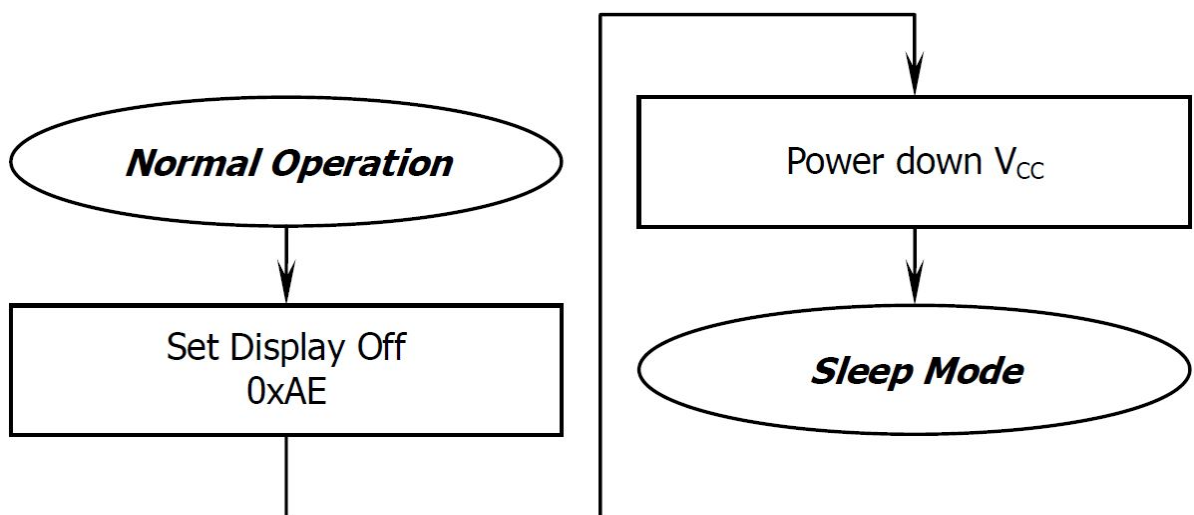
External setting
```
{
    RES=1;
    delay(1000);
    RES=0;
    delay(1000);
    RES=1;
    delay(1000);
```

```
        write_i(0xAE);       /*display off*/

        write_i(0x00);       /*set lower column address*/
        write_i(0x10);       /*set higher column address*/

        write_i(0x40);       /*set display start line*/

        write_i(0xB0);       /*set page address*/

        write_i(0x81);       /*contract control*/
        write_i(0x66);       /*128*/

        write_i(0xA1);       /*set segment remap*/

        write_i(0xA6);       /*normal / reverse*/

        write_i(0xA8);       /*multiplex ratio*/
        write_i(0x3F);       /*duty = 1/64*/

        write_i(0xC8);       /*Com scan direction*/

        write_i(0xD3);       /*set display offset*/
        write_i(0x00);

        write_i(0xD5);       /*set osc division*/
        write_i(0x80);

        write_i(0xD9);       /*set pre-charge period*/
        write_i(0x1f);

        write_i(0xDA);       /*set COM pins*/
        write_i(0x12);

        write_i(0xdb);       /*set vcomh*/
        write_i(0x30);

        write_i(0x8d);       /*set charge pump disable*/
        write_i(0x10);

        write_i(0xAF);       /*display ON*/
        }

void write_i(unsigned char ins)
{

        DC=0;
        CS=0;
        WR=1;
```
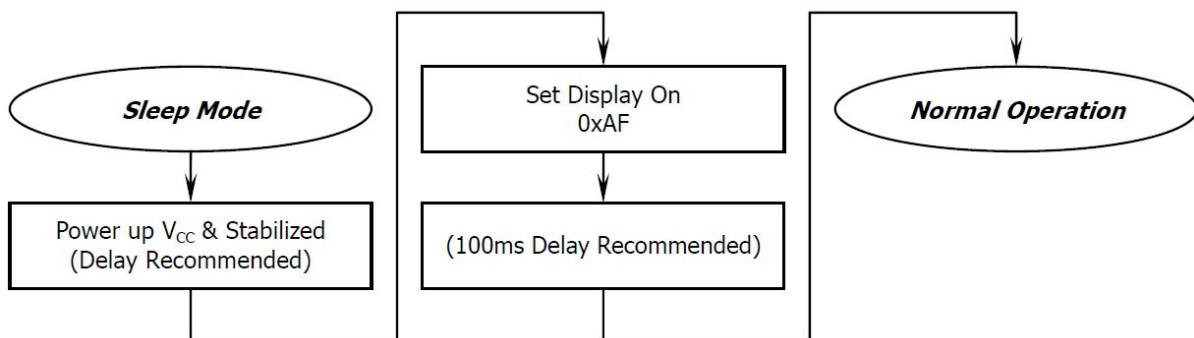
```
        P1=ins;        /*inst*/
        WR=0;
        WR=1;
        CS=1;
}

void write_d(unsigned char dat)
{
        DC=1;
```

12 Command Table

1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	81	1	0	0	0	0	0	0	1	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll
0	A[7:0]	0	0	0	0	0	0	0	0		27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h)
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		B[2:0] : Define start page address
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	0	0	0	0		
0	F[7:0]	1	1	1	1	1	1	1	1		

B[2:0] : Define start page address

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
010b – PAGE2	101b – PAGE5	

C[2:0] : Set time interval between each scroll step in terms of frame frequency

000b – 5 frames	100b – 3 frames
001b – 64 frames	101b – 4 frames
010b – 128 frames	110b – 25 frame
011b – 256 frames	111b – 2 frame

D[2:0] : Define end page address

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
010b – PAGE2	101b – PAGE5	

The value of D[2:0] must be larger or equal to B[2:0]

E[7:0] : Dummy byte (Set as 00h)

F[7:0] : Dummy byte (Set as FFh)

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte
0	A[2:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		

B[2:0] : Define start page address

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
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D[2:0] : Define end page address

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
010b – PAGE2	101b – PAGE5	

The value of D[2:0] must be larger or equal to B[2:0]

E[5:0] : Vertical scrolling offset
e.g. E[5:0]= 01h refer to offset =1 row
E[5:0] =3Fh refer to offset =63 rows

Note
[1] No continuous vertical scrolling is available.

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. Note [1] After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:

Valid command sequence 1: 26h ;2Fh.
Valid command sequence 2: 27h ;2Fh.
Valid command sequence 3: 29h ;2Fh.
Valid command sequence 4: 2Ah ;2Fh.

For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

DisplayModule logo

DM-OLED096-624

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A3	1	0	1	0	0	0	1	1	Set Vertical Scroll Area	$A[5:0]$: Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0]
0	$A[5:0]$	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	$B[6:0]$	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		$B[6:0]$: Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]

Note
[1] $A[5:0]+B[6:0] <=$ MUX ratio
[2] $B[6:0] <=$ MUX ratio
[3a] Vertical scrolling offset ($E[5:0]$ in 29h/2Ah) < $B[6:0]$
[3b] Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < $B[6:0]$
[4] The last row of the scroll area shifts to the first row of the scroll area.
[5] For 64d MUX display
$A[5:0]$ = 0, $B[6:0]$=64 : whole area scrolls
$A[5:0]$= 0, $B[6:0]$ < 64 : top area scrolls
$A[5:0]$ + $B[6:0]$ < 64 : central area scrolls
$A[5:0]$ + $B[6:0]$ = 64 : bottom area scrolls
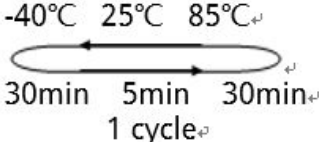
3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using $X[3:0]$ as data bits. The initial display line register is reset to 0000b after RESET. Note [1] This command is only for page addressing mode
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using $X[3:0]$ as data bits. The initial display line register is reset to 0000b after RESET. Note [1] This command is only for page addressing mode
0	20	0	0	1	0	0	0	0	0	Set Memory Addressing Mode	$A[1:0]$ = 00b, Horizontal Addressing Mode $A[1:0]$ = 01b, Vertical Addressing Mode $A[1:0]$ = 10b, Page Addressing Mode (RESET) $A[1:0]$ = 11b, Invalid
0	$A[1:0]$	*	*	*	*	*	*	A_1	A_0		
0	21	0	0	1	0	0	0	0	1	Set Column Address	Setup column start and end address $A[6:0]$: Column start address, range : 0-127d, (RESET=0d)
0	$A[6:0]$	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	$B[6:0]$	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		$B[6:0]$: Column end address, range : 0-127d, (RESET =127d) Note [1] This command is only for horizontal or vertical addressing mode.

3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	22	0	0	1	0	0	0	1	0	Set Page Address	Setup page start and end address
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		A[2:0] : Page start Address, range : 0-7d, (RESET = 0d)
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) **Note** [1] This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. **Note** [1] This command is only for page addressing mode

4. Hardware Configuration (Panel resolution & layout related) Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N −1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0	D3	1	1	0	1	0	0	1	1	Set Display Offset	Set vertical shift by COM from 0d~63d
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00h after RESET.
0	DA	1	1	0	1	1	0	1	0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap
0	A[5:4]	0	0	A_5	A_4	0	0	1	0		

5. Timing & Driving Scheme Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D5	1	1	0	1	0	1	0	1	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0	D9	1	1	0	1	1	0	0	1	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0	DB	1	1	0	1	1	0	1	1	Set V_{COMH} Deselect Level	
0	A[6:4]	0	A_6	A_5	A_4	0	0	0	0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

A[6:4]	Hex code	V_{COMH} deselect level
000b	00h	~ 0.65 x V_{CC}
010b	20h	~ 0.77 x V_{CC} (RESET)
011b	30h	~ 0.83 x V_{CC}

13 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 ℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation -40℃ 25℃ 85℃ 30min 5min 30min 1 cycle	-40℃/85℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.
Note3: Test performed on product itself, not inside a container.

14 Warranty and Conditions

http://www.displaymodule.com/pages/faq