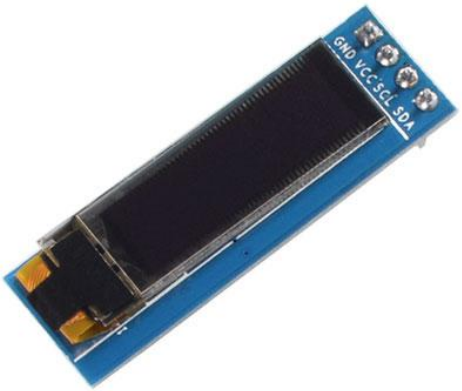
DisplayModule



DM-OLED086-646

0.86" 96 × 32 WHITE GRAPHIC OLED DISPLAY MOUDULE - I2C

Contents

1 Revision History

Date	Changes
2019-06-11	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	0.86	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome (White)	Colors
Resolution	96 x 32	pixel
Controller IC	SSD1316	-
Interface	I^2C	-
Active Area	21.1 x 6.06	mm
Module Dimension	29.1 x 9.2 x 1.2	mm
Pixel Pitch	0.22 x 0.19	mm
Weight	5	g

3 Pin Description

3.1 Panel Pin Description

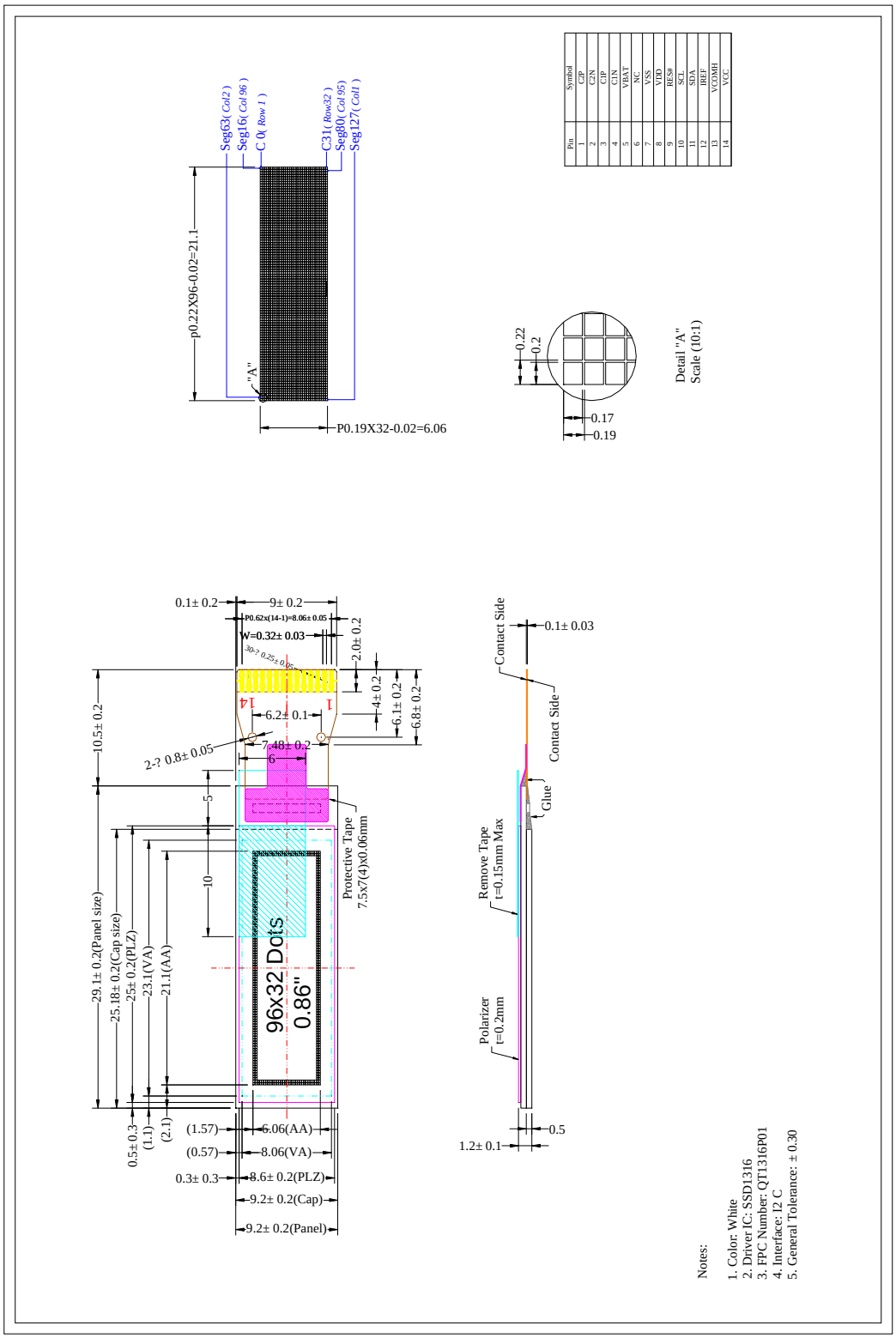
Pin No.	Symbol	Function Description
3 / 4 1 / 2	C1P / C1N C2P / C2N	**Positive Terminal of the Flying Inverting Capacitor** **Negative Terminal of the Flying Boost Capacitor** The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
5	VBAT	**Power Supply for DC/DC Converter Circuit** This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.
6	VBREF	NC
7	VSS	**Ground of Logic Circuit** This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
8	VDD	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
9	RES#	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
10	SCL	**IIC Bus Clock Signal** The transmission if information in the I2C bus is following a clock sigmal. Each transmission of data bit is taken place during a single clock period of this pin.
11	SDA	**I2C Bus Data Signal** This pin acts as a communication channel between the transmitter and the receiver.
12	IREF	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5 A maximum.capacitor should be connected between this pin and VSS.
13	VCOMH	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
14	VCC	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.

3.2 Module Pin Description

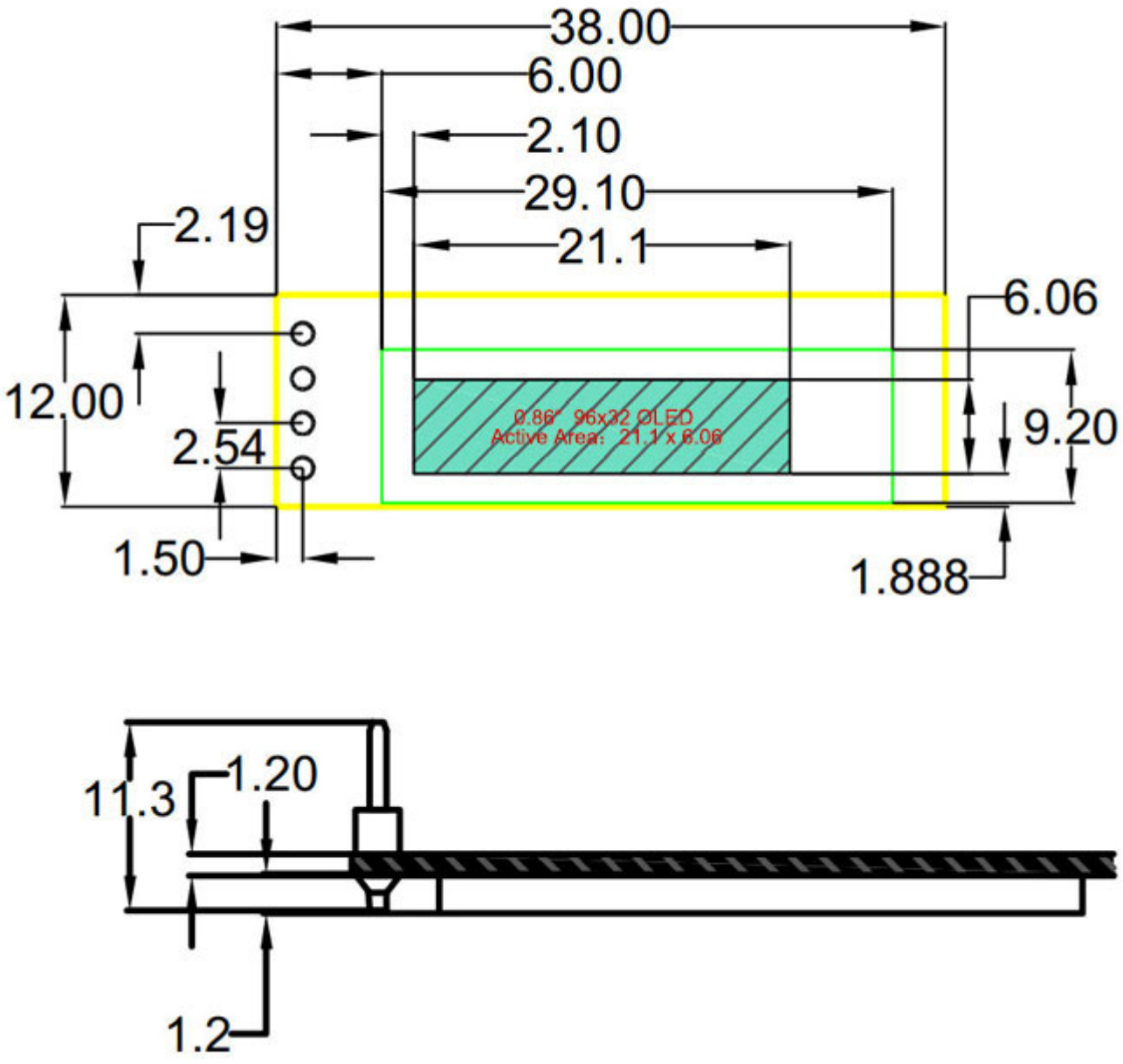
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC_IN	Power Supply 3.3V to 5V
3	SCL	SPI Clock
4	SDA	SPI DATA

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles		-	Free	-	°	
C.I.E. (White)	(x) (y)	0.28 0.31	0.32 0.35	0.36 0.39		CIE1931
Pixel Luminance (V_{CC} Supplied Externally)	L_{br}	120	-	-	cd/m²	Note 5
Standby Luminance (V_{CC} Generated by Internal DC/DC)	L_{br}	120	150	-	cd/m²	Note 6
Dark room Contrast Ratio	CR	-	2000:1	-		

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 7.25V.

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
DC/DC Supply Voltage for panel	V_{BAT}	-0.3	4.3	V	1,2
Logic Supply Voltage for panel	V_{DD}	-0.3	4	V	1,2
Display Supply Voltage for panel	V_{CC}	0	16	V	1,2
Display Supply Voltage for module	V_{CC_IN}	3.3	-	5	V
Operating Temperature	T_{OP}	-40	85	℃	
Storage Temperature	T_{STG}	-40	85	℃	3
Life Time (120 cd/m²)		10,000	-	Hour	4
Life Time (80 cd/m²)		30,000	-	hour	4
Life Time (60 cd/m²)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

Note 4: VCC = 8.0V, Ta = 25℃ 50% Checkerboard. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 DC Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
DC/DC Supply Voltage for panel	V_{BAT}	Internal DC/DC Enable	3.5	-	4.2	V
Logic Supply Voltage for panel	V_{DD}		1.65	2.8	3.3	V
Display Supply Voltage for panel (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	7	-	9	V
Display Supply Voltage for panel (Generated by Internal DC/DC)	V_{CC}	Note 6 (Internal DC/DC Disable)	7	7.25	7.5	V
Display Supply Voltage for module	V_{CC_IN}		3.3	-	5	V
Operating Current V_{BAT}	I_{BAT}	Note 7	-	15	23	mA
Operating Current V_{CC}	I_{CC}	Note 8	-	10	15	mA
Sleep Mode Current V_{DD}	$I_{DD,SLEEP}$		-	1	10	µA
Sleep Mode Current V_{CC}	$I_{CC,SLEEP}$		-	2	10	µA
Low Level Input Voltage	V_{IL}	I_{out} =100µA, 3.3MHz	0	-	0.2 x V_{DD}	V
High Level Input Voltage	V_{IH}	I_{out} =100µA, 3.3MHz	0.8 x V_{DD}	-	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{out} =100µA, 3.3MHz	0	-	0.1 x V_{DD}	V
High Level Output Voltage	V_{OH}	I_{out} =100µA, 3.3MHz	0.9 x V_{DD}	-	V_{DD}	V

Note 5 & 6 : Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 7: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.

Note 8: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.

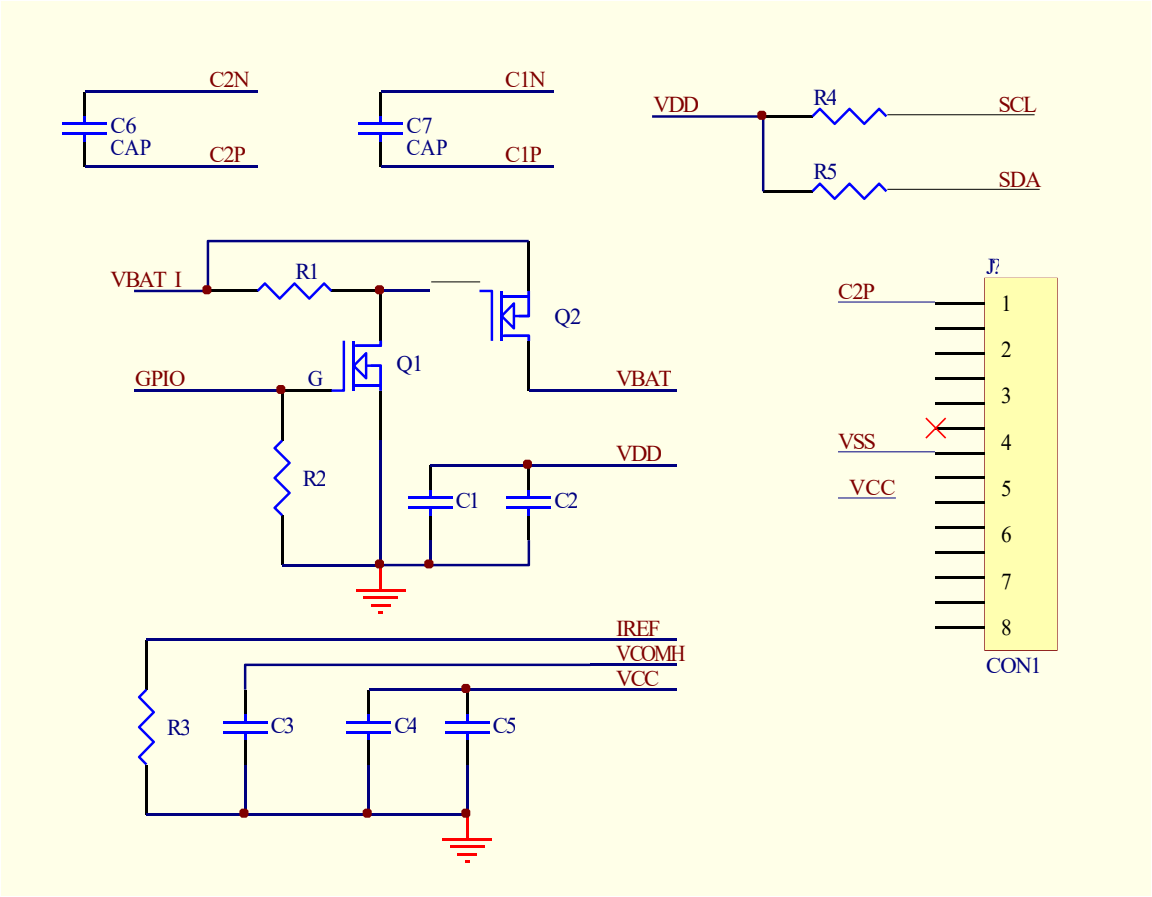
5.4 AC Characteristics

5.4.1 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	ns
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	us
t_R	Rise Time for data and clock pin	-	300	ns
t_F	Fall Time for data and clock pin	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3		us

* (V_{DD} -V_{SS} = 1.65V to 3.3V, Ta = 25°C)

5.4.2 I²C Interface with Internal Charge Pump



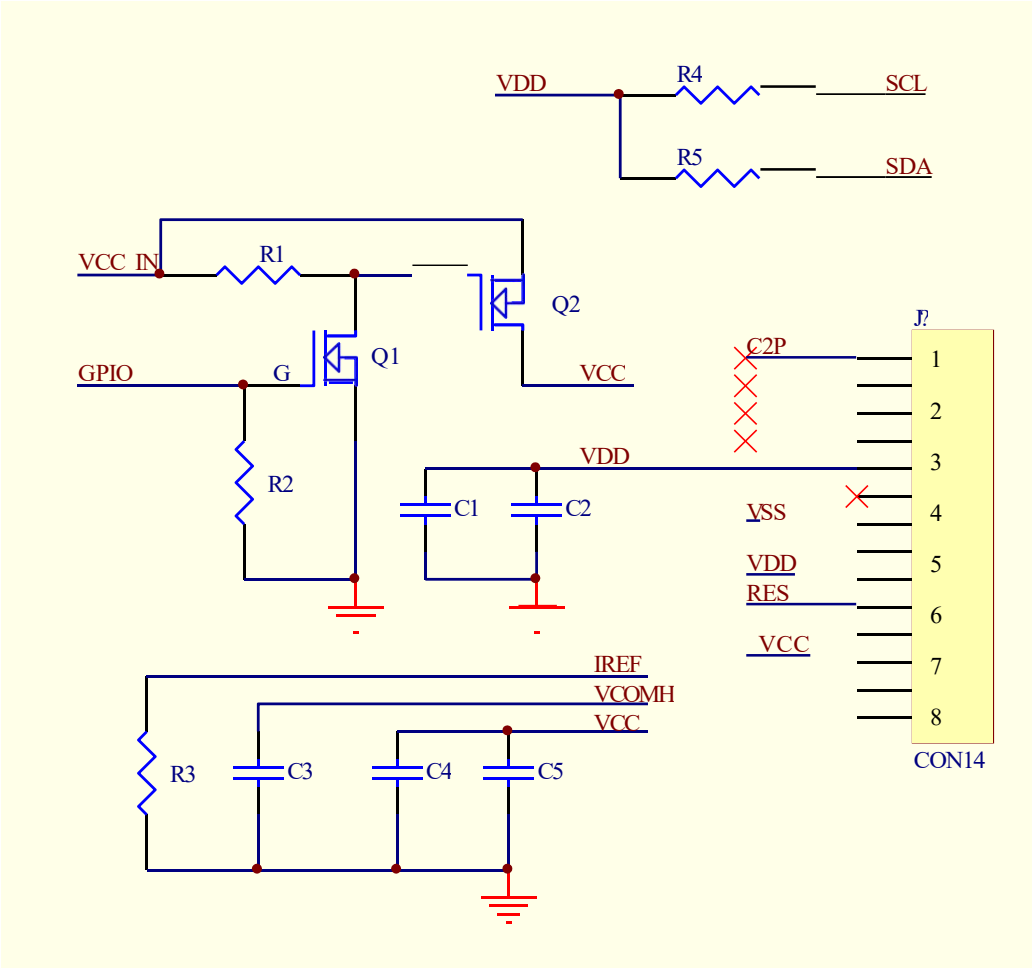
Recommended Components:

C1,: 0.1µF / 6.3V, X5R
C2: 4.7µF / 6.3V, X5R
C3: 2.2µF/ 16V, X7R
C4: 4.7µF / 16V, X7R
C5: 0.1µF / 16V, X7R
C6,C7: 1µF / 16V, X7R
R3: 560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1: 47kΩ
R4, R5: 4.7kΩ
Q1: FDN338P
Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.
VBAT_in: 3.5~4.2V

5.4.3 I²C Interface with External VCC



Recommended Components:

C1,: 0.1µF / 6.3V, X5R
C2: 4.7µF / 6.3V, X5R
C3: 2.2µF/ 16V, X7R
C4: 4.7µF / 16V, X7R
C5: 0.1µF / 16V, X7R
R3: 560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1: 47kΩ
R4, R5: 4.7kΩ
Q1: FDN338P
Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.
VCC_in: 7~9V

6 Functional Specification

6.1 Commands

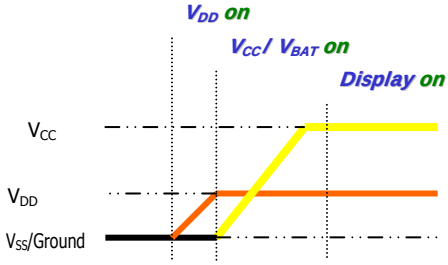
Refer to the Technical Manual for the SSD1316

6.2 Power down and Power up Sequence

To protect OEL paneland extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

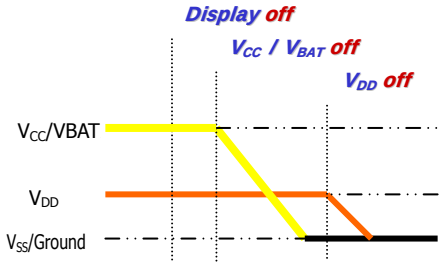
6.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC} /V_{BAT}
6. Delay 100ms (When V_{CC} is stable)
7. Send Display on command



6.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC} /V_{BAT}
3. Delay 100ms
4. (When V_{CC} /V_{BAT} is reach 0 and panel is completely discharges)
5. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} /V_{BAT} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{BAT}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} /V_{BAT} power down.

6.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 96 x 16 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

7 Power ON/OFF Timing Sequence

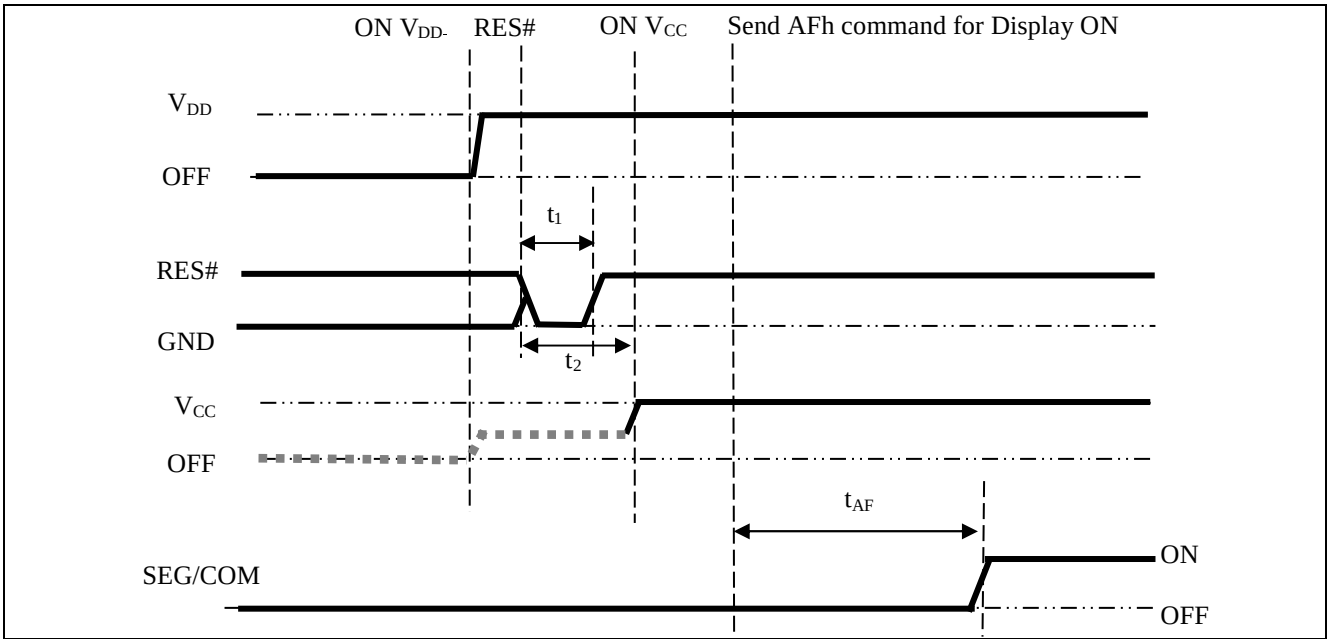
The following figures illustrate the recommended power ON and power OFF sequence of SSD1316 :

7.1 Power ON and OFF sequence with External VCC

Power ON sequence:

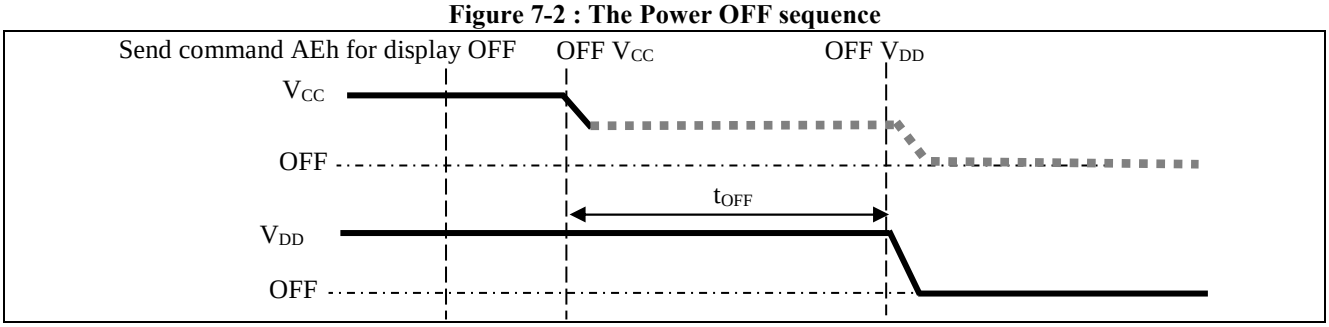
1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

Figure 7-1 : The Power ON sequence.



Power OFF sequence:

Figure 7-2 : The Power OFF sequence



Note:

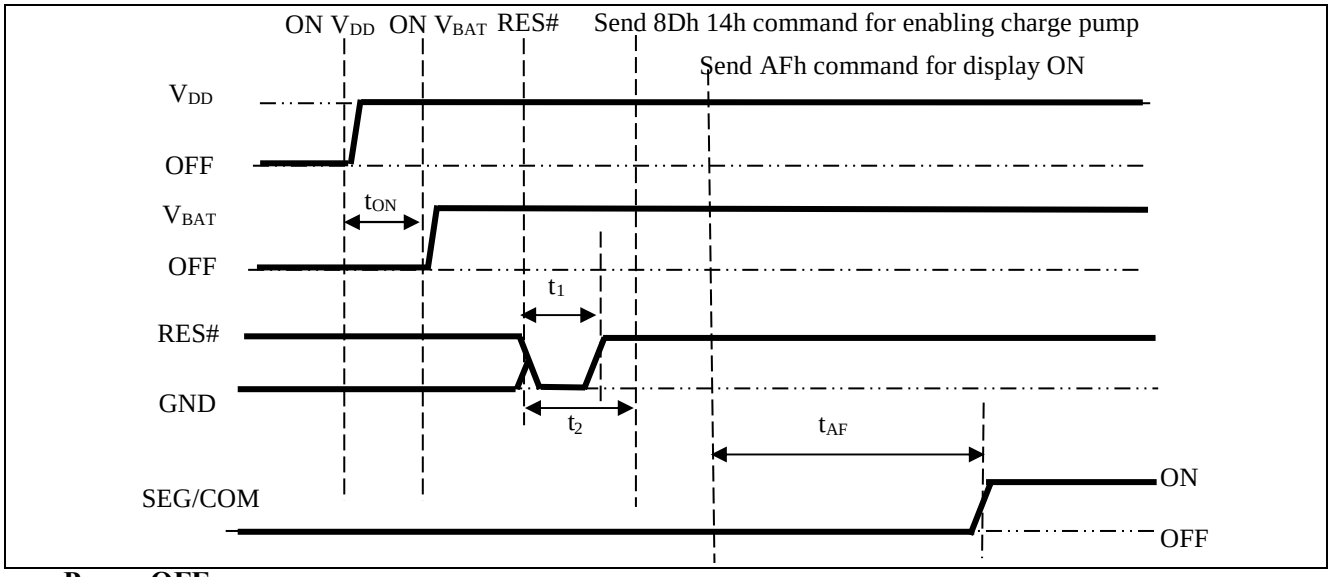
[1] Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-1 and Figure 7-2.
[2] V_{CC} should be kept float (i.e. disable) when it is OFF.
[3] Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.
[4] The register values are reset after t_1.
[5] V_{DD} should not be Power OFF before V_{CC} Power OFF.

7.2 Power ON and OFF sequence with Charge Pump Application

Power ON sequence:

1. Power ON V_{DD}
2. Wait for t_{ON}. Power ON V_{BAT}.(1), (2) (where Minimum t_{ON} = 0ms)
3. After V_{BAT} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) (3) and then HIGH (logic high).
4. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then input commands with below sequence:
   a. 8Dh 14h for enabling charge pump
   b. AFh for display ON
5. SEG/COM will be ON after 100ms(t_{AF}).

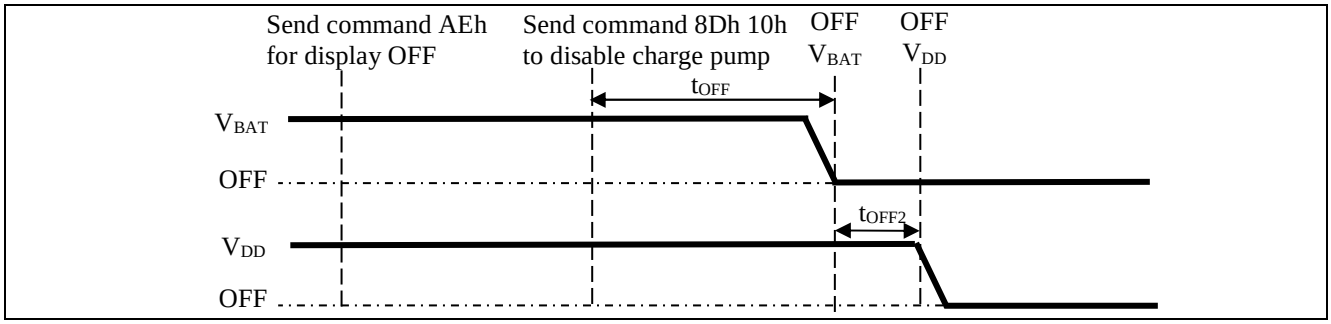
Figure 7-3 : The Power ON sequence with Charge Pump Application.



Power OFF sequence:

1. Send command AEh for display OFF
2. Send command 8Dh 10h to disable charge pump
3. Power OFF V_{BAT} after t_{OFF}.(1), (2) (Typical t_{OFF} =500ms)
4. Power OFF V_{DD} after t_{OFF2}. (where Minimum t_{OFF2} = 0ms (4), Typical t_{OFF2}=5ms)

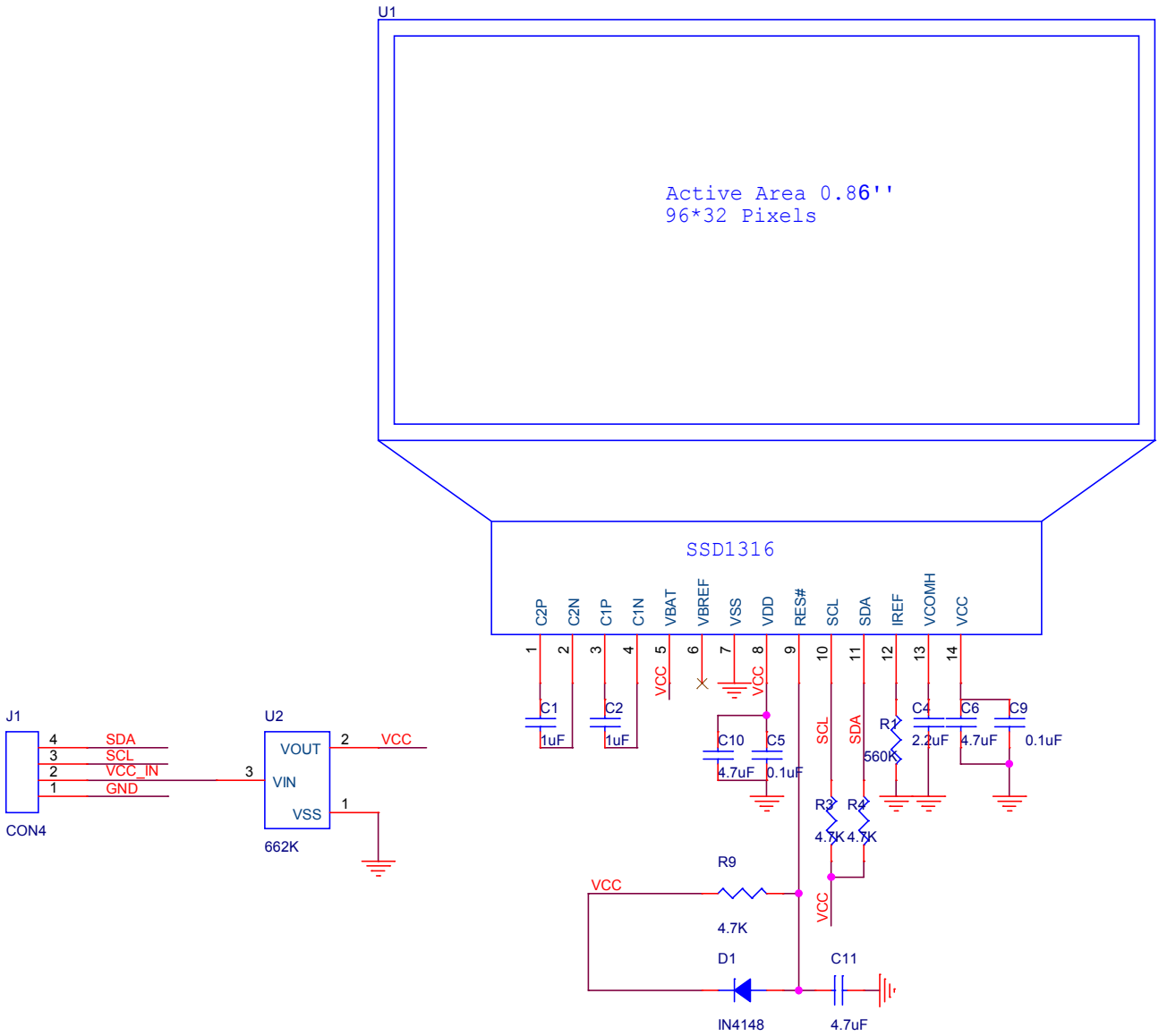
Figure 7-4 : The Power OFF sequence with Charge Pump Application.



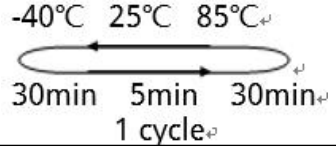
Note:

(1) V_{BAT} should be kept float (i.e. disable) when it is OFF.
(2) Power Pins (V_{DD} , V_{BAT}) can never be pulled to ground under any circumstance.
(3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{BAT} Power OFF

8 Module Schematic



9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85℃ 240hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40℃ 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 240hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 ℃ 240hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 120hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40℃/85℃ 24 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"