SONY

1.8 cm (Type 0.71) Active Matrix Color OLED Panel

ECX335AF-6

1. Description

The ECX335AF is a 1.8 cm (type 0.71) diagonal, 1920(RGB) × 1080 dots active matrix color OLED panel module using single crystal silicon transistors. This panel incorporates panel driver and logic driver, and realizes small size, light weight and high definition.

(Applications: View finders, head mounted displays, very small monitors etc.)

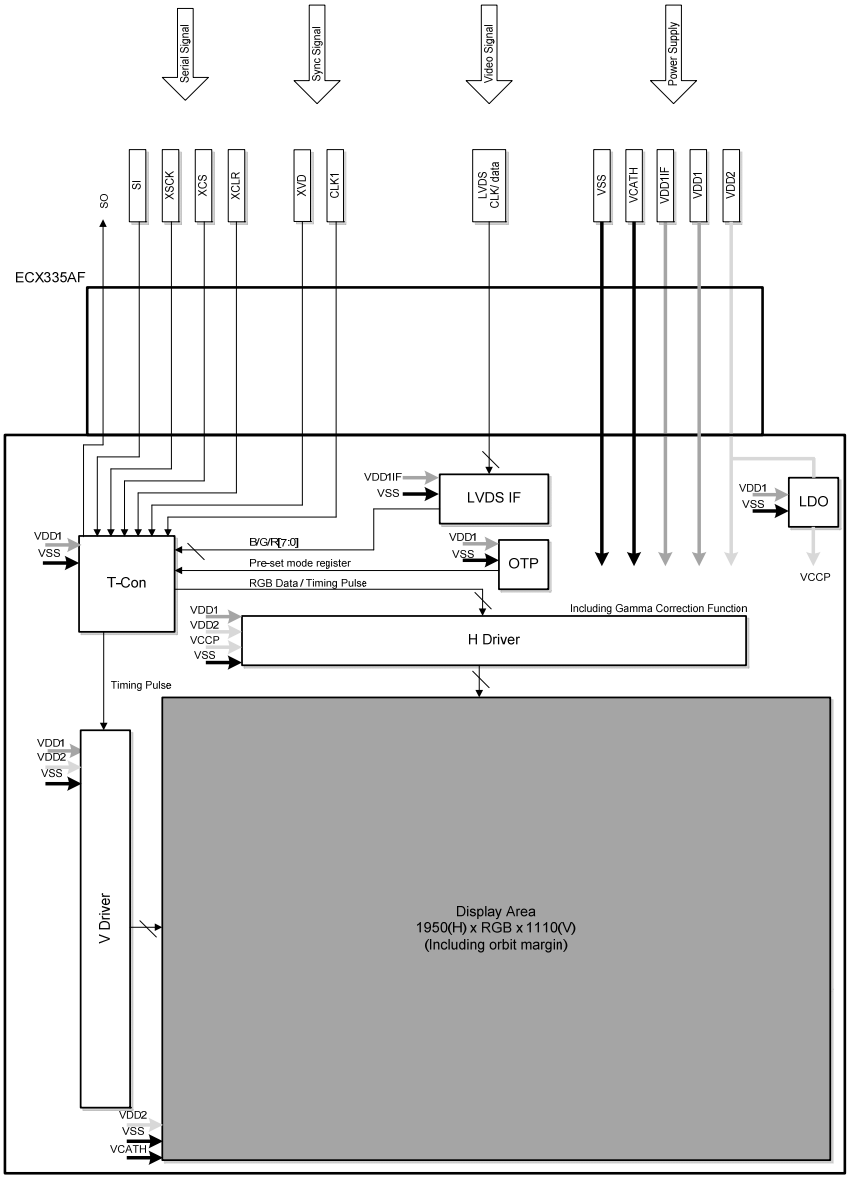
2. Features

- Small size high definition type 0.70 display dots: 1920 (RGB)×1080 = 6.22 M dots
- High contrast
- Wide color reproduction range
- High-speed response
- Thin type and light weight
- Power saving function
- Up/down and/or right/left inverse display function
- Orbit supported

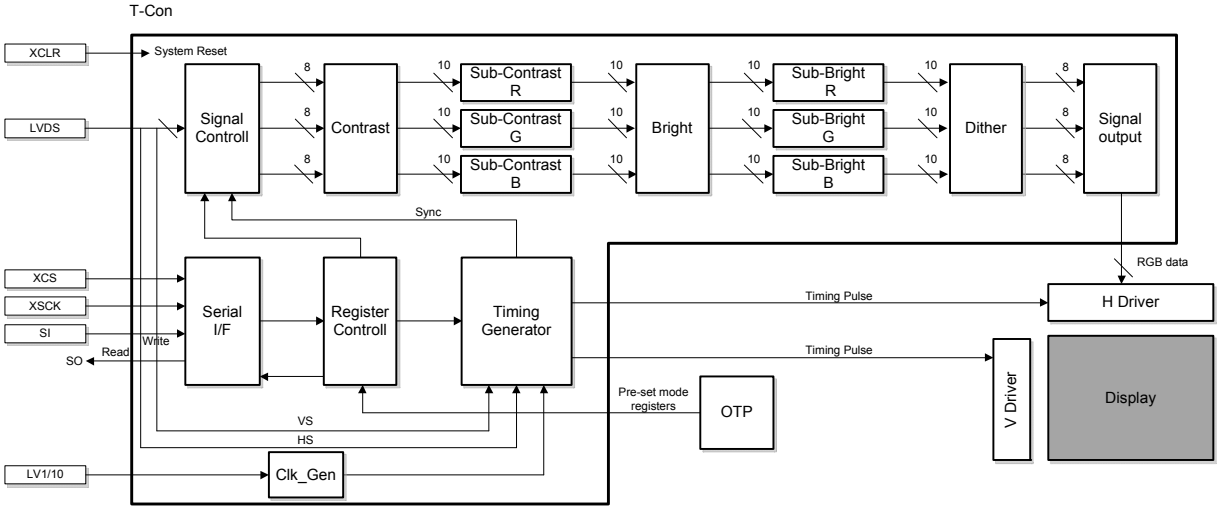
3. Element Structure

Active matrix color OLED display element with on-chip driver using single crystal silicon transistors

4. System Block Diagram

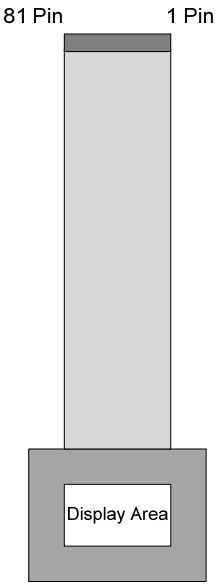


Details of “T-con”



5. Pin Description

5.1 Pin Assignment



5.2 Pin description (LVDS input)

Pin No. (FPC Side)	Symbol	Type	Description	Equivalent circuit
1	VCATH	Power Supply	EL cathode power supply	
2	VCATH	Power Supply	EL cathode power supply	
3	VCCP_O	Power Supply	VCCP power supply	※8
4	VCCP_I	Power Supply	VCCP power supply	
5	VCCP_I	Power Supply	VCCP power supply	
6	VDD2	Power Supply	10V power supply	
7	VDD2	Power Supply	10V power supply	
8	VSS	Power Supply	GND	
9	VSS	Power Supply	GND	
10	VSS	Power Supply	GND	
11	VSS	Power Supply	GND	
12	VDD1	Power Supply	1.8V power supply	
13	VDD1	Power Supply	1.8V power supply	
14	XCS	Input	Serial communication Chip select	※1
15	XSCK	Input	Serial communication Serial clock	※1
16	SI	Input	Serial communication Data input	※1
17	SO	Output	Serial communication Data output	※2

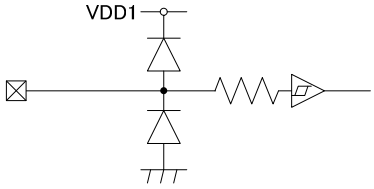
Pin No. (FPC Side)	Symbol	Type	Description	Equivalent circuit
18	PSCNT	Input	Power save communication enable Connect to GND	※1
19	XCLR	Input	System reset	※1
20	TEST	Output	Test pin (no connect)	※3
21	TEST	-	Test pin (connect to GND)	
22	TEST	Input	Test pin (connect to GND)	※4
23	TEST	Input	Test pin (connect to GND)	※5
24	TEST	Input	Test pin (connect to GND)	※1
25	TEST	Input / Output	Test pin (connect to GND)	※4
26	TEST	Output	Test pin（no connect）	※1
27	VDD1IF	Power Supply	1.8V power supply for LVDS	
28	VSSIF	Power Supply	GND for LVDS	
29	TEST	Input	Test pin (connect to GND)	※6
30	TEST	Input	Test pin (connect to GND)	※6
31	LV1A	Input	LVDS clock	※6
32	LV1B	Input	LVDS clock	※6
33	LV2A	Input	LVDS data input	※6
34	LV2B	Input	LVDS data input	※6
35	LV3A	Input	LVDS data input	※6
36	LV3B	Input	LVDS data input	※6
37	LV4A	Input	LVDS data input	※6
38	LV4B	Input	LVDS data input	※6
39	LV5A	Input	LVDS data input	※6
40	LV5B	Input	LVDS data input	※6
41	VDD1IF	Power Supply	1.8V power supply for LVDS	
42	VSSIF	Power Supply	GND for LVDS	
43	TEST	Input	Test pin (connect to GND)	※6
44	TEST	Input	Test pin (connect to GND)	※6
45	VSSIF	Power Supply	GND for LVDS	
46	VDD1IF	Power Supply	1.8V power supply for LVDS	
47	LV9A	Input	LVDS data input	※6
48	LV9B	Input	LVDS data input	※6
49	LV8A	Input	LVDS data input	※6
50	LV8B	Input	LVDS data input	※6
51	LV7A	Input	LVDS data input	※6
52	LV7B	Input	LVDS data input	※6
53	LV6A	Input	LVDS data input	※6

Pin No. (FPC Side)	Symbol	Type	Description	Equivalent circuit
54	LV6B	Input	LVDS data input	※6
55	LV10A	Input	LVDS clock	※6
56	LV10B	Input	LVDS clock	※6
57	TEST	Input	Test pin (connect to GND)	※6
58	TEST	Input	Test pin (connect to GND)	※6
59	VSSIF	Power Supply	GND for LVDS	
60	VDD1IF	Power Supply	1.8V power supply for LVDS	
61	TEST	Output	Test pin (no connect)	※1
62	IFSW	Input	Interface select pin (connect to GND)	※1
63	VDD1	Power Supply	1.8V power supply	
64	VDD1	Power Supply	1.8V power supply	
65	VSS	Power Supply	GND	
66	VSS	Power Supply	GND	
67	TEST	Input	Test pin (connect to GND)	※7
68	VCAL	Output	Output of temperature sensing circuit	※8
69	R_IB	Input / Output	Bias current adjustment resistance connect pin	※8
70	VREF	Output	VREF voltage	※8
71	VG255	Output	Gamma top voltage	※8
72	VG0	Output	Gamma bottom voltage	※8
73	VOFS	Output	Vofs voltage	※8
74	VSS	Power Supply	GND	
75	VSS	Power Supply	GND	
76	VDD2	Power Supply	10V power supply	
77	VDD2	Power Supply	10V power supply	
78	VCCP_I	Power Supply	VCCP power supply	
79	VCCP_I	Power Supply	VCCP power supply	
80	VCATH	Power Supply	EL cathode power supply	
81	VCATH	Power Supply	EL cathode power supply	

5.3 Equivalent Circuits

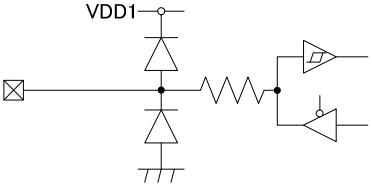
※1

14:XCS
15:XSCK
16:SI
18:PSCNT
19:XCLR
24:CLK1
62:IFSW



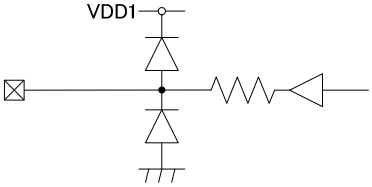
※2

17:SO



※3

20:TEST



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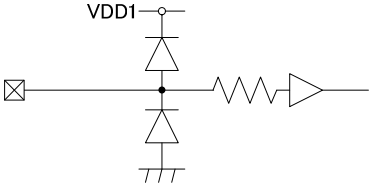
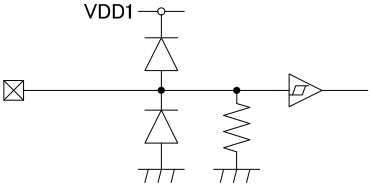
22:XVD
25:TEST
26:TEST
61:TEST



※5

23:TEST



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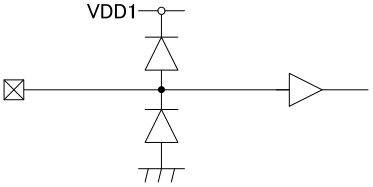
29–40:data
43–44:CLKA CLKB
47–58:data



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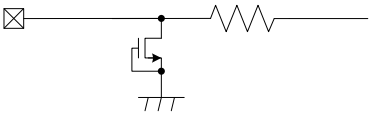
67:TEST



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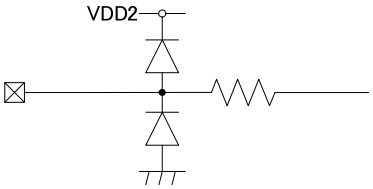
3:VCCP_O
68:VCAL
69:R_IB
70:VREF
71:VG255
72:VG0
73:VOFS



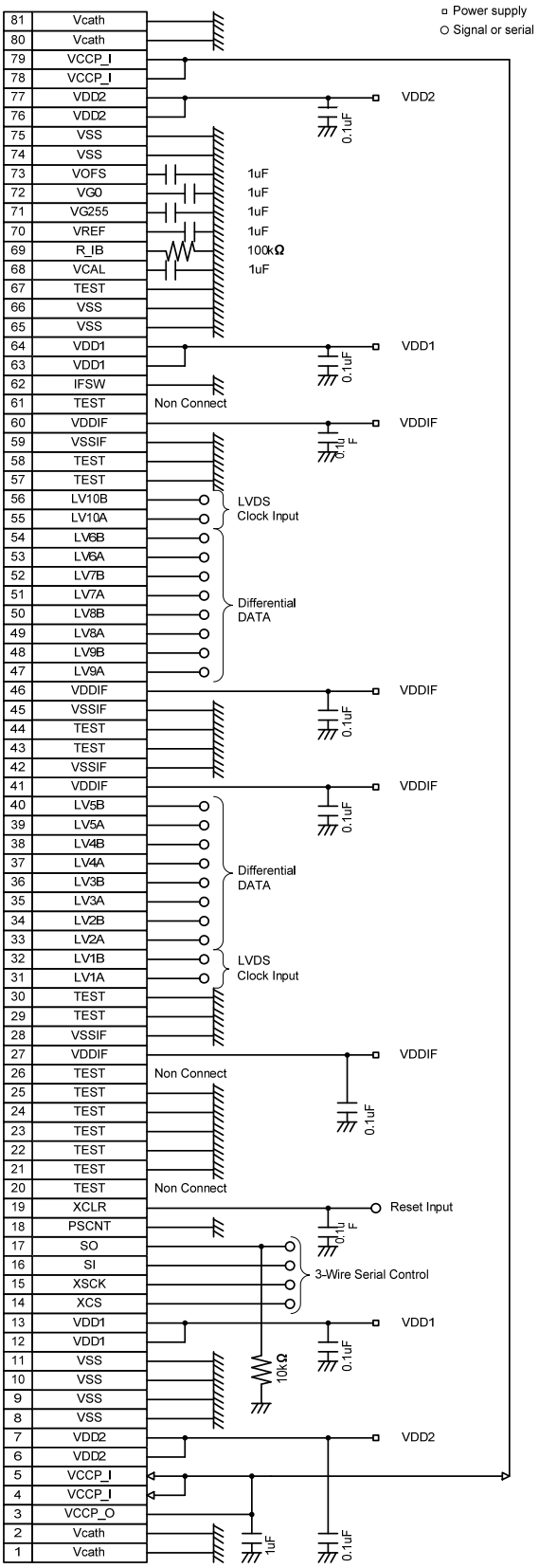
5.4 Peripheral Circuit

Regarding power supply capacitor connections, mount an approximately 2.2 μF to 10 μF capacitor for each power supply. Insufficient capacitance may affect the picture quality.

External capacitor characteristic : X5R or Class B

Notes

Regarding power supply connections, mount an appropriate capacitor as close to the connector as possible.
Insufficient capacitance may affect the picture quality



※This circuit is a typical example illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of the circuit.

6. Absolute Maximum Ratings

Item	Symbol	Min.	Maximum Ratings	Unit
1.8V power supply	VDD1	-0.3	2.0	V
1.8V power supply (IF)	VDD1IF	-0.3	2.5	V
10 V power supply	VDD2	-0.3	12.0	V
EL cathode voltage	Vcath	-0.3	0.3	V
Logic input voltage ※	Vi	-0.3	VDD1+0.3	V
IF input voltage ※※	ViIF	-0.3	VDD1IF+0.3	V
Storage temperature	Tpnl	-30	+80	°C

※ Pin no. 14,15,16,18,19,22,23,24 & 62

※※ Pin no. 29 to 40,43,44 & 47 to 58

7. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
1.8V power supply	VDD1	1.62	1.8	1.98	V
1.8V power supply (IF)	VDD1IF	1.62	1.8	1.98	V
10 V power supply	VDD2	9.7	10.0	10.3	V
EL cathode voltage	Vcath	-0.3	0	0.3	V
Operating temperature range	Tpnl	0		70	°C

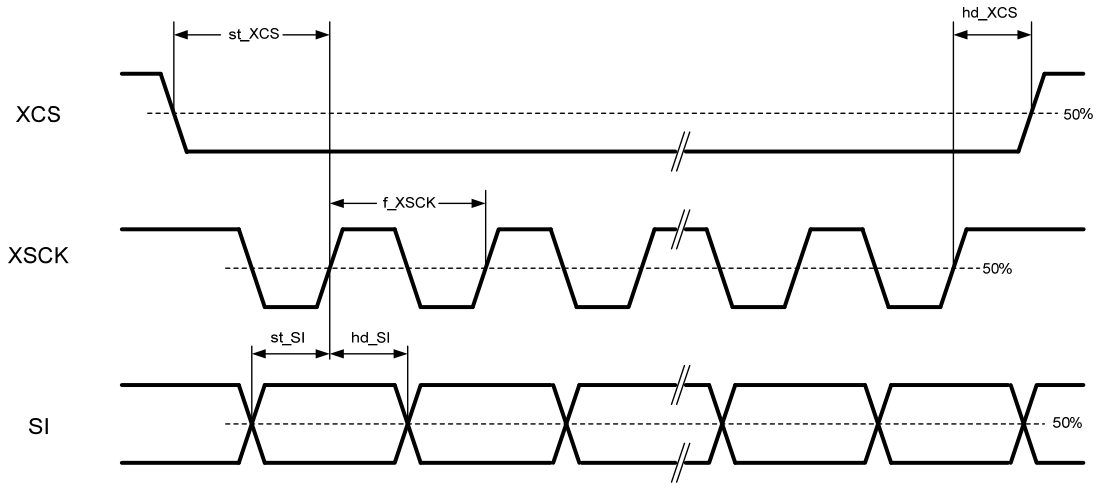
8. Electrical Characteristics

8.1. DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	VIH		0.7VDD1		VDD1	V
Low-level input voltage	VIL		0		0.3VDD1	V
Logic High -level Output voltage	VOH		VDD1 - 0.5			V
Logic Low -level Output voltage	VOL				0.5	V

8.2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
XSCK frequency	f_XSCK			0.8	2.5	MHz
XCS setup time	st_XCS		0.4			µs
XCS hold time	hd_XCS		0.2			µs
SI setup time	st_SI		0.2			µs
SI hold time	hd_SI		0.2			µs



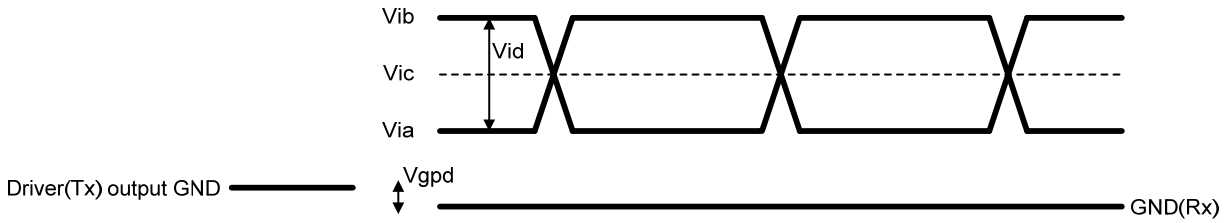
8.3. LVDS I/F Specifications

◆Resolution :Full-HD 1920x1080
◆Frame Rate :60Hz
◆Gradation :8bit
◆Number of pairs :Clk: 2pairs, Data:8pairs

8.4. DC Characteristics

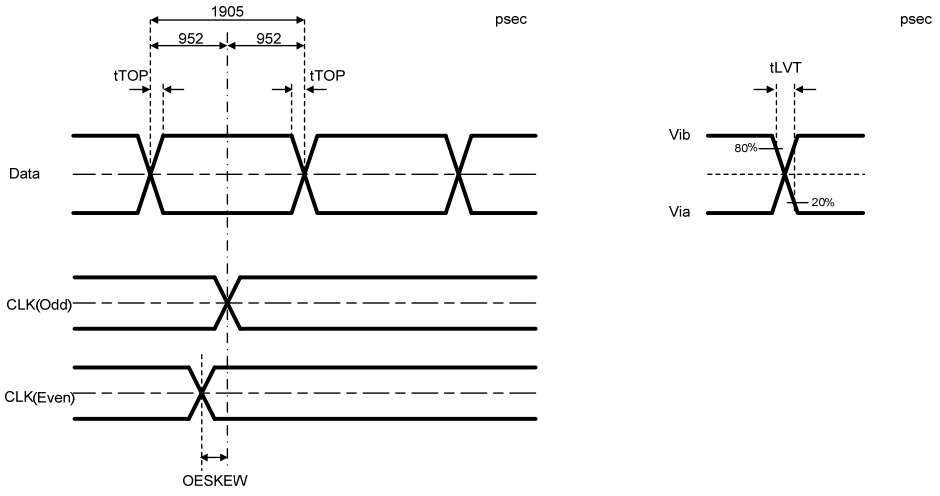
Item	Symbol	Min.	Typ.	Max.	Unit
Voltage range (*)	Vi	890		1550	mV
Common Mode Voltage	Vic	1040		1400	mV
Each DATA-DATA and DATA-CLK Vic difference	⊿Vic			35	mV
Differential Input Voltage	Vid	130		300	mV
Each DATA-DATA and DATA-CLK Vid difference	⊿Vid			35	mV
Driver-receiver ground potential difference	Vgpd			50	mV

(*)Assumed driver output differential voltage =180mV



8.5. LVDS AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Tx Timing Budget	tTOP	-250	0	250	psec
Tx tLVT	tLVT	300	500	600	psec
Odd and Even clock skew	OESKEW	0		500	psec



8.6 Power Consumption

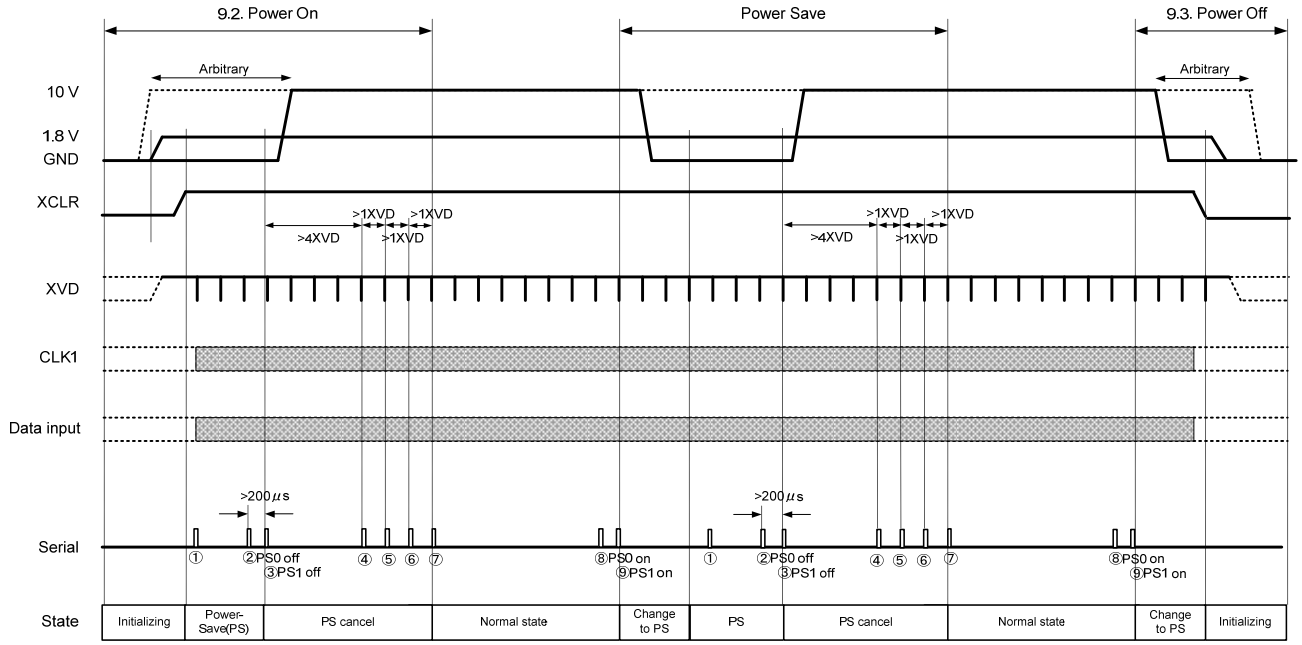
Item	Symbol	Condition	Typ. (*)				Unit
			200	120	90	Standby	cd/m^2
VDD1 power consumption	PDD1	VDD1=1.8V VDD2=10V LVDS input Tpnl=40°C	30	30	30	0.4	mW
VDD1IF power consumption	PDD1IF		80	80	80	0	mW
VDD2 power consumption	PDD2		440	360	330	0	mW
Total power consumption	PDDTTL		550	470	440	0.4	mW

*: All white raster display, Clock frequency = 148.5MHz, Frame rate = 60Hz

9. Power Supply Sequence

To avoid panel breakdown caused by excessive current flow into the internal circuit, power supply sequence written below should be kept.

9.1 Sequence Diagram



	Data								
Address	Serial Setting①	Serial Setting②	Serial Setting③	Serial Setting④	Serial Setting⑤	Serial Setting⑥	Serial Setting⑦	Serial Setting⑧	Serial Setting⑨
0x00		0x0F						0x0E	
0x01			0x01						0x00
0x02	0x40								
0x03	0xA0						0x20		
0x04	0x5F			0x3F					
0x6D	0x04					0x00			
0x6F	0x03					0x00			
0x71	0x4E				0x46	0x00			
0x72	0x4E				0x46	0x00			

9.2. Power On Sequence

1. Set XCLR to low and turn on 1.8V power supply.
2. After completion of 1.8 V power supply rising, set XCLR to high, then the panel changes to the power-saving mode.
3. Perform the serial setting ①
4. Perform power-save 0 (PS0) off serial setting ②, then perform power-save 1 (PS1) off serial setting ③ at an interval of > 200μs.

5. After serial setting ③ completion, perform the serial setting ④ at an interval of > 4XVD.

6. After serial setting ④ completion, perform the serial setting ⑤ at an interval of > 1XVD.

7. After serial setting ⑤ completion, perform the serial setting ⑥ at an interval of > 1XVD.

8. After serial setting ⑥ completion, perform the serial setting ⑦ within V-blanking period just after 1V period from serial setting ⑥.

*Complete turning on of 10V power supply within 3 XVD periods after power saving mode off setting ③, while the order of turning on of 1.8V and 10V power supply is not restricted.

9.3. Power Off Sequence

1. Perform PS0 on and PS1 on serial setting to enter power-saving mode.

2. After power-saving mode starts, set XCLR to low and turn off 1.8V and 10V power supplies.

*Turning off of 1.8V and 10V power supplies should be done after completion of setting XCLR to low, while the order of turning off of 1.8V and 10V power supply is not restricted.

10. Description of Function

10.1. Serial Communication

10.1.1. Register Map

	Addr.	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Initial
0	+0x00	RGB_YCB	YCB_DEC	*	*	DWN	RGT	MCLKPOL	PS0	0E
1	+0x01	VCAL_MON	CALSEL[1:0]		YCB_P	*	*	*	PS1	00
2	+0x02	*	*	*	ORBIT_H[4:0]					00
3	+0x03	*	*	*	ORBIT_V[4:0]					00
4	+0x04	*	*	*	*	*	*	*	*	1F
5	+0x05	*	*	*	*	DITHERON	LUMINANCE[2:0]			00
6	+0x06	*	*	*	*	*	*	*	*	00
7	+0x07	*	*	*	*	*	*	*	*	00
8	+0x08	*	*	*	*	*	OTPCALDAC_REGDIS	*	OTPDG_REGDIS	00
9	+0x09	*	*	*	*	*	*	*	*	56
A	+0x0A	*	*	*	*	*	*	*	*	00
B	+0x0B	*	*	*	*	*	*	*	*	00
C	+0x0C	*	*	*	*	*	*	*	*	00
D	+0x0D	*	*	*	*	*	*	*	*	00
E	+0x0E	*	*	*	*	*	*	*	*	00
F	+0x0F	*	*	*	*	*	*	*	*	00
10	+0x10	*	*	*	*	*	*	*	*	00
11	+0x11	*	*	*	*	*	*	*	*	00
12	+0x12	*	*	*	*	*	*	*	*	00
13	+0x13	*	*	*	*	*	*	*	*	00
14	+0x14	CONT[7:0]								00
15	+0x15	CONT[8]	RCONT[6:0]							C0
16	+0x16	*	GCONT[6:0]							40
17	+0x17	*	BCONT[6:0]							40
18	+0x18	BRT[7:0]								80
19	+0x19	*	RBRT[6:0]							40
1A	+0x1A	*	GBRT[6:0]							40
1B	+0x1B	*	BBRT[6:0]							40
1C	+0x1C	*	*	*	*	*	*	*	*	10
1D	+0x1D	CALDAC[7:0]								80
1E	+0x1E	*	*	*	*	*	*	*	*	40
1F	+0x1F	*	*	*	*	*	*	*	*	10
20	+0x20	H_ACT_U[7:0]								60
21	+0x21	H_ACT_U[8]	V_ACT_D[10:8]			*	H_ACT_D[10:8]			44
22	+0x22	H_ACT_D[7:0]								20
23	+0x23	V_ACT_U[7:0]								29
24	+0x24	V_ACT_D[7:0]								61
25	+0x25	*	*	*	*	*	*	*	*	00
26	+0x26	*	*	*	*	*	*	*	*	04
27	+0x27	*	*	*	*	*	*	*	*	4C
28	+0x28	*	DE_D[10:8]			*	DE_U[10:8]			40
29	+0x29	DE_U[7:0]								58
2A	+0x2A	DE_D[7:0]								28
2B	+0x2B	*	*	*	*	*	*	*	*	04
2C	+0x2C	*	*	*	*	*	*	*	*	65
2D	+0x2D	*	WSST1_D[10:8]			*	WSST1_U[10:8]			00
2E	+0x2E	WSST1_U[7:0]								18
2F	+0x2F	WSST1_D[7:0]								19
30	+0x30	*	WSST2_D[10:8]			*	WSST2_U[10:8]			44
31	+0x31	WSST2_U[7:0]								0D
32	+0x32	WSST2_D[7:0]								0E

33	+0x33	*	*	*	*	*	*	*	*	80
34	+0x34	*	*	*	*	*	*	*	*	00
35	+0x35	*	*	*	*	*	*	*	*	24
36	+0x36	WSEN1_U[7:0]								DD
37	+0x37	*	*	*	*	*	*	*	WSEN1_U[8]	00
38	+0x38	WSEN1_W[7:0]								01
39	+0x39	*	*	*	*	*	WSEN2_U[10:8]			04
3A	+0x3A	WSEN2_U[7:0]								35
3B	+0x3B	WSEN2_W[7:0]								07
3C	+0x3C	WSEN3_U[7:0]								5D
3D	+0x3D	WSEN3_W[7:0]								0A
3E	+0x3E	DSEN_U[7:0]								B6
3F	+0x3F	*	*	*	DESN_U[8]	*	DSEN_W[10:8]			03
40	+0x40	DSEN_W[7:0]								8D
41	+0x41	*	*	VCK_W[9:8]		*	*	VCK_U[9:8]		00
42	+0x42	VCK_U[7:0]								01
43	+0x43	VCK_W[7:0]								7B
44	+0x44	*	*	*	*	*	*	SGSELREF_U[9:8]		00
45	+0x45	SIGSELREF_U[7:0]								17
46	+0x46	SIGSELREF_W[7:0]								76
47	+0x47	*	*	*	*	SIGSELOFS_U[3:0]				00
48	+0x48	SIGSELOFS_W[7:0]								76
49	+0x49	*	*	SIGSEL_W[9:8]		SIGSEL_U[3:0]				00
4A	+0x4A	SIGSEL_W[7:0]								5A
4B	+0x4B	*	*	*	*	*	*	SELREF_U[9:8]		00
4C	+0x4C	SELREF_U[7:0]								0A
4D	+0x4D	SELREF_W[7:0]								5D
4E	+0x4E	SELOFS_U[7:0]								0A
4F	+0x4F	SELOFS_W[7:0]								5D
50	+0x50	*	*	SEL_W[9:8]		*	*	SEL_U[9:8]		00
51	+0x51	SEL_U[7:0]								0A
52	+0x52	SEL_W[7:0]								41
53	+0x53	*	*	*	*	*	*	*	*	00
54	+0x54	*	*	*	*	*	*	*	*	51
55	+0x55	*	*	*	*	*	*	*	*	0A
56	+0x56	*	*	*	*	*	*	*	*	38
57	+0x57	*	AZEN_D[10:8]			*	*	*	AZEN_U[8]	40
58	+0x58	AZEN_U[7:0]								62
59	+0x59	AZEN_D[7:0]								2F
5A	+0x5A	*	*	*	*	*	*	*	*	00
5B	+0x5B	*	*	*	*	*	*	*	*	76
5C	+0x5C	*	*	*	*	*	*	*	*	00
5D	+0x5D	*	*	*	*	*	*	*	*	01
5E	+0x5E	*	*	*	*	*	*	*	*	0B
5F	+0x5F	*	*	*	*	*	*	*	*	00
60	+0x60	*	*	*	*	*	*	*	*	01
61	+0x61	*	*	*	*	*	*	*	*	A0
62	+0x62	*	*	*	*	*	*	*	*	00
63	+0x63	*	*	*	*	*	*	*	*	02
64	+0x64	*	*	*	*	*	*	*	*	0F
65	+0x65	*	*	*	*	*	*	*	*	00
66	+0x66	*	*	*	*	*	*	*	*	00
67	+0x67	*	*	*	*	*	*	*	*	00
68	+0x68	*	*	*	*	*	*	*	*	00
69	+0x69	*	*	*	*	*	*	*	*	00
6A	+0x6A	*	*	*	*	*	*	*	*	00
6B	+0x6B	*	*	*	*	*	*	*	*	00
6C	+0x6C	*	*	*	*	*	*	*	*	00

6D	+0x6D	120MODE	*	*	*	*	*	*	*	00
6E	+0x6E	*	*	*	*	*	*	*	*	E8
6F	+0x6F	*	*	*	*	*	*	*	*	00
70	+0x70	*	*	*	*	*	*	*	*	00
71	+0x71	*	*	*	*	*	*	*	*	00
72	+0x72	*	*	*	*	*	*	*	*	00
73	+0x73	*	*	*	*	*	*	*	*	00
74	+0x74	*	*	*	*	*	*	*	*	00
75	+0x75	*	*	*	*	*	*	*	*	00
76	+0x76	*	*	*	*	*	*	*	*	00
77	+0x77	*	*	*	*	*	*	*	*	00
78	+0x78	*	*	*	*	*	*	*	*	00
79	+0x79	*	*	*	*	*	*	*	*	00
7A	+0x7A	*	*	*	*	*	*	*	*	00
7B	+0x7B	*	*	*	*	*	*	*	*	00
7C	+0x7C	*	*	*	*	*	*	*	*	00
7D	+0x7D	*	*	*	*	*	*	*	*	30
7E	+0x7E	*	*	*	*	*	*	*	*	00
7F	+0x7F	*	*	*	*	*	*	*	*	00
80	+0x80	*	*	*	*	*	*	*	RD_ON	00
81	+0x81	RD_ADDR[7:0]								00

* Setting values are separately presented.

10.1.2. Description of Register

Register	Bits	V sync	Function	Related Items
PS0	1		Power save mode 0:Power save on 1:Power save off	9.2 9.3
MCLKPOL	1		MCLK polarity 0: Negative 1: Positive	—
RGT	1		Selection of rightward / leftward scan	10.4
DWN	1		Selection of upward / down ward scan	10.4
YCB_DEC	1		Selection of YCbCr / YPbPr conversion	10.2
RGB_YCB	1		Selection of RGB / YCbCr (YPbPr) format	10.2
PS1	1		IF block output control 0: off (PS1 on) 1: output (PS1 off)	9.2 9.2
YCB_P	1		Selection of YCbCr (YPbPr) input pattern	10.2
CALSEL	2		VCAL output selection	10.5
VCAL_MON	1		Temperature sensing circuit monitoring on / off	10.5
ORBIT_H	5	○	Horizontal orbit adjustment	10.10.1
ORBIT_V	5	○	Vertical orbit adjustment	10.10.2
LUMINANCE	3		Luminance and white chromaticity preset mode selection	10.6
DITHERON	1		Dithering On/Off	10.9
OTPDG_REGDIS	1		White chromaticity preset mode on / off	10.6
OTPCALDAC_REGDIS	1		Luminance preset mode on / off	10.6
CONT	9		Contrast adjustment	10.8.1
RCONT	7		R sub-contrast adjustment	10.8.1
GCONT	7		G sub-contrast adjustment	10.8.1
BCONT	7		B sub-contrast adjustment	10.8.1
BRT	8		Brightness adjustment	10.8.2
RBRT	7		R sub-brightness adjustment	10.8.2
GBRT	7		G sub-brightness adjustment	10.8.2
BBRT	7		B sub-brightness adjustment	10.8.2
CALDAC	8		Manual luminance adjustment	10.7
H_ACT_U	9		Timing setting register (setting value separately presented)	10.3
H_ACT_D	11		Timing setting register (setting value separately presented)	10.3
V_ACT_U	8		Timing setting register (setting value separately presented)	10.3
V_ACT_D	11		Timing setting register (setting value separately presented)	10.3
DE_U	11		Timing setting register (setting value separately presented)	10.3
DE_D	11		Timing setting register (setting value separately presented)	10.3
WSST1_U	11		Timing setting register (setting value separately presented)	10.3
WSST1_D	11		Timing setting register (setting value separately presented)	10.3
WSST2_U	11		Timing setting register (setting value separately presented)	10.3

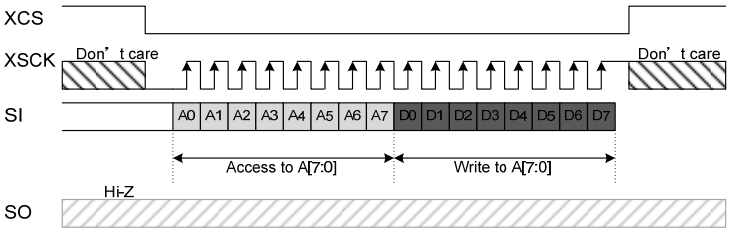
Register	Bits	V sync	Function	Related Items
WSST2_D	11		Timing setting register (setting value separately presented)	10.3
WSEN1_U	9		Timing setting register (setting value separately presented)	10.3
WSEN1_W	8		Timing setting register (setting value separately presented)	10.3
WSEN2_U	11		Timing setting register (setting value separately presented)	10.3
WSEN2_W	8		Timing setting register (setting value separately presented)	10.3
WSEN3_U	8		Timing setting register (setting value separately presented)	10.3
WSEN3_W	8		Timing setting register (setting value separately presented)	10.3
DSEN_U	9		Timing setting register (setting value separately presented)	10.3
DSEN_W	11		Timing setting register (setting value separately presented)	10.3
VCK_U	10		Timing setting register (setting value separately presented)	10.3
VCK_W	10		Timing setting register (setting value separately presented)	10.3
SIGSELREF_U	10		Timing setting register (setting value separately presented)	10.3
SIGSELREF_W	8		Timing setting register (setting value separately presented)	10.3
SIGSELOFS_U	4		Timing setting register (setting value separately presented)	10.3
SIGSELOFS_W	8		Timing setting register (setting value separately presented)	10.3
SIGSEL_U	4		Timing setting register (setting value separately presented)	10.3
SIGSEL_W	10		Timing setting register (setting value separately presented)	10.3
SELREF_U	10		Timing setting register (setting value separately presented)	10.3
SELREF_W	8		Timing setting register (setting value separately presented)	10.3
SELOFS_U	8		Timing setting register (setting value separately presented)	10.3
SELOFS_W	8		Timing setting register (setting value separately presented)	10.3
SEL_U	10		Timing setting register (setting value separately presented)	10.3
SEL_W	10		Timing setting register (setting value separately presented)	10.3
AZEN_U	9		Timing setting register (setting value separately presented)	10.3
AZEN_D	11		Timing setting register (setting value separately presented)	10.3
RD_ON	1		Register read on / off	10.1.4
RD_ADDR	8		Register read address setting	10.1.4

10.1.3. Serial I/F Write Access

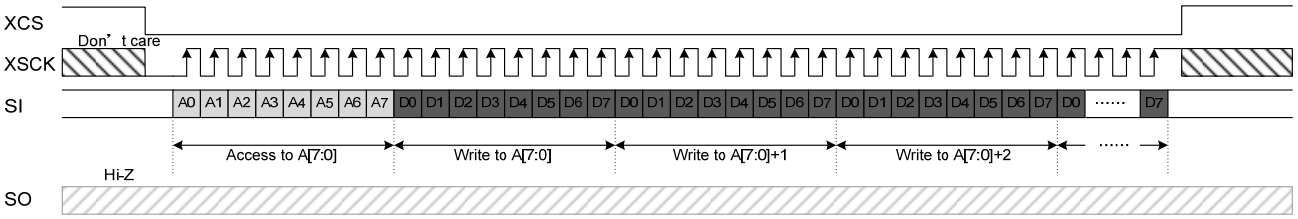
Serial communication of normal / burst transfer, LSB first is supported for write operation.

Input the address of the objective register from SI pin (#16), then input the data to the address.

The timing of write access is shown below.



Write Access Normal Transfer (LSB First)



Write Access Burst Transfer (LSB First)

10.1.4 Serial I/F Read Access

Serial communication of normal / burst transfer, LSB first is supported for read operation.

◆Register Settings

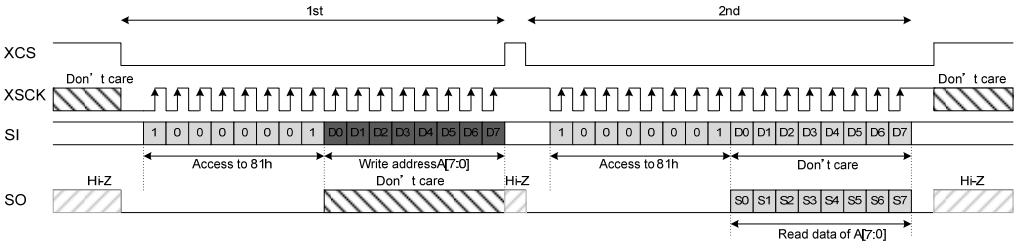
Address	Register name	Bits	Function
0x80	RD_ON	1	Register read on / off 0: Off (default) 1: On
0x81	RD_ADDR	8	Register read address setting

Set RD_ON to 1, and then perform 2 times serial communication.

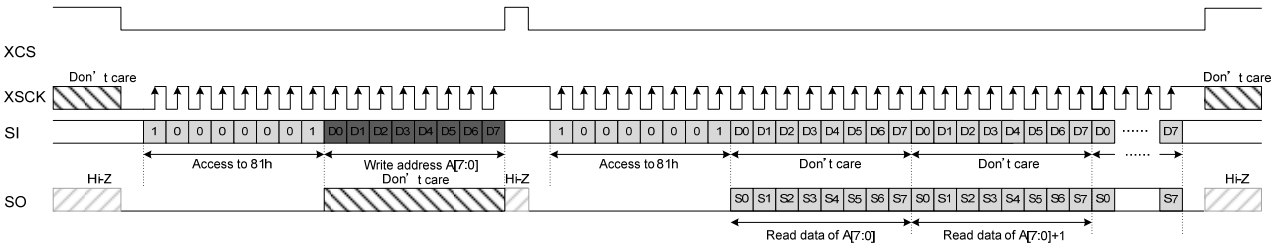
1st: Write the address of the objective register to RD_ADDR.

2nd: Read the data of the objective register from SO pin (#17) after accessing to the RD_ADDR.

The timing of read access is shown below.



Read Access Normal Transfer(LSB First)



Read Access Burst Transfer (LSB First)

10.2. Video Signal Transfer Format

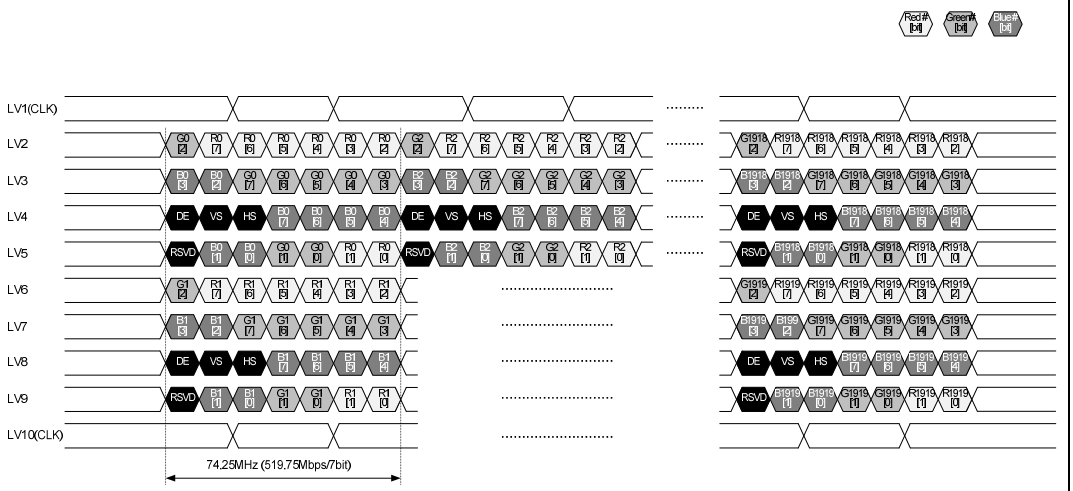
Set the registers appropriately for the video signal transfer format according to the table below.

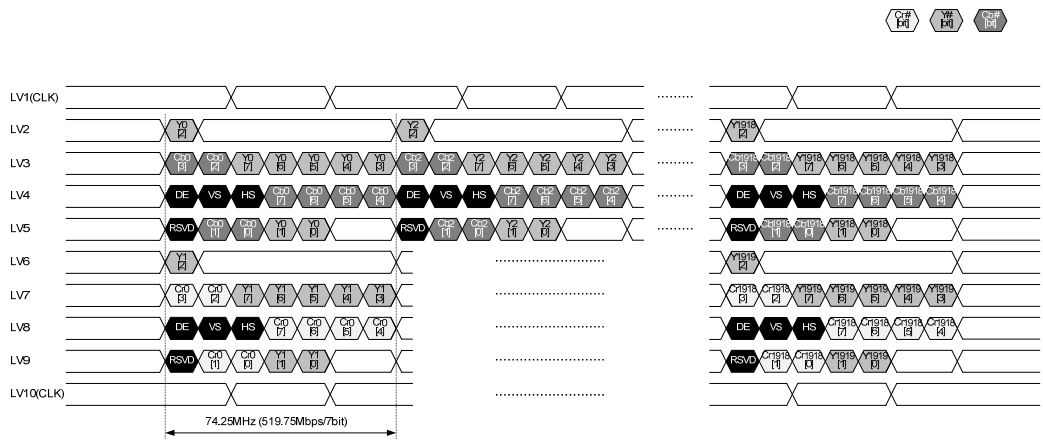
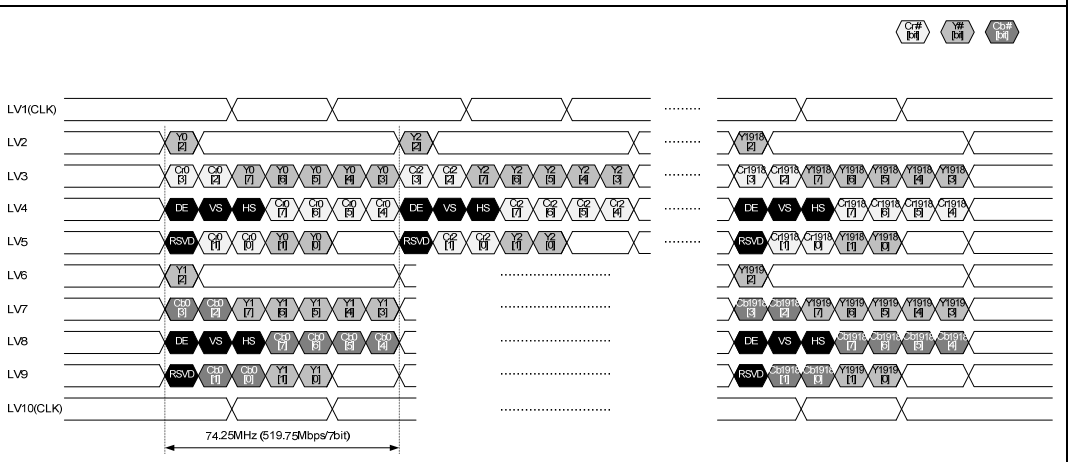
◆Register Settings

Address	Register name	Bits	Function
0x00	RGB_YCB	1	Selection of RGB / YCbCr (YPbPr) format 0: RGB (default) 1: YCbCr and YPbPr
0x00	YCB_DEC	1	Selection of YCbCr / YPbPr conversion 0: YCbCr (BT. 601) (default) 1: YPbPr (BT. 709)
0x01	YCB_P	1	Selection of YCbCr (YPbPr) input pattern 0: Cb and Pb first (default) 1: Cr and Pr first

◆Register settings for each video signal transfer formats when YCB_DEC=0.

*Cb and Cr are replaced by Pb and Pr respectively when YCB_DEC=1.

Register settings		Video signal transfer format
RGB_YCB	YCB_P	
0	—	

Register settings		Video signal transfer format
RGB_YCB	YCB_P	
1	0	
	1	

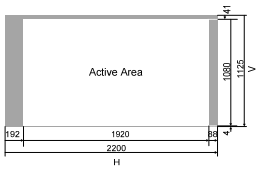
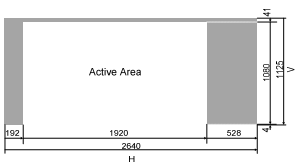
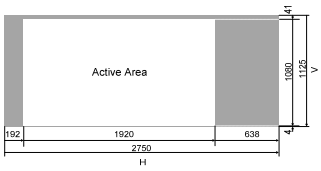
10.3. Input Signal Data Format

Set the panel timing registers appropriately for the input signal data format.

◆Register Settings

Address	Register name	Bits	Function
0x20 | 0x59	H_ACT_U | AZEN_D		Timing setting registers. Should be set appropriately for the input signal data format. Setting values are separately presented.

◆Panel Display Modes and Input Supported Formats

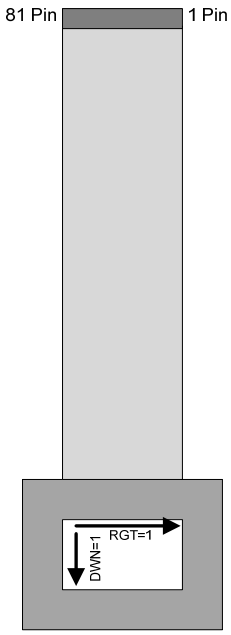
		①Full-HD 59.94Hz / 60Hz Frame Rate	②Full-HD 50Hz Frame Rate	③Full-HD 47.952Hz / 48Hz Frame Rate
Panel Display Mode		1920(H) X 1080(V)	1920(H) X 1080(V)	1920(H) X 1080(V)
Input Supported Format				
Active	H	1920	1920	1920
	V	1080	1080	1080
Total	H	2200	2640	2750
	V	1125	1125	1125
FP	H	88	528	638
	V	4	4	4
SYNC	H	44	44	44
	V	5	5	5
BP	H	148	148	148
	V	36	36	36
BP+SYNC	H	192	192	192
	V	41	41	41
fv	Hz	59.95 / 60	50	47.952 / 48
Th	µs	14.830 / 14.815	17.778	18.537 / 18.519
Clock	MHz	148.35 / 148.5	148.5	148.35 / 148.5

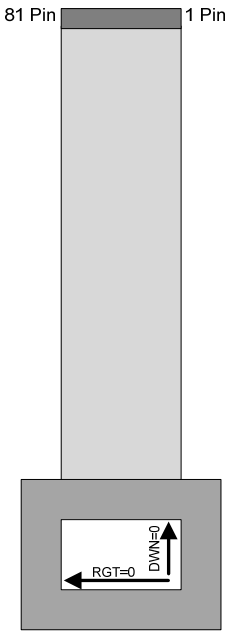
10.4. Up/down and/or Right/left Inversion Function

Up/down and right/left inverse display of the panel are set by the registers RGT and DWN, respectively.

◆Register settings

Address	Register	Bits	Setting Value
0x00	RGT	1	Selection of rightward / leftward scan 0: Leftward scan 1: Rightward scan (Default)
0x00	DWN	1	Selection of upward / downward scan 0: Upward scan 1: Downward scan (Default)

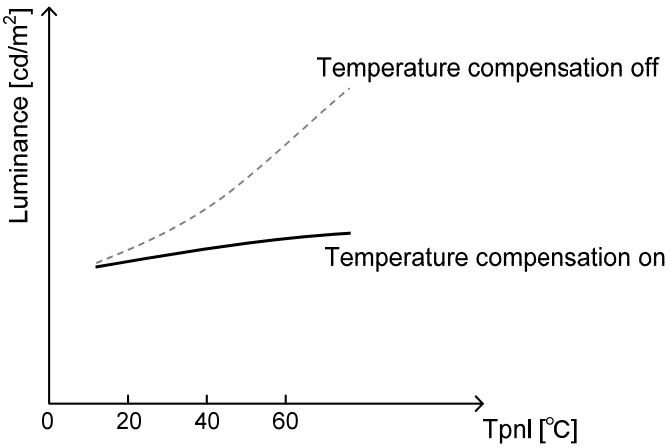




10.5. Luminance Temperature Compensation Function

Organic EL panels have characteristics such that the luminance changes according to the temperature.

This product has a function that compensates the temperature dependence of the panel luminance.



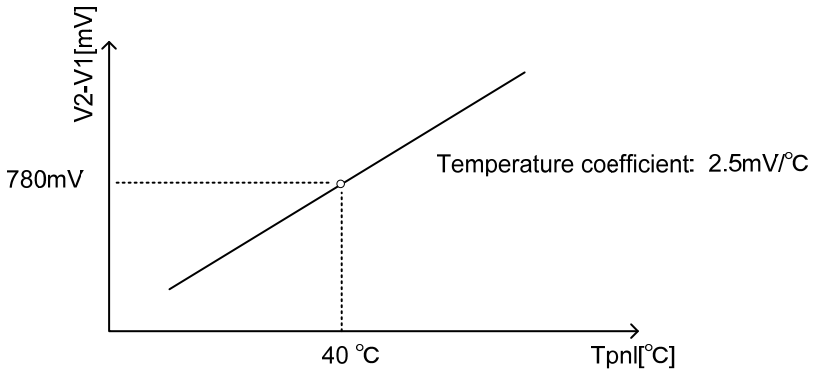
◆Register Settings

Address	Register name	Bits	Function
0x01	VCAL_MON	1	Display on/off when temperature sensor monitoring 0: on (Default) 1: off
0x01	CALSEL[1:0]	2	VCAL output selection 00: (default) 01: V1 output 10: V2 output

◆Method of Checking the Panel Temperature

The temperature sensor output voltage can be output from VCAL pin (#68).

Set the register VCAL_MON to 1: valid, set the register CALSEL as noted above, and read the V1 and V2 outputs. The temperature can be calculated by subtracting V1 from V2.



10.6. Luminance and White Balance Preset Mode

This product has 3 luminance and white balance preset modes.

By selecting the mode according to the register LUMINNACE, the luminance and the white chromaticity are adjusted to preset value.

◆Register Settings

Address	Register name	Number of bits	Function
0x08	OTPCALDAC_REGDIS	1	Luminance adjustment 0: Preset mode valid 1: Preset mode invalid (CALDAC adjustment)
0x08	OTPDG_REGDIS	1	White chromaticity adjustment 0: Preset mode valid 1: Preset mode invalid (CONT/BRT adjustment)
0x05	LUMINANCE[2:0]	3	Luminance and white chromaticity preset mode selection 2: 90cd/m2, (0.313,0.329) 0: 120cd/m2, (0.313,0.329) 3: 200cd/m2, (0.313,0.329)

10.7. Luminance adjustment function

Manual luminance adjustment is performed by CALDAC register.

This function is valid when OTPCALDAC_REGDIS=1.

◆Register settings

Address	Register name	Bits	Function
0x08	OTPCALDAC_REGDIS	1	Luminance adjustment 0: Preset mode valid 1: Preset mode invalid (CALDAC adjustment)
0×1D	CALDAC[7:0]	8	Luminance adjustment setting value: 1 to 255 (in decimal notation) Default :128

10.8. White Balance Adjustment Function

10.8.1. Contrast / Sub Contrast

RGB simultaneous and R, G and B separate contrast adjustment.
This function is valid when OTPDG_REGDIS=1.

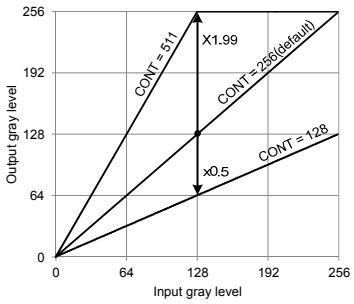
◆ Register Settings

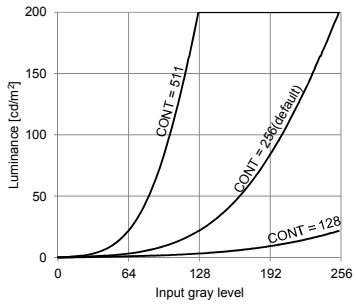
Address	Register name	Number of bits	Function
0x08	OTPDG_REGDIS	1	White chromaticity adjustment 0: Preset mode valid 1: Preset mode invalid (CONT and R/G/BCONT adjustment)
0x14, 0x15	CONT	9	To RGB input signal, × 0 ... × 1 (Default) ... × 1.99
0x15	RCONT	7	Sets R relative to CONT to × 0.75 ... × 1 (Default) ... × 1.24
0x16	GCONT	7	Sets G relative to CONT to × 0.75 ... × 1 (Default) ... × 1.24
0x17	BCONT	7	Sets B relative to CONT to ×0.75 ... × 1 (Default) ... ×1.24

◆Contrast Adjustment

R, G and B are adjusted simultaneously relative to the input signal using the register CONT. The setting value is 0 to 511 (decimal notation).

CONT setting value	0	…	128	…	256 (Default)	…	384	…	511
Gain (to input)	× 0	…	× 0.5	…	× 1	…	× 1.5	…	× 1.99



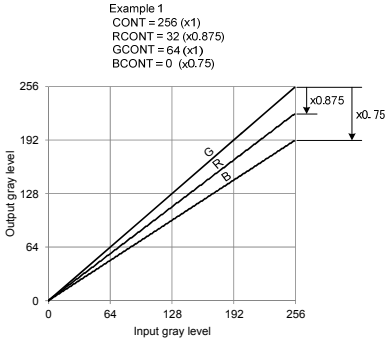


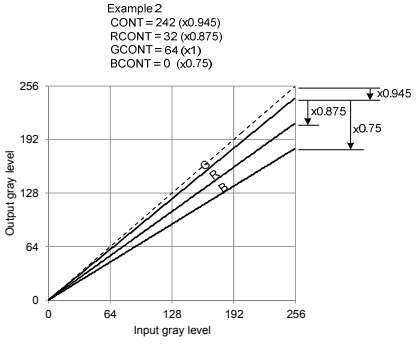
◆Sub Contrast Adjustment

R, G and B are adjusted separately using the registers RCONT, GCONT and BCONT, respectively.

The R, G and B gains can be set separately relative to the main CONT setting. The setting range is 0 to 127 (decimal notation).

R/G/BCONT setting value	0	…	32	…	64 (Default)	…	96	…	127
Gain (to CONT)	× 0.75	…	× 0.875	…	× 1	…	× 1.125	…	× 1.24





10.8.2. Bright/Sub Bright

RGB simultaneous and R, G and B separate brightness adjustment.
This function is valid when OTPDG_REGDIS=1.

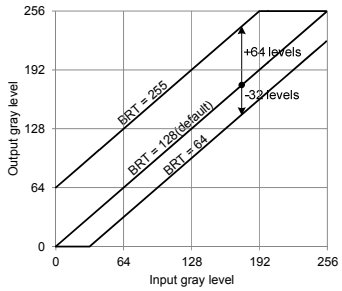
◆Register Settings

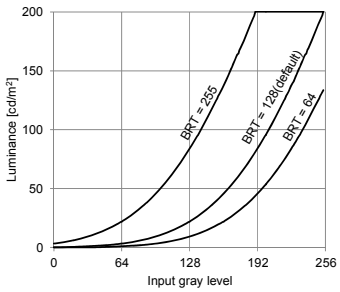
Address	Register name	Number of bits	Function
0x08	OTPDG_REGDIS	1	White chromaticity adjustment 0: Preset mode valid 1: Preset mode invalid (BRT and R/G/BBRT adjustment)
0x18	BRT	8	To RGB input signal, -64 ... 0 (Default) ... +63 gradations
0x19	RBRT	7	Sets R relative to BRT to-32 ... 0 (Default) ... +31 gradations
0x1A	GBRT	7	Sets G relative to BRT to-32 ... 0 (Default) ... +31 gradations
0x1B	BBRT	7	Sets B relative to BRT to-32 ... 0 (Default) ... +31 gradations

◆Brightness Adjustment

R, G and B are adjusted simultaneously relative to the input signal using register BRT. The setting value is 0 to 255 (decimal notation).

BRT setting value	0	…	64	…	128(Default)	…	192	…	255
Output gradations(to input)	-64	…	-32	…	0	…	+32	…	+63



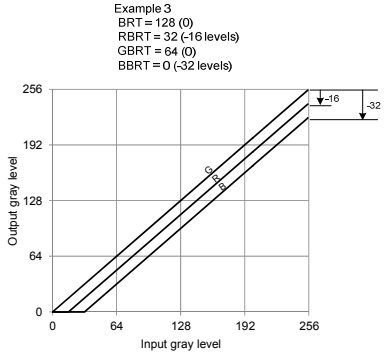


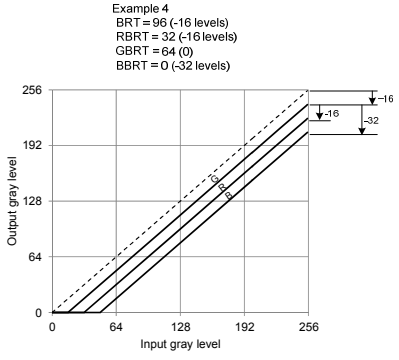
◆Sub Brightness Adjustment

R, G and B are adjusted separately using registers RBRT, GBRT and BBRT, respectively.

The R, G and B adjustments can be set separately relative to the main BRT setting. The setting range is 0 to 127 (decimal notation).

R/G/BBRT setting value	0	…	32	…	64 (Default)	…	96	…	127
Output gradations (to BRT)	-32	…	-16	…	0	…	+16	…	+31





10.9. Dithering Function

This function expresses simulated gradations between the original gradations by using FRC.

This is used to interpolate gradations that decrease due to contrast or brightness adjustment.

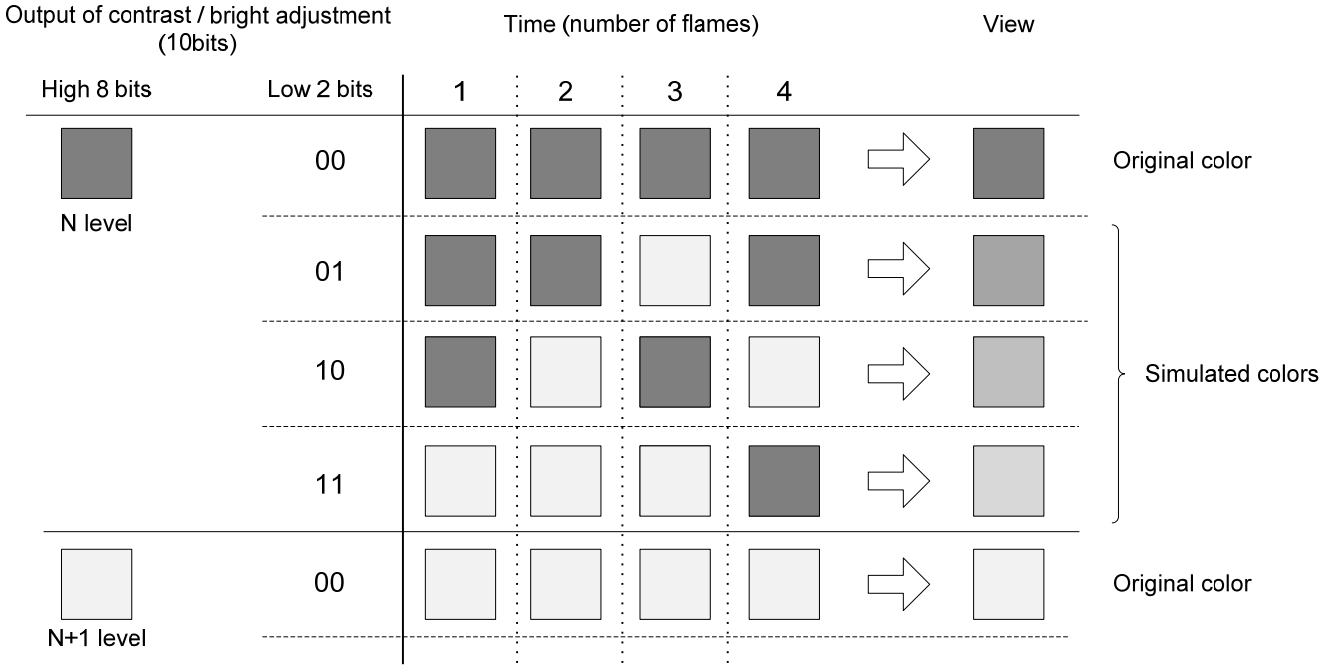
◆Register Settings

Address	Register name	Bits	Function
0x05	DITHERON	1	Dithering processing 0: Off 1: On

10.9.1. FRC (Frame Rate Control)

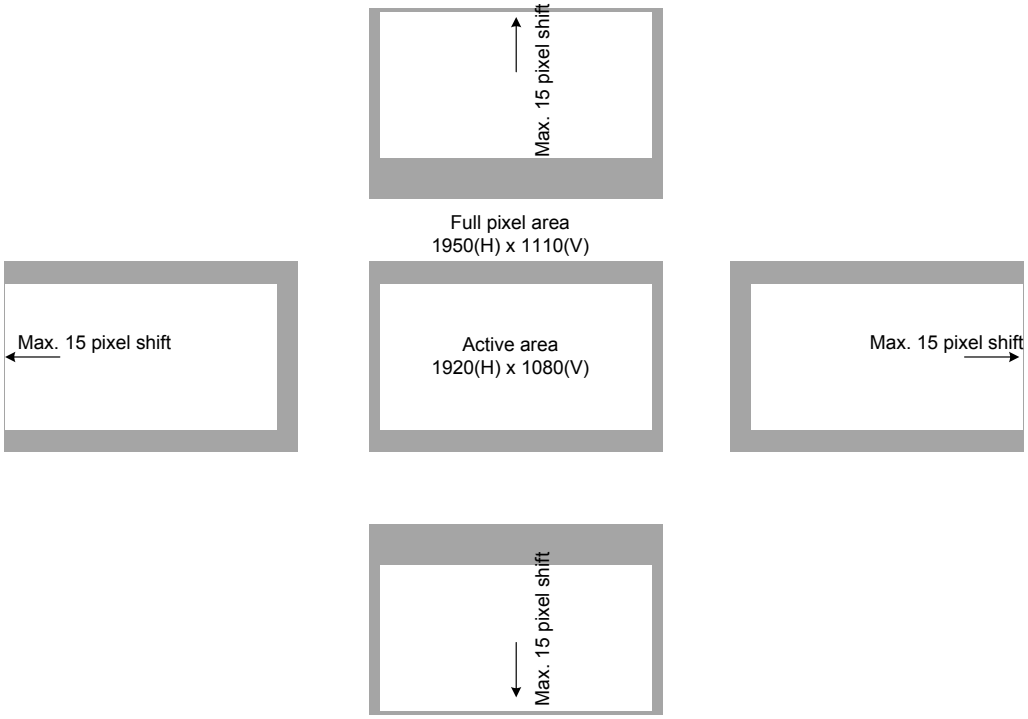
Simulated colors are expressed making use of frame rate and image lag effect of human eyes. When two colors are switching alternately in high-speed, it looks an intermediate color for human eyes. Three simulated colors can be added to original colors by changing data in 4-frame cycle making use of this property (2 bit FRC).

FRC simulated color image when noticing arbitral one pixel is shown below.



10.10. Orbit Function

The image data start position can be changed. This enables reducing of the noticeability of local drops in luminance.



◆Register Settings

Address	Register name	Bits	Function
0x02	ORBIT_H[4:0]	5	Horizontal orbit adjustment -15 to 0 to +15, Default: 0
0x03	ORBIT_V[4:0]	5	Vertical orbit adjustment -15 to 0 to +15, Default: 0

10.1. Horizontal Display Position Shift

Change the display start position using the register ORBIT_H. The variable range is ± 15 pixels.

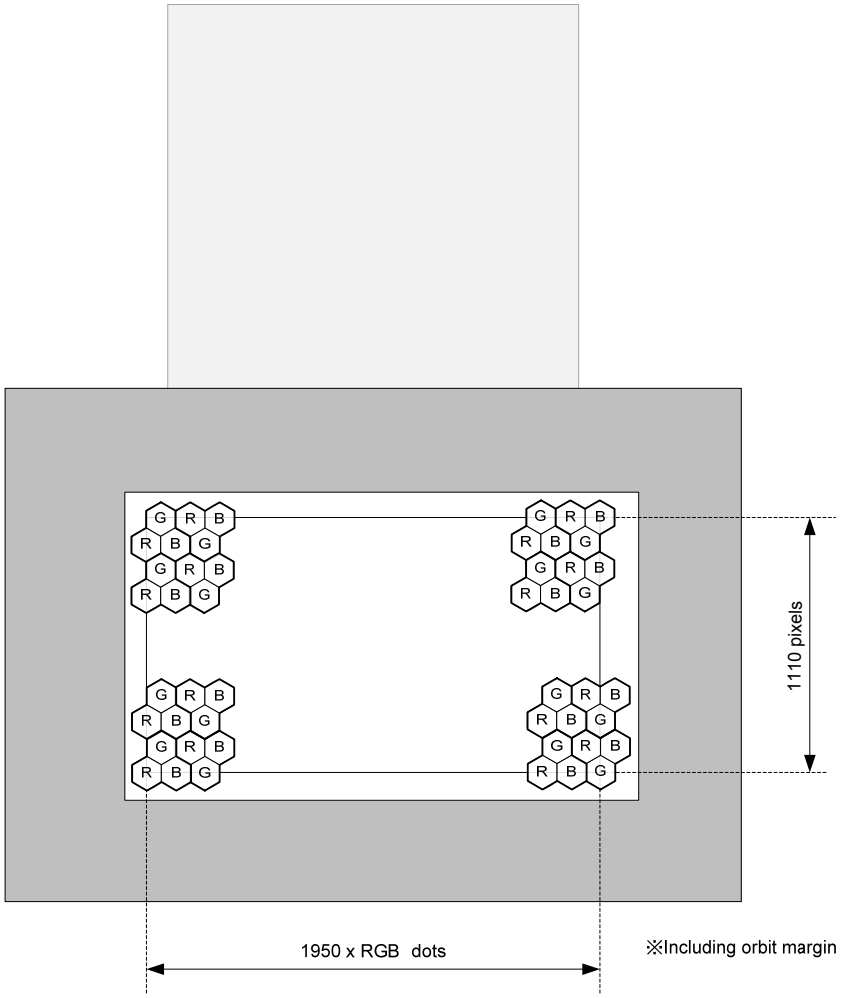
ORBIT_H setting value	-15	…	-1	0 (Default)	1	…	15
Number of pixels shifted	Leftward 15-pixel	…	Leftward 1-pixel	Center	Rightward 1-pixel	…	Rightward 15-pixel

10.2. Vertical Display Position Shift

The display start position is changed by the register ORBIT_V The variable range is ± 15 pixels.

ORBIT_V setting value	-15	…	-1	0 (Default)	1	…	15
Number of pixels shifted	Upward 15-pixels	…	Upward 1-pixel	Center	Downward 1-pixel	…	Downward 15-pixel

11. Pixel Alignment



12. Optical Characteristics

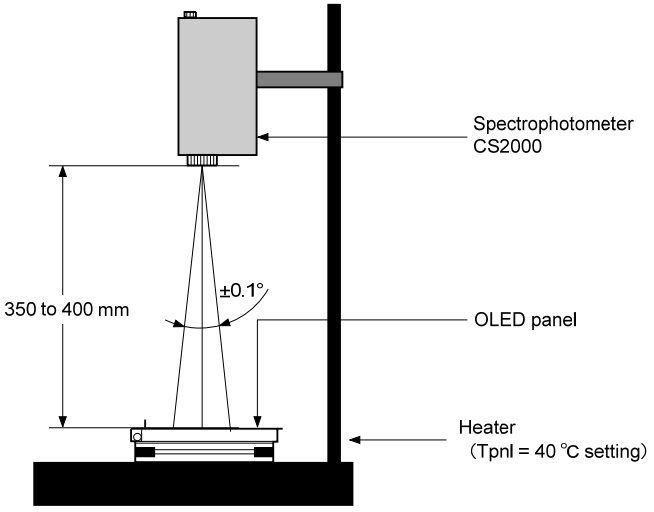
12.1. Optical Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
Luminance	Mode 2	L2	76	90	104	Cd/m^2
	Mode 0	L0	102	120	138	Cd/m^2
	Mode 3	L3	170	200	230	Cd/m^2
White chromaticity	Mode 2	W2x	0.298	0.313	0.328	CIE
		W2y	0.314	0.329	0.344	CIE
	Mode 0	W0x	0.298	0.313	0.328	CIE
		W0y	0.314	0.329	0.344	CIE
	Mode 3	W3x	0.298	0.313	0.328	CIE
		W3y	0.314	0.329	0.344	CIE
Monochrome chromaticity	R	Rx	0.635	0.655	0.675	CIE
		Ry	0.310	0.330	0.350	CIE
	G	Gx	0.255	0.275	0.295	CIE
		Gy	0.625	0.645	0.665	CIE
	B	Bx	0.127	0.147	0.167	CIE
		By	0.045	0.065	0.085	CIE
Contrast		CR	10,000	—	—	

12.2. Measurement System・Measurement Method

Measurement temperature: Tpnl = 40°C
Measurement point: One point on the screen center
Regisiter setting: OTPCALDAC_REGDIS = 0、OTPDG_REGDIS = 0

Item		Pattern / Gray level		Register setting	Method
Luminance / White chromaticity	L2,W2x,W2y	White raster	R=255 G=255 B=255	LUMINANCE = 2	Measured by system A
	L0,W0x,W0y			LUMINANCE = 0	
	L3,W3x,W3y			LUMINANCE = 3	
Monochrome chromaticity	Rx,Ry	Red raster	R=255		Measured by system A
	Gx,Gy	Green raster	G=255		
	Bx,By	Blue raster	B=255		
Contrast	CR	White & black raster	White: R=255 G=255 B=255 Black: R=0 G=0 B=0	LUMINANCE = 3	Measured by system A Contrast = white / black



System A

13. Picture Quality Specification

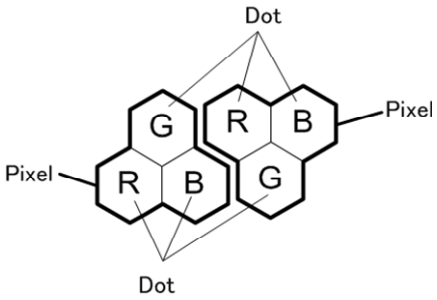
13.1. Dot and Pixel defect specification

Dot and Pixel defect specification is summarized in below. Definition of each defect is listed in following section.

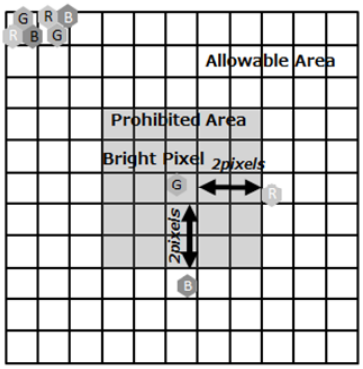
	Inspection condition			Maximum acceptable number of defect			Minimum acceptable distance between defects	Reference
	Luminance 100%	Defect size	Criteria of Luminance Level	Zone A	Zone B	Total		
Bright Dot	Green Raster Red Raster Blue Raster (White 200cd/m2)	1 dot	Green : L≧20% Red : L≧25% Blue : L≧80%	0	0	0	N/A	13.1.1
		1 dot	Green : 20%>L≧11% Red : 25%>L≧11% Blue : 80%>L≧50%	0	2	2	“Horizontal 2 pixels” or “Vertical 2 pixels”	13.1.1
		1 dot	Green : 11%>L Red : 11%>L Blue : 50%>L	Ignored	Ignored	Ignored	N/A	13.1.1
Too-Bright Dot	Green Raster Red Raster Blue Raster (White 200cd/m2)	1 dot	Green : L≧200% Red : L≧200% Blue : L≧300%	0	0	0	N/A	13.1.2
		1 dot	Green : 200%>L Red : 200%>L Blue : 300%>L	Ignored	Ignored	Ignored	N/A	13.1.2
Dim Pixel	White raster 200cd/m2	1 pixel	White : 10%≧L	2	5	7	“Horizontal 2 pixels” or “Vertical 2 pixels”	13.1.3
		1 pixel	White : L>10%	Ignored	Ignored	Ignored	N/A	13.1.3

13.1.1 Definition of Bright dot defect

Suspected bright dot defect is inspected on Black raster display. Criteria to judge as defect or not should be comparison with Luminance level on Red or Green or Blue raster display, according to which dot is suspected. 1 Dot is unit of the Bright dot defect. Please refer definition for Dot and Pixel. Minimum acceptable distance between defects is defined as following.



Definition of Pixel and Dot



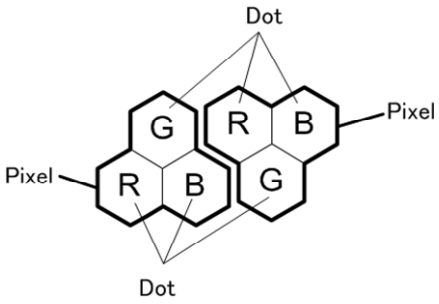
Minimum acceptable distance between defects

13.1.2 Definition of too-bright dot defect

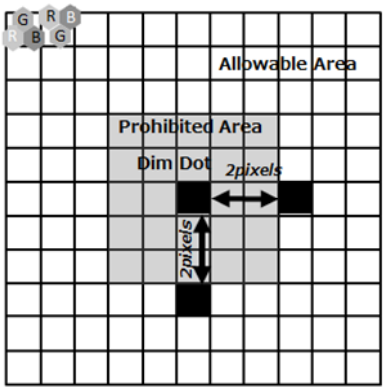
Suspected too-bright dot defect is too-much brighter dot other than normal luminance. Criteria to judge as defect or not should be comparison with Luminance level on Red or Green or Blue raster display, according to which dot is suspected. Minimum acceptable distance between defects is same as that of bright dot defect.

13.1.3 Definition of Dim pixel defect

Suspected dim pixel is inspected White raster display. Criteria to judge as defect or not should be comparison with Luminance level on White raster. 1 pixel consists of 3 Dots. 1 Pixel is unit of the Dim pixel defect. And, minimum acceptable distance between defects is defined as following.



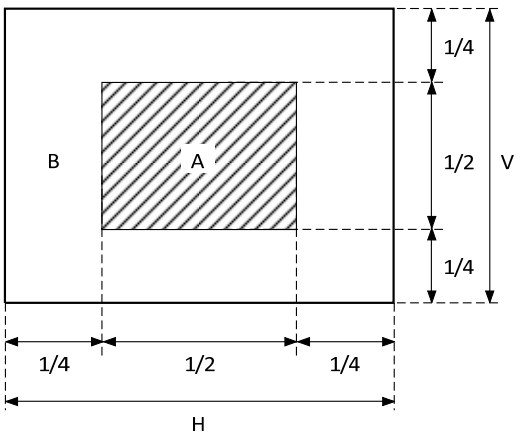
Definition of Pixel and Dot



Minimum acceptable distance between defects

13.1.4 Definition of Zone A and B

Zone A and Zone B are defined as shown in below.



14. Line defect specification

Line defect specification and definition is summarized in below.

Item		Definition as defect	Maximum acceptable number of defect
Line defect	Bright line defect	Bright line consists of continuous 2 dots or more	0
	Dim line defect	Dim line consists of continuous 2 pixels or more	0

15. Uniformity Specification

Uniformity specification is unevenness display due to not dot or pixel defects but others.

(Tpn1 = 40 °C)

Item	Definition	Specification
Vertical uneven line	Dark uneven vertical line of 1 dot width on R or G, B raster.	There should be no abnormality that impairs practical usage. Separated discussions shall be held if needed.
Horizontal uneven line	Horizontal uneven line can be detected ranging from White raster to brighter gray raster.	
Dark stain	Dark strain can be detected at darker gray raster.	
Bright stain	Bright strain can be detected ranging from White raster to brighter gray raster.	
Uneven lines like string	Uneven lines like string can be detected ranging from White raster to brighter gray raster.	

16. Appearance Specification

Appearance specification is detected at power off because of physical related not electrical related defect.

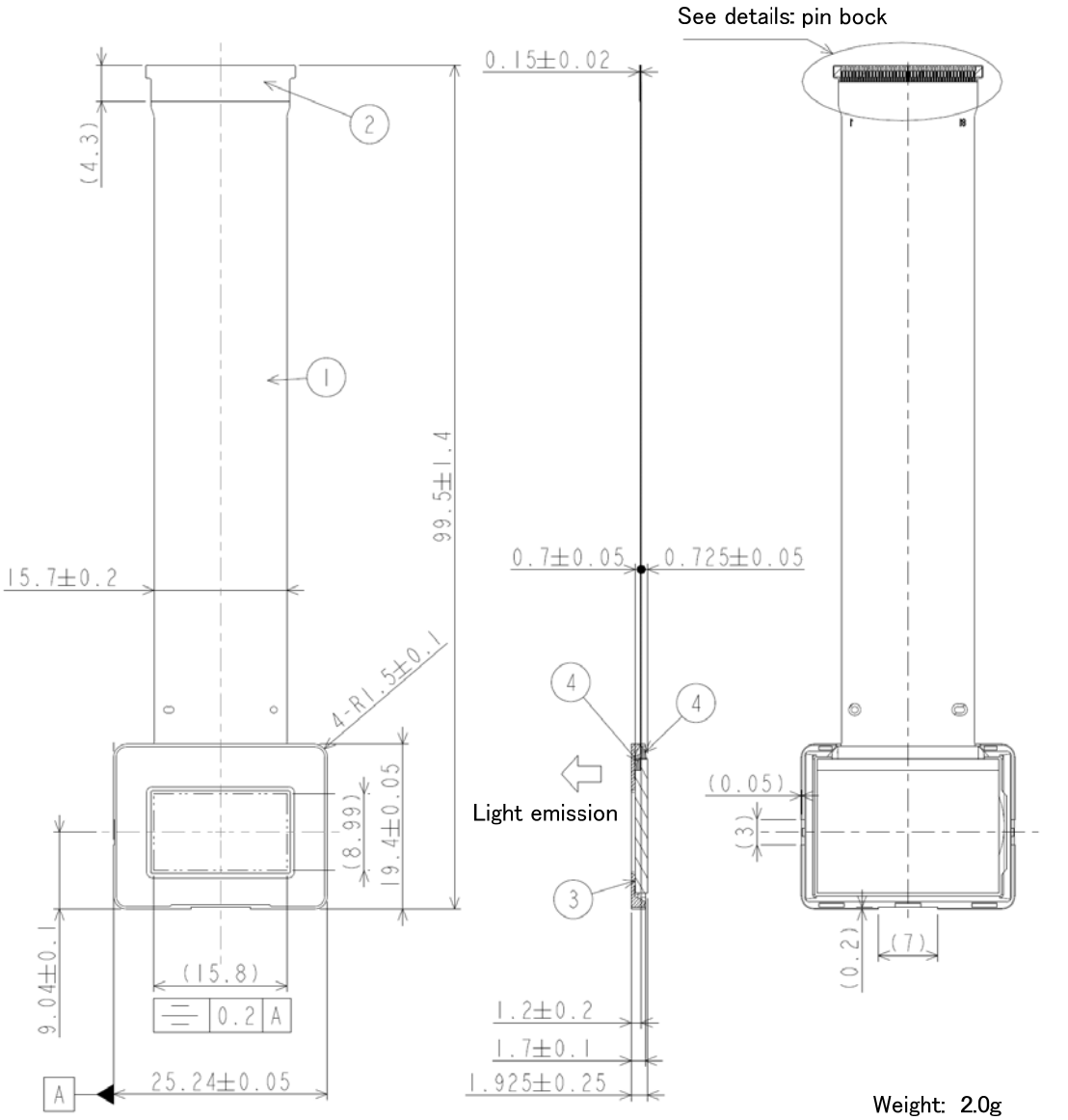
Item	Definition	Specification
Abnormality on panel surface	For example, unevenness in Active Area. Chipping and scratching on other than Active Area, etc.	There shall be no hindrance to actual use. Separated discussions shall be held if needed. (Ignore abnormalities that cannot be detected in the picture quality inspection.)

17. Environmental Test

Item		Specification	Criteria
Storage test	High temperature	85 °C 1000 hours	There should be no remarkable deterioration in appearance and performance after the test.
	High temperature and high humidity	60 °C 90 % 1000 hours	
	Low temperature	-30 °C 1000 hours	
	Temperature cycle	-30 to 85 °C, 100 cycles (retention time is 30min.)	
Operation test	High temperature	70 °C 500 hours	
	High temperature and high humidity	40 °C 95 % 500 hours	
	Low temperature	-10 °C 500 hours	
Strength test	Static charge	JEITA ED-4701/302 (HBM・CDM)	There should be no remarkable abnormality that impairs use in display appearance and panel appearance.
	Vibration	20 min. in X, Y, Z direction, 5 to 50 Hz (random wave vibration)	
	Shock	980m/s^2 6ms ±X,±Y,±Z (each 3 times)	

18. Package Outline (Nagasaki 200mm wafer)

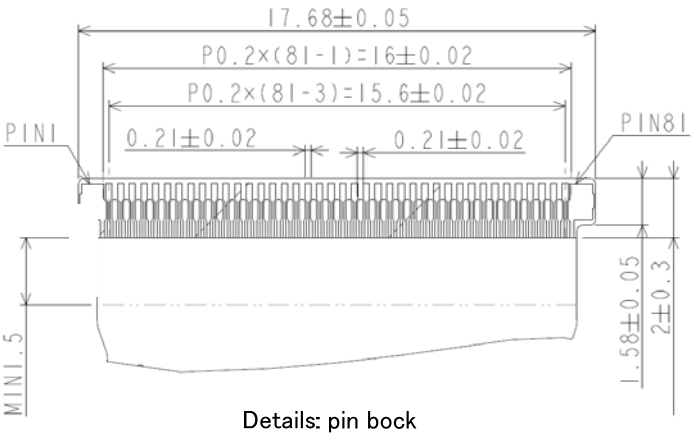
(Unit : mm)



Weight: 2.0g

No	Item
1	FPC
2	Reinforcing Plate
3	Frame
4	Stiffner

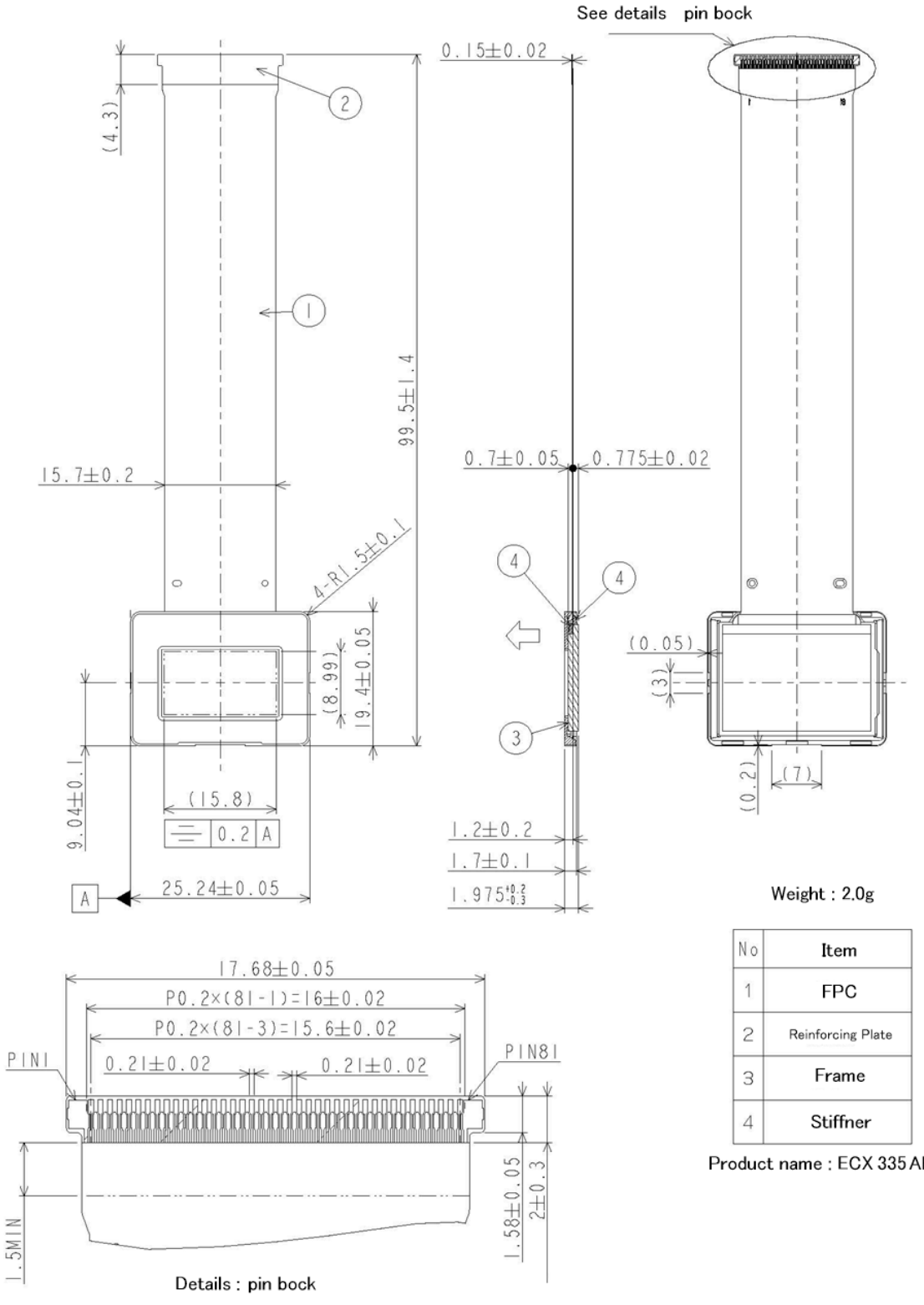
Product name: ECX335AF



Details: pin bock

Package Outline (Kumamoto 300mm wafer)

(Unit : mm)

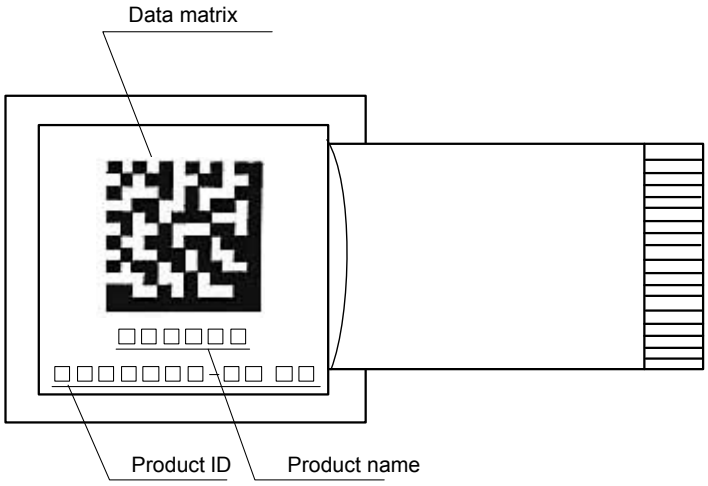


No	Item
1	FPC
2	Reinforcing Plate
3	Frame
4	Stiffner

Product name : ECX 335 AF

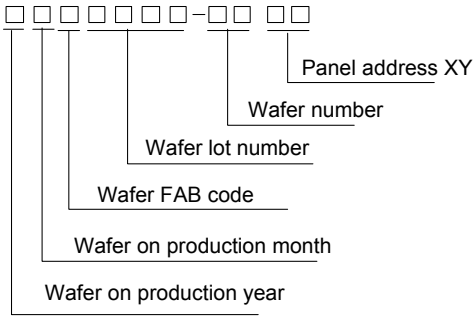
19. Marking Specification

To make sure traceability, following marks are recorded.

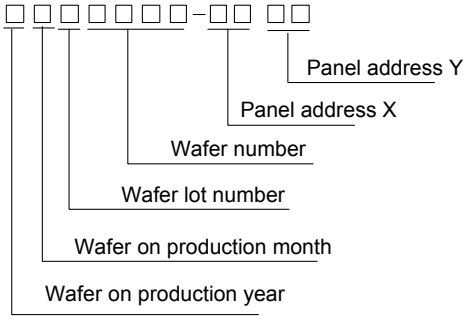


Product ID

(Nagasaki 200mm wafer)



(Kumamoto 300mm wafer)



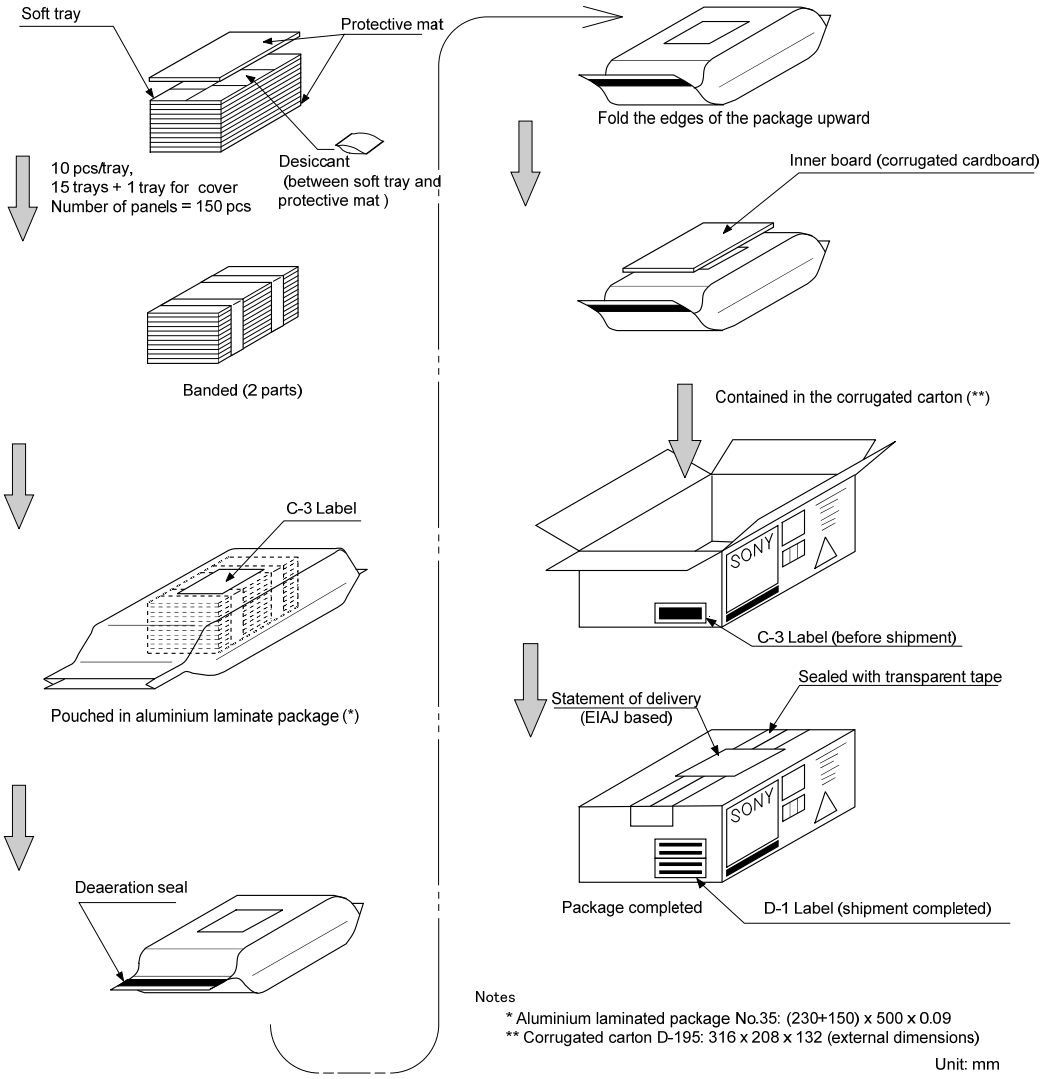
20. Packing Specification

Tray design: Soft type

Number of panel module in tray : 10pcs

Number of tray in Carton: 15 sheets

Number of panel module in carton : 10 pcs × 15 sheets = 150 pcs

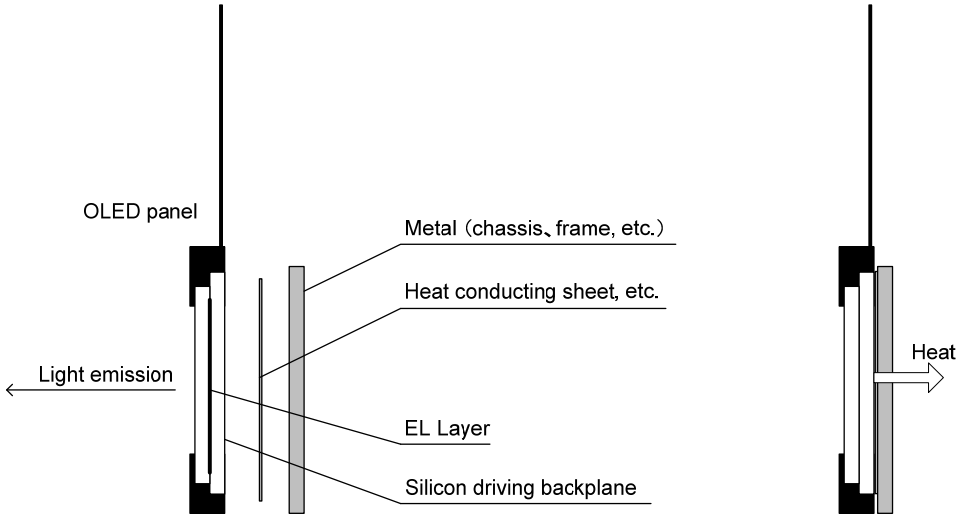


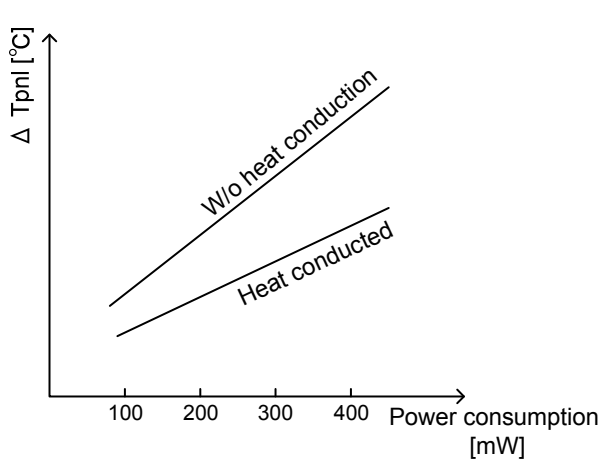
21. Recommendation Item

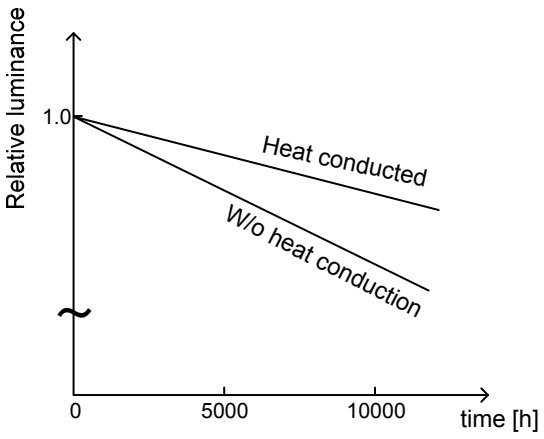
21.1. Suppression of the Panel Temperature

Organic EL panel temperatures rise due to power consumption (heat generation) by the EL emissive layer and the silicon drive board. A rise in the panel temperature may affect the drop in luminance over time.

The rise in panel temperature can be suppressed by establishing a thermal connection between the rear surface (silicon board surface) of the panel and metal (chassis, frame, etc.) in the panel mount area.







22. Notes on Handling

22.1. Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves, use bare hands.

(2) Use a wrist strap when handling.

(3) Do not touch any electrodes of the panel.

(4) Wear non-chargeable clothes and conductive shoes.

(5) Install grounded conductive mats on the working floor and working table.

(6) Keep the panel away from any charged materials.

22.2. Protection from dust and dirt

(7) Operate in a clean environment.

(8) Do not touch the panel surface. The surface is easily scratched.
When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.

(9) Use ionized air to blow dust off the panel surface.

22.3. Others

(10) Do not hold the flexible board or twist or bend it because the flexible board connection block is easily affected by twisting.

(11) The minimum fold radius of the flexible board is 1 mm.

(12) Do not drop the panel.

(13) Do not twist or bend the panel.

(14) Keep the panel away from heat sources.

(15) Do not dampen the panel with water or other solvents.

(16) Do not store or use the panel (module) at high temperatures or high humidity, as this may affect the characteristics.

(17) When disposing of this panel, handle it as industrial waste and comply with related regulations.

(18) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as this may affect the performance.

(19) This panel is delivered packed in a degassed aluminum laminated bag.
When storing this panel after unsealing the bag, put it into the aluminum laminated bag again and seal it with tape with the opening folded after inserting desiccants.