SONY

1.3 cm (0.5inch) Active Matrix Color OLED Panel Module

ECX337AF

1. Overview / Application

ECX337AF is a 1.3 cm (0.5inch) diagonal, 1280(RGB) × 960 dots active matrix color OLED (Organic Light Emitting Display) panel module based on single crystal silicon transistors. The module integrates panel driver and logic driver, and achieves smaller size, light in weight and high resolution. .

(Potential applications: Head mounted displays, View finders, Small monitors etc.)

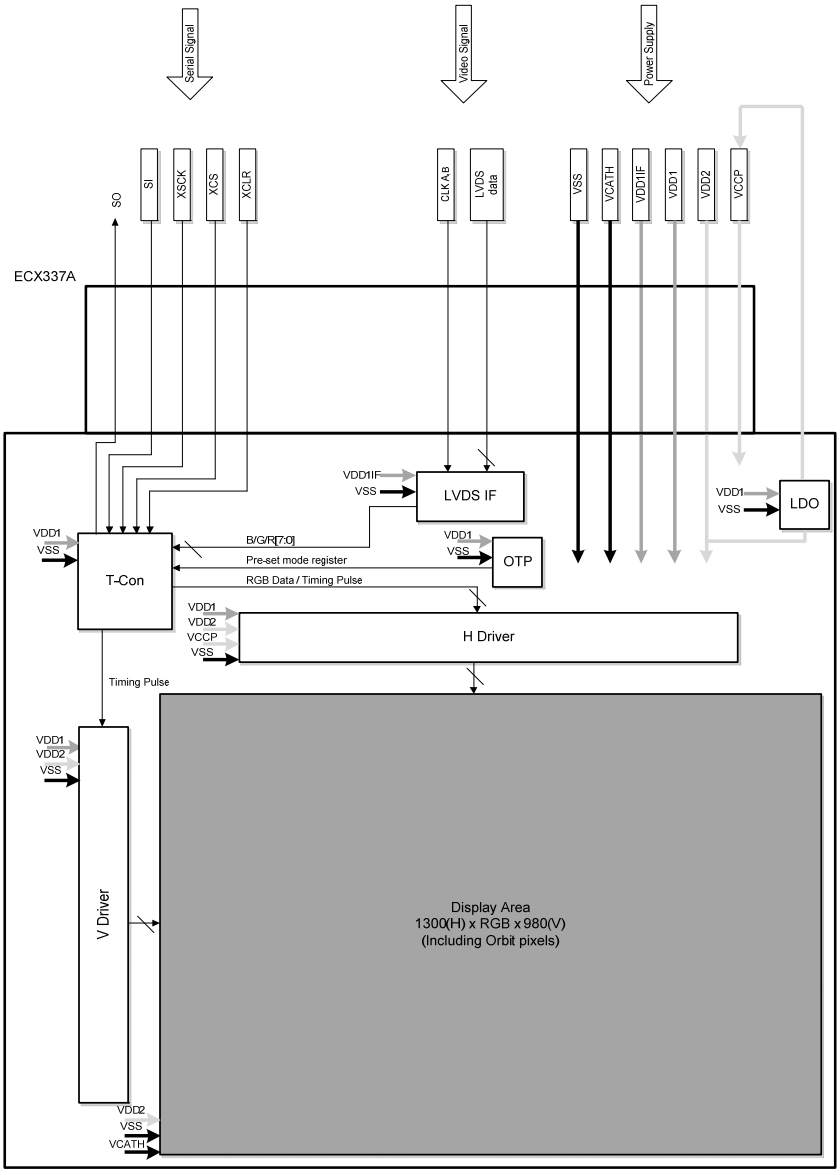
2. Features / Function

- Small size high resolution type 0.5 inch display module
- Effective Dots: 1280 x RGB × 960 = 3.69 M dots
- Actual Dots including Orbit function: Total dots 1300 x RGB x 980 = 3.82 M dots
- Ultra high contrast
- Wide color gamut
- Fast response speed
- Thin and light in weight
- Power consumption Saving (PS) mode
- Scan direction selection, up or down and right or left.

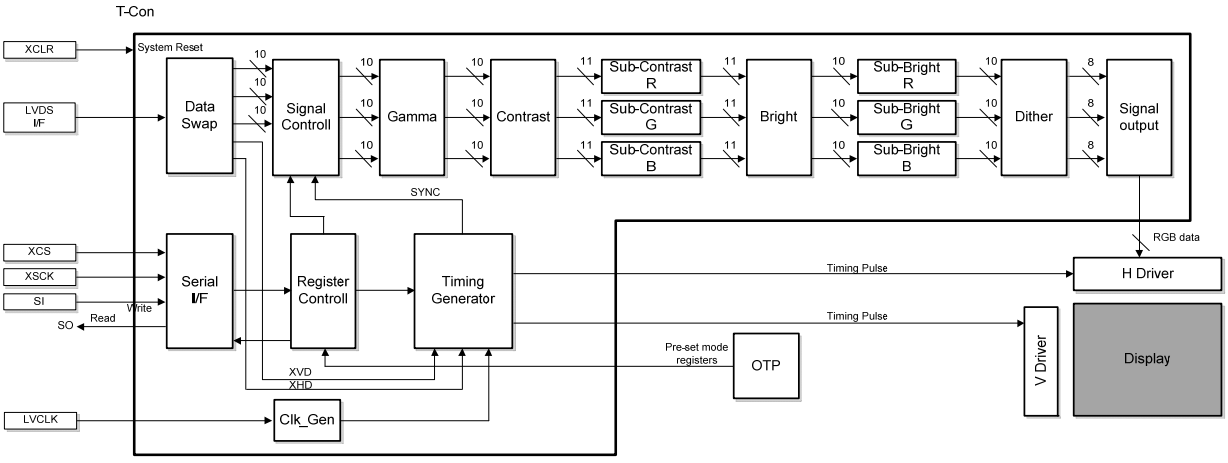
3. Module Structure

Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

4. System Block Diagram

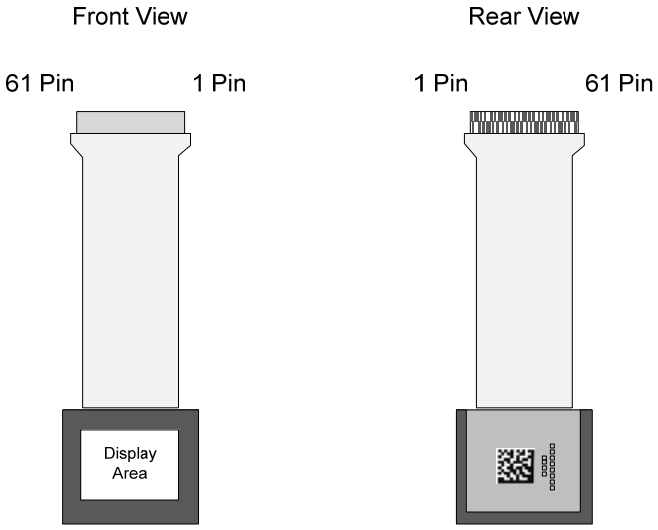


Details of “T-con”



5. Pin Description

5.1. Pin Assignment



5.2. Pin description

Pin No. (FPC Side)	Symbol	I/O Type	Voltage System	Description	Equivalent circuit
1	VCATH	GND(0)	10V	EL Cathode Voltage (Connect to GND)	
2	VCCP_O	Power Output	10V	LDO Output	※8
3	VDD2	Power Input	10V	VDD2 Power Supply	
4	VSS	GND	10V	Ground	
5	VDD1	Power Input	1.8V	VDD1 Power Supply	
6	TEST	Power Input	10V	Test Pin (Connect to GND)	※7
7	TEST	Input	1.8V	Test Pin (Connect to GND)	※5
8	XCS	Input	1.8V	SPI Communication Chip Select	※1
9	XSCK	Input	1.8V	SPI Communication Clock	※1
10	SI	Input	1.8V	SPI Communication Data Input	※1
11	SO	Output	1.8V	SPI Communication Data Output	※2
12	TEST	Output	1.8V	Test Pin (Open)	※3
13	TEST	Input	1.8V	Test Pin (Connect to GND))	※1
14	TEST	Input	1.8V	Test Pin (Connect to VDD1)	※1
15	XCLR	Input	1.8V	System Reset Signal	※1
16	VSSIF	GND	1.8V	Interface GND ※	
17	VDD1IF	Power Input	1.8V	Interface VDD1Power Supply	
18	TEST	Output	1.8V	Test Pin (Open)	※4
19	LVCLK0A	Input	1.8V	sub-LVDS / LVDS clock (Positive)	※6
20	LVCLK0B	Input	1.8V	sub-LVDS / LVDS clock (Negative)	※6

Pin No. (FPC Side)	Symbol	I/O Type	Voltage System	Description	Equivalent circuit
21	LV0A	Input	1.8V	Data signal (Positive)	※6
22	LV0B	Input	1.8V	Data signal (Negative)	※6
23	LV1A	Input	1.8V	Data signal (Positive)	※6
24	LV1B	Input	1.8V	Data signal (Negative)	※6
25	LV2A	Input	1.8V	Data signal (Positive)	※6
26	LV2B	Input	1.8V	Data signal (Negative)	※6
27	LV3A	Input	1.8V	Data signal (Positive)	※6
28	LV3B	Input	1.8V	Data signal (Negative)	※6
29	LV4A	Input	1.8V	Data signal (Positive)	※6
30	LV4B	Input	1.8V	Data signal (Negative)	※6
31	VDD1IF	Power Input	1.8V	Interface VDD1 power supply	
32	VSSIF	GND	1.8V	Interface Ground ※	
33	TEST	GND	1.8V	Test Pin (Connect to Interface Ground) ※	※6
34	TEST	GND	1.8V	Test Pin (Connect to Interface Ground) ※	※6
35	VSSIF	GND	1.8V	Interface Ground ※	
36	VDD1IF	Power Input	1.8V	Interface VDD1 power supply	
37	LV5A	Input	1.8V	Data signal (Positive)	※6
38	LV5B	Input	1.8V	Data signal (Negative)	※6
39	LV6A	Input	1.8V	Data signal (Positive)	※6
40	LV6B	Input	1.8V	Data signal (Negative)	※6
41	LV7A	Input	1.8V	Data signal (Positive)	※6
42	LV7B	Input	1.8V	Data signal (Negative)	※6
43	LV8A	Input	1.8V	Data signal (Positive)	※6
44	LV8B	Input	1.8V	Data signal (Negative)	※6
45	LV9A	Input	1.8V	Data signal (Positive)	※6
46	LV9B	Input	1.8V	Data signal (Negative)	※6
47	LVCLK1A	Input	1.8V	sub-LVDS / LVDS clock (Positive)	※6
48	LVCLK1B	Input	1.8V	sub-LVDS / LVDS clock (Negative)	※6
49	VDD1IF	Power Input	1.8V	Interface VDD1 power supply	
50	VSSIF	GND	1.8V	Interface Ground ※	
51	VDD1	Power Input	1.8V	VDD1 Power Supply	
52	VSS	GND	10V	Ground	
53	VDD2	Power Input	10V	VDD2 Power Supply	
54	VGC	Power Output	10V	Gamma Voltage	※8
55	VCAL	Power Output	10V	Temperature Sensor Output Voltage	※8
56	VG255	Power Output	10V	Gamma Reference Voltage	※8

Pin No. (FPC Side)	Symbol	I/O Type	Voltage System	Description	Equivalent circuit
57	VG0	Power Output	10V	Gamma Reference Voltage	※8
58	VOFS	Power Output	10V	Offset Voltage	※8
59	VREF	Power Output	10V	Reference Voltage	※8
60	VCCP_I	Power Output	10V	Panel Power Supply	
61	VCATH	GND	10V	EL Cathode Voltage (Connect to GND)	

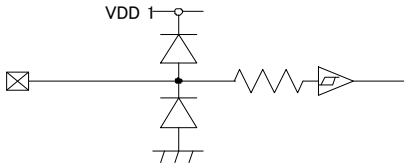
※Note ; Please allocate “VSSIF” independent ground, not common ground with other ground.

Please refer “10.3 Swapping function” with regarding to Positive/Negative.

5.3. Equivalent Circuits

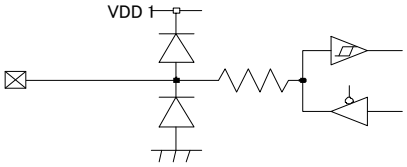
※1 Schmitt Pin

8. XCS
9. XSCK
10. SI
13. TEST
14. TEST
15. XCLR



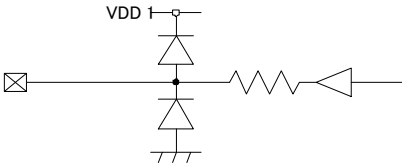
※2 Schmitt Pin

11. SO



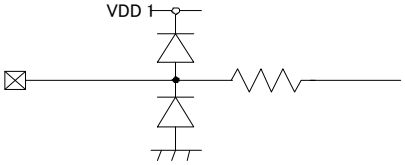
※3

12. TEST



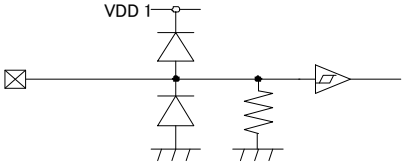
※4

18. TEST



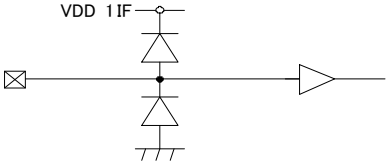
※5 Schmitt Pin

7. TEST



※6

19. LVCLK0A
20. LVCLK0B
21. LV0A
22. LV0B
23. LV1A
24. LV1B
25. LV2A
26. LV2B
27. LV3A
28. LV3B
29. LV4A
30. LV4B
33. TEST
34. TEST
37. LV5A
38. LV5B
39. LV6A
40. LV6B
41. LV7A
42. LV7B
43. LV8A
44. LV8B
45. LV9A
46. LV9B
47. LVCLK1A
48. LVCLK1B



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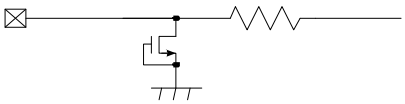
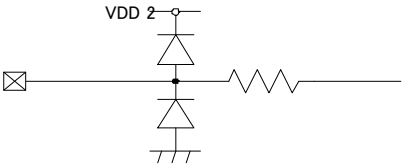
6. TEST



※8

2. VCCP O
54. VGC
55. VCAL
56. VG255
57. VG0
58. VOFS
59. VREF



5.4. Peripheral Circuit Example

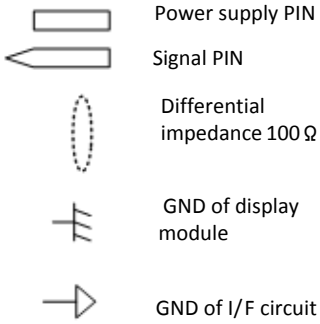
1) Capacitance specification;X5 R or B

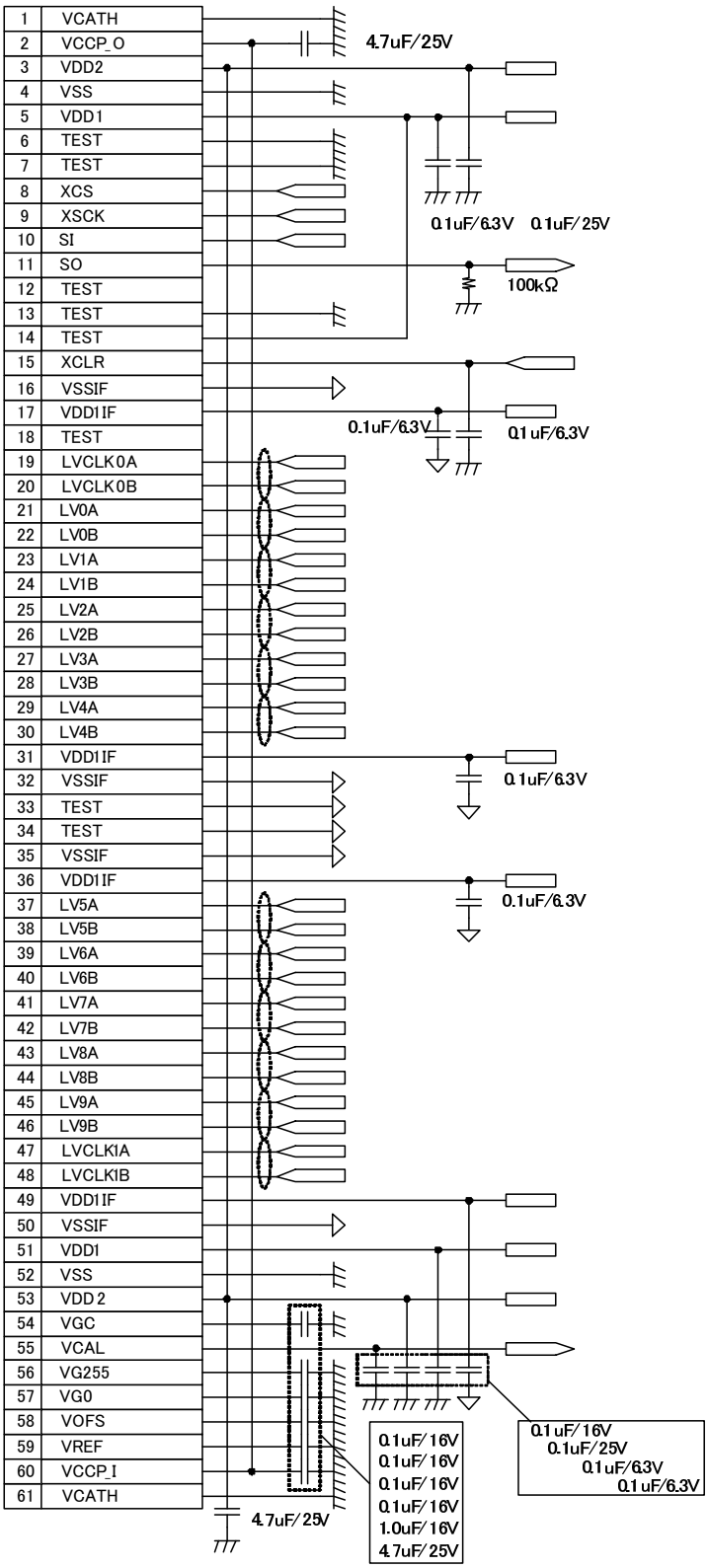
2) Capacitance for power supply
Please connect the capacitance directly to each power supply. If effective capacitance is not enough it can affect display picture quality.

3) Connection between 2 pin and 60pin
Please design connection between them as short as possible.

4) Please connect un-used pin based on selected interface specification to ground pin of input interface circuit.

5) VSS IF
Please allocate independent GND pattern for VSSIF.





※Above circuit is just one of typical example for reference to drive the module. Sony does NOT take any liability if the circuit example cause any problem because the circuit is only for reference。

6. Absolute Maximum Ratings

Item	Symbol	Min.	Maximum Ratings	Unit
1.8V power supply	VDD1	-0.3	2.0	V
1.8V power supply (IF)	VDD1IF	-0.3	2.0	V
10 V power supply	VDD2	-0.3	12.0	V
EL cathode voltage	Vcath	-0.3	0.3	V
Logic input voltage ※	Vi	-0.3	VDD1+0.3	V
IF input voltage ※※	ViIF	-0.3	VDD1IF+0.3	V
Storage temperature	Tpnl	-30	+80	°C

※ Pin # 8-10,30

※※ Pin # 19-30,37-48.

7. Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
1.8V power supply	VDD1	1.62	1.8	1.98	V
1.8V power supply (IF)	VDD1IF	1.62	1.8	1.98	V
10 V power supply	VDD2	9.7	10.0	10.3	V
EL cathode voltage	Vcath	-0.3	0	0.3	V
Operating temperature range ※	Tpnl	-10		70	°C

※Center position on panel rear surface.

8. Electrical Characteristics

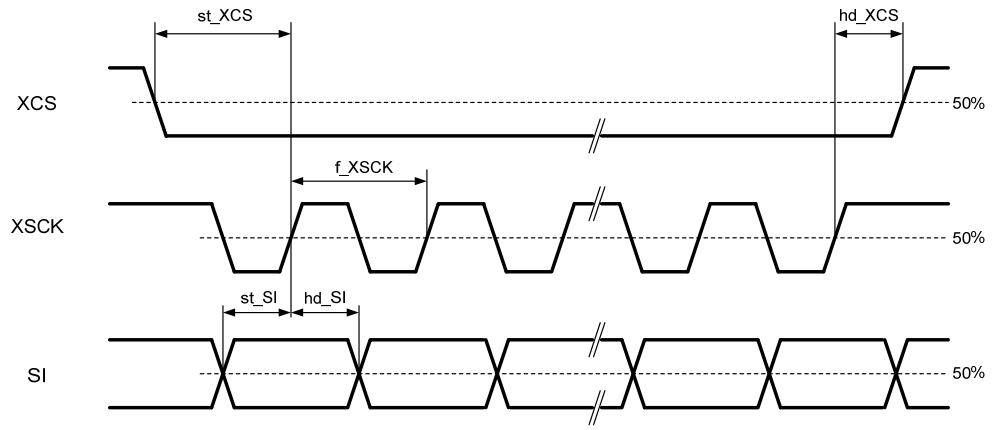
8.1. Serial Interface

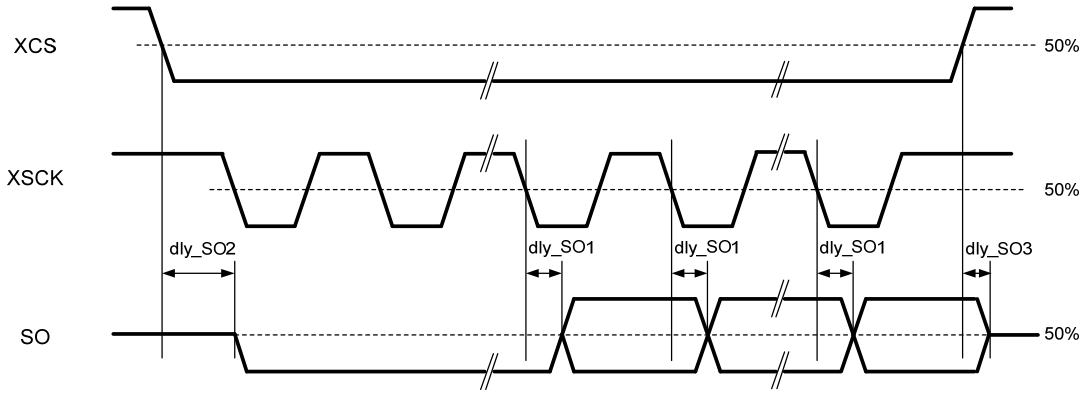
8.1.1. DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	VIH		0.7xVDD1		VDD1	V
Low-level input voltage	VIL		0		0.3xVDD1	V
High-level input voltage	Vt+	Schmitt input	0.7xVDD1		VDD1	V
Low-level input voltage	Vt-	Schmitt input	0		0.3xVDD1	V
Vt+ - Vt-	Vhys	Schmitt input		0.50		V
Logic High -level Output voltage	VOH	IO = -1.0mA	VDD1 - 0.4			V
Logic Low -level Output voltage	VOL	IO = +1.0mA			0.4	V

8.1.2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
XSCK frequency	f_XSCK			0.8	10	MHz
XCS setup time	st_XCS		12.5			ns
XCS hold time	hd_XCS		12.5			ns
SI setup time	st_SI		12.5			ns
SI hold time	hd_SI		12.5			ns
SO output delay 1	dly_SO1		3.0		12.5	ns
SO output delay 2	dly_SO2		3.5		18.5	ns
SO output delay 3	dly_SO3		3.5		18.5	ns

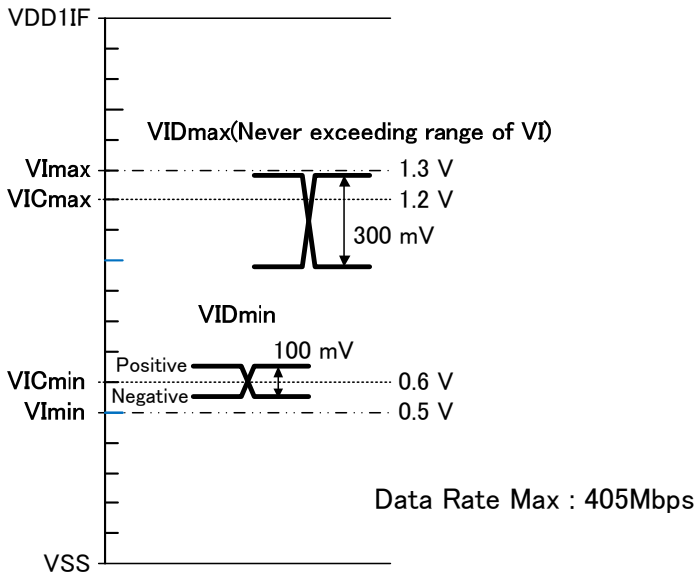




8.2. sub-LVDS Input

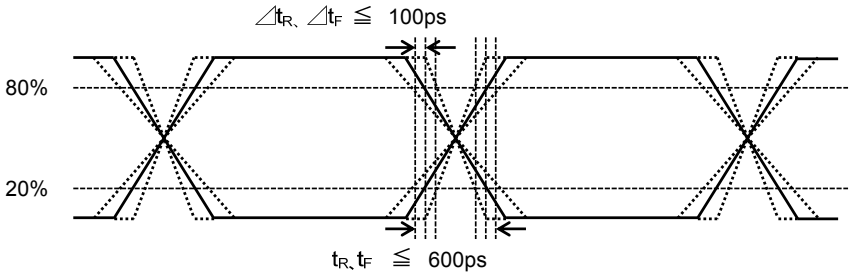
8.2.1. DC Characteristics

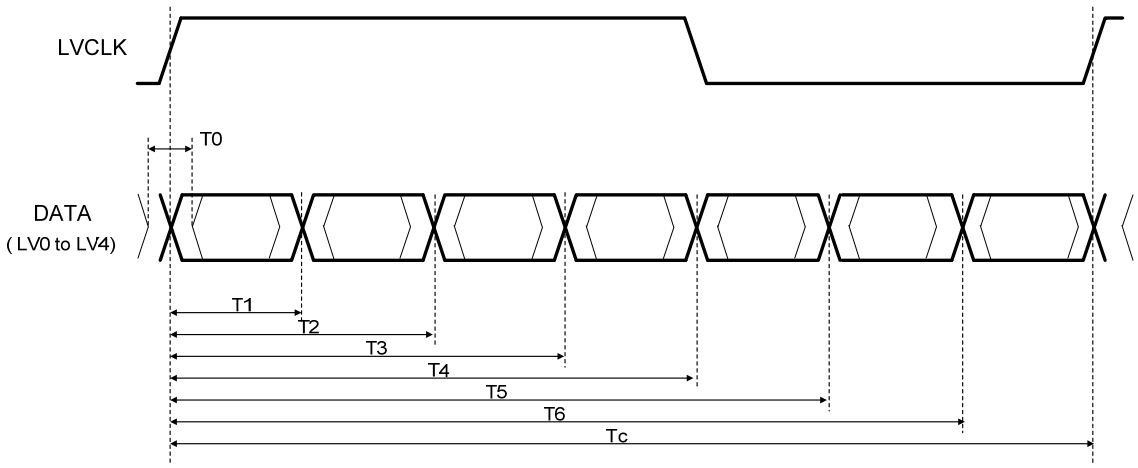
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD1IF		1.62	1.8	1.98	V
Differential Voltage Range	VID		100		300	mV
Differential Voltage Deviation (Between Lanes)	⊿VID		-10		10	%
Input voltage range	VI		500		1300	mV
Common Voltage	VIC		600		1200	mV
Common Voltage Deviation (Between Lanes)	⊿VIC		-100		100	mV



8.2.2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Pulse Period	Tc		24.69			ns
Clock Data Rise Time	t_R	20% to 80% At Panel Input			600	ps
Clock Data Fall Time	t_F	80% to 20% At Panel Input			600	ps
Clock Data Fall/Rise Time Deviation (Between Lanes)	Δt_R, Δt_F				100	ps
Clock Duty	Duty	Tc(H) / Tc	40		60	%
Data Setup Time	TSKEW		540		1000	ps
Delay of serial bit data (n:0 to 6)	Tn		(n/7)Tc-0.265		(n/7)Tc+0.265	ns
Delay of serial bit data 2 (n:0 to 9)	Tn		(n/10)Tc-0.265		(n/10)Tc+0.265	ns

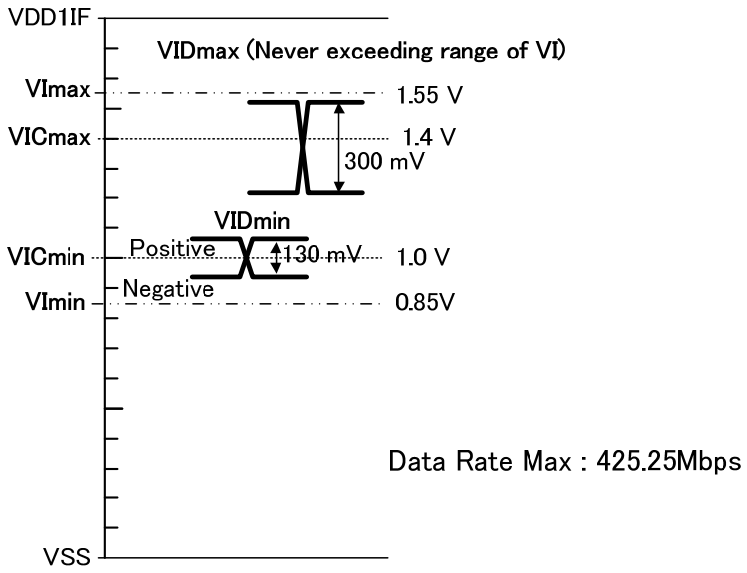




8.3. LVDS Input

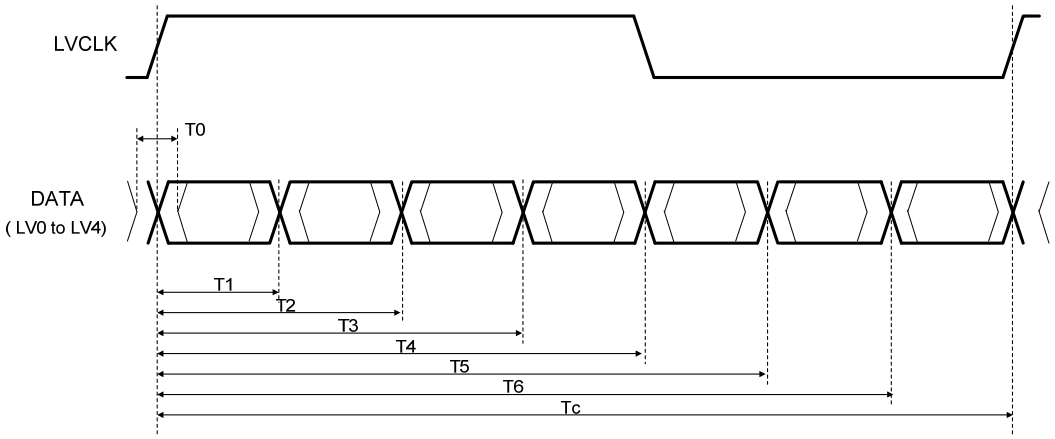
8.3.1. DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD1IF		1.62	1.8	1.98	V
Differential Voltage Range	VID		130		300	mV
Differential Voltage Deviation (Between Lanes)	⊿VID		-10		10	%
Input voltage range	VI		850		1550	mV
Common Voltage	VIC		1000		1400	mV
Common Voltage Deviation (Between Lanes)	⊿VIC		-100		100	mV



8.3.2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Pulse Period	Tc		16.46			ns
Clock Data Rise Time	t_R	20% to 80% At Panel Input			600	ps
Clock Data Fall Time	t_F	80% to 20% At Panel Input			600	ps
Clock Data Fall/Rise Time Deviation (Between Lanes)	Δt_R, Δt_F				100	ps
Clock Duty	Duty	Tc(H) / Tc	40		60	%
Data Setup Time	TSKEW				1000	ps
Delay of serial bit data (n:0 to 6)	Tn		(n/7)Tc-0.535		(n/7)Tc+0.535	ns
Delay of serial bit data 2 (n:0 to 9)	Tn		(n/10)Tc-0.535		(n/10)Tc+0.535	ns



8.4. Power Consumption (Tentative)

Power consumption in display

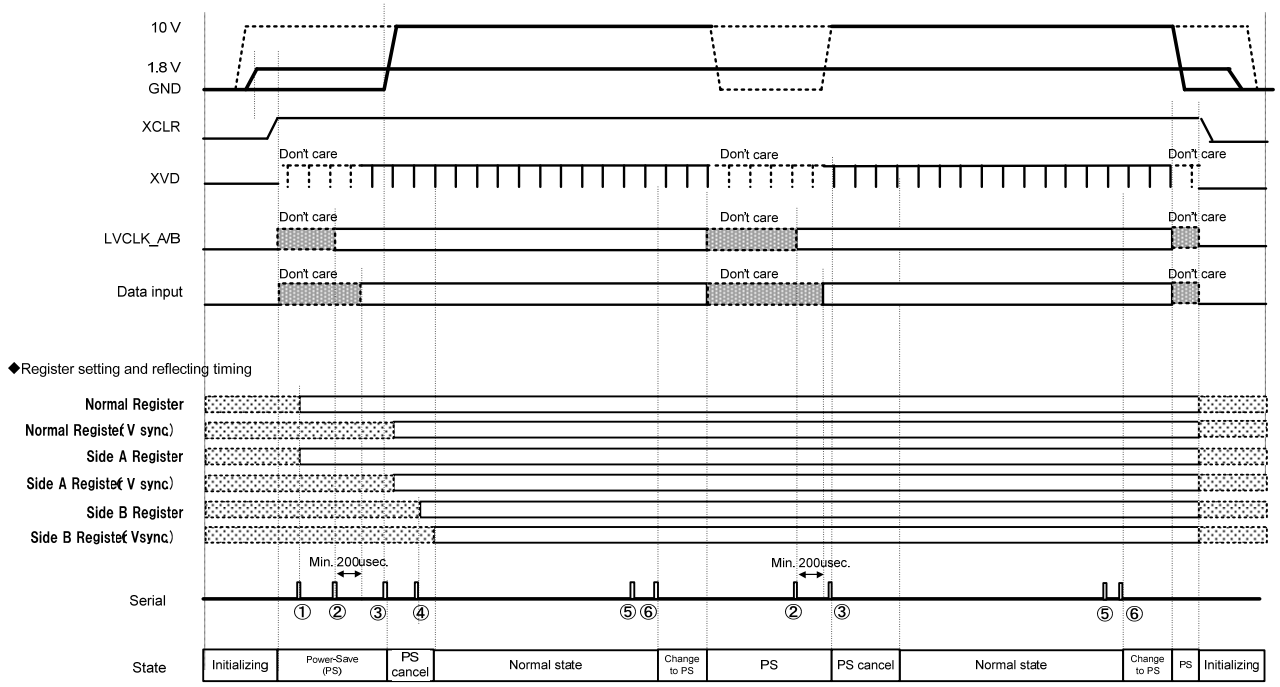
Item	Symbol	Condition	Luminance					Unit
			1000	500	200	120	Stand-by	cd/m^2
VDD1 Power consumption	PDD1	VDD1=1.8V VDD2=10V LVDS Tpnl = 40℃	24				0.1	mW
VDD1IF Power consumption	PDD1IF		57				0	mW
VDD2+VCCP Power consumption	PDD2		640	379	222	180	0	mW
Total	PDDTTL		720	459	303	261	0.1	mW

Note) White raster display, Clock frequency = 40.5MHz, Frame rate = 60Hz

9. Power Supply Sequence

Power supply sequence shown in below should be followed to avoid panel breakdown caused by excessive current flow into the internal circuit.

9.1. Sequence Diagram



	Serial Input					
Address	Setting①	Setting②	Setting③	Setting④	Setting⑤	Setting⑥
0x00	–	0x4D	0x4F	–	0x4D	0x4C
0x01～0x14 0x6B～0x81 (Normal Register)	※	–	–	–	–	–
0x15～0x6A (Side A Register)	※	–	–	–	–	–
0x15～0x6A (Side B Register)	–	–	–	※	–	–

※Setting values should be submitted separately.

9.2. Power On Sequence

1. Set XCLR to low and turn on 1.8V power supply, then the panel should be initialized.
2. After completion of 1.8 V power supply rising, set XCLR to high, then the panel changes to PS (Power-saving) mode within 16 msec.
3. Executing serial setting ①. (Sending data, from 0x01 to 0x81.)
4. Executing PS0 (Power-saving)-off by serial setting ②, 200usec later, it can be valid to input data .
5. Executing PS1 (Power-saving)-off by serial setting ③, then the panel should be in normal state.
6. It is available to input Side B register (setting ④).

*Sequential order of turning on 1.8V and 10V power supplies is no matter.

* Power supply of 10V should be ON before serial setting③.

* In terms of Side A and B register, please refer “10.1.5 Register Structure (Dual Register Mapping).

9.3. Power Off Sequence

1. By executing serial setting ⑤ and ⑥, set both PS1 and PS0 to be ON.

2. After PS (Power Saving) mode transition, set XCLR to low and turn off 1.8V power supply. Turn off 10V power supply after PS (Power Saving) mode transition.

*Sequential order of serial setting ⑤ and ⑥ is no matter, even same time setting is acceptable.

*Sequential order of turning off 1.8V and 10V power supplies is no matter. Even same time transition is acceptable.

*1.8V power supply should be Low after XCLR status set to Low.

10. Description of Function

10.1. Serial Communication

10.1.1. Register Map of Serial Control

Address	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Default
0x00	RGB_YCB	YCB_DEC	YCB_CMPLE	YCB_OFSET	DWN	RGT	PS1	PS0	0x4C
0x01	0	T_SLOPE[1:0]		YCB_P	CALSEL[1:0]		LVDS_MAP	MCLKPOL	0x00
0x02	0	0	ORBIT_H[5:0]						0x00
0x03	1	0	ORBIT_V[5:0]						0x80
0x04	PN_POL[1:0]		PINSWP[1:0]		PRTSWP	IFSW			0x03
0x05	0	0	0	FORMAT_SEL_DATA	DITHEREN	0	0	0	0x08
0x06	VD_POL	HD_POL	0	0	0	OTPCALDAC_REGEN	0	OTPDG_REGEN	0x00
0x07	VD_FILTER	HD_FILTER	0	1	0	C_SLOPE[2:0]			0x10
0x08	0	0	0	0	1	1	0	0	0x0C
0x09	0	0	0	0	0	0	0	REF_MAPSEL	0x00
0x0A	0	0	0	0	0	0	0	MAPWRITE_SEL	0x00
0x0B	0	0	0	0	0	0	0	RD_MAPSEL	0x00
0x0C	0	RD_SEL[6:0]							0x00
0x0D	MAPRD_DATA[7:0]								0x00
0x0E	0	0	0	0	0	0	0	0	0x00
0x0F	0	1	0	0	0	1	0	0	0x44
0x10	0	0	0	0	0	0	0	0	0x00
0x11	0	0	0	0	0	WB_CALEN	L_SEAMLESSEN	L_AT_CALEN	0x00
0x12	0	0	1	0	1	0	0	0	0x28
0x13	0	REQUEST_LV[6:0]							0x0F
0x14	0	0	0	0	0	0	0	0	0x00
0x15	0	DRGAMMA1[6:0]							0x00
0x16	DRGAMMA2[7:0]								0x00
0x17	DRGAMMA3[7:0]								0x00
0x18	DRGAMMA4[7:0]								0x00
0x19	DRGAMMA5[7:0]								0x00
0x1A	DRGAMMA6[7:0]								0x00
0x1B	0	DRGAMMA7[6:0]							0x00
0x1C	0	DGGAMMA1[6:0]							0x00
0x1D	DGGAMMA2[7:0]								0x00
0x1E	DGGAMMA3[7:0]								0x00
0x1F	DGGAMMA4[7:0]								0x00
0x20	DGGAMMA5[7:0]								0x00
0x21	DGGAMMA6[7:0]								0x00
0x22	0	DGGAMMA7[6:0]							0x00
0x23	0	DBGAMMA1[6:0]							0x00
0x24	DBGAMMA2[7:0]								0x00
0x25	DBGAMMA3[7:0]								0x00
0x26	DBGAMMA4[7:0]								0x00
0x27	DBGAMMA5[7:0]								0x00
0x28	DBGAMMA6[7:0]								0x00
0x29	0	DBGAMMA7[6:0]							0x00
0x2A	VDR120MODE	OESW	FORMAT_SEL_V[1:0]		0	0	0	FORMAT_SEL_H	0x00
0x2B	0	0	0	0	0	0	0	CONT[8]	0x01
0x2C	CONT[7:0]								0x00
0x2D	RCONT[7:0]								0x80
0x2E	GCONT[7:0]								0x80
0x2F	BCONT[7:0]								0x80
0x30	BRT[7:0]								0x80
0x31	RBRT[7:0]								0x80

Address	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Default
0x32	GBRT[7:0]								0x80
0x33	BBRT[7:0]								0x80
0x34	0	0	H_ACT_D[9:8]		0	0	H_ACT_U[9:8]		0x20
0x35	H_ACT_U[7:0]								0x0C
0x36	H_ACT_D[7:0]								0x8C
0x37	0	V_ACT_D[10:8]			0	V_ACT_U[10:8]			0x30
0x38	V_ACT_U[7:0]								0x1A
0x39	V_ACT_D[7:0]								0xDA
0x3A	0	0	DE_D[9:8]		0	0	DE_U[9:8]		0x20
0x3B	DE_U[7:0]								0x07
0x3C	DE_D[7:0]								0x91
0x3D	0	WSST1_D[10:8]			0	WSST1_U[10:8]			0x00
0x3E	WSST1_U[7:0]								0x0F
0x3F	WSST1_D[7:0]								0x10
0x40	0	WSST2_D[10:8]			0	WSST2_U[10:8]			0x33
0x41	WSST2_U[7:0]								0x93
0x42	WSST2_D[7:0]								0x94
0x43	CALDAC[8:1]								0x55
0x44	0	0	0	0	0	0	0	CALDAC[0]	0x01
0x45	0	0	0	0	0	0	0	0	0x00
0x46	0	0	0	0	0	0	WSEN1_U[9:8]		0x00
0x47	WSEN1_U[7:0]								0x57
0x48	WSEN1_W[7:0]								0x08
0x49	0	0	0	0	0	0	WSEN2_U[9:8]		0x02
0x4A	WSEN2_U[7:0]								0x7D
0x4B	WSEN2_W[7:0]								0x08
0x4C	0	0	0	0	0	0	WSEN3_U[9:8]		0x00
0x4D	WSEN3_U[7:0]								0x21
0x4E	WSEN3_W[7:0]								0x08
0x4F	0	0	DSEN_W[9:8]		0	0	DSEN_U[9:8]		0x20
0x50	DSEN_U[7:0]								0x69
0x51	DSEN_W[7:0]								0x34
0x52	0	0	VCK_W[9:8]		0	0	VCK_U[9:8]		0x00
0x53	VCK_U[7:0]								0x01
0x54	VCK_W[7:0]								0x78
0x55	0	0	AZEN_D[9:8]		0	0	AZEN_U[9:8]		0x20
0x56	AZEN_U[7:0]								0x25
0x57	AZEN_D[7:0]								0x76
0x58	0	0	0	0	0	0	0	0	0x00
0x59	SIGSELOFS_U[3:0]				SIGSELREF_U[3:0]				0x01
0x5A	SIGSELREF_W[7:0]								0x36
0x5B	SIGSELOFS_W[7:0]								0x36
0x5C	SIGSEL_W[7:0]								0x2C
0x5D	1	1	0	0	0	0	0	0	0xC0
0x5E	SELOFS_U[3:0]				SELREF_U[3:0]				0x22
0x5F	SELREF_W[7:0]								0x2E
0x60	SELOFS_W[7:0]								0x2E
0x61	0	0	0	0	SEL_U[3:0]				0x02
0x62	SEL_W[7:0]								0x24
0x63	0	0	0	0	1	0	1	0	0x0A
0x64	0	0	0	0	0	0	0	0	0x00
0x65	0	0	0	0	0	0	0	0	0x00
0x66	0	0	0	0	0	0	0	0	0x00
0x67	0	0	0	0	0	0	0	0	0x00
0x68	0	0	0	0	0	0	0	0	0x00
0x69	0	0	0	0	0	0	0	0	0x00
0x6A	0	0	0	0	0	0	0	0	0x00

Address	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Default
0x6B	0	0	0	0	0	0	0	0	0x00
0x6C	0	0	0	1	0	0	0	0	0x10
0x6D	0	0	1	0	1	1	0	0	0x2C
0x6E	1	1	1	1	1	1	1	1	0xFF
0x6F	0	0	0	0	0	0	0	0	0x00
0x70	0	0	0	0	0	0	0	0	0x00
0x71	0	0	0	0	0	0	0	0	0x00
0x72	0	0	0	0	0	0	0	0	0x00
0x73	0	0	0	0	0	0	0	0	0x00
0x74	0	0	0	0	0	0	0	0	0x00
0x75	0	0	0	0	0	0	0	0	0x00
0x76	0	0	0	0	0	0	0	0	0x00
0x77	0	0	0	0	0	0	0	1	0x01
0x78	0	0	1	0	0	0	1	1	0x23
0x79	0	1	0	0	0	1	0	1	0x45
0x7A	0	1	1	0	0	1	1	1	0x67
0x7B	1	0	0	0	1	0	0	1	0x89
0x7C	1	0	1	0	1	0	1	1	0xAB
0x7D	0	0	0	0	0	0	0	0	0x00
0x7E	0	0	0	0	0	0	0	0	0x00
0x7F	0	1	0	1	0	1	1	0	0x56
0x80	0	0	0	0	0	0	0	RD_ON	0x00
0x81	RD_ADDR[7:0]								0x00

* Setting values should be submitted separately.

10.1.2. Description of Register

Address	DATA	Register	R/W	Synchronized with VSync	Function	Related Items
0x00	[0]	PS0	RW		Power save 0 mode 0:Power save 0 on 1:Power save 0 off	9.2 9.3
	[1]	PS1	RW		Power save 1 mode 0:Power save 1 on 1:Power save 1 off	9.2 9.3
	[2]	RGT	RW		Selection of rightward / leftward scan	10.6
	[3]	DWN	RW		Selection of upward / downward scan	10.6
	[4]	YCB_OFSET	RW		Offset selection of YCbCr	10.2
	[5]	YCB_CMPLE	RW		interpolation selection of 4:2:2 CbCr input	10.2
	[6]	YCB_DEC	RW		Selection of YCbCr / YPbPr conversion	10.2
	[7]	RGB_YCB	RW		Selection of RGB / YCbCr (YPbPr) format	10.2
0x01	[0]	MCLKPOL	RW		Maser clock polarity 1b0: Negative (Default) 1b1: Positive	—
	[1]	LVDS_MAP	RW		LVDS data map selection	10.2
	[3:2]	CALSEL	RW		VCAL(pin# 55) output selection	10.7
	[4]	YCB_P	RW		Selection of YCbCr (YPbPr) input pattern	10.2
	[6:5]	T_SLOPE	RW		Gain selection of Temperature compensation	10.7
0x02	[5:0]	ORBIT_H	RW	○	Horizontal orbit adjustment	10.14
0x03	[5:0]	ORBIT_V	RW	○	Vertical orbit adjustment	10.14
0x04	[2:0]	IFSW	RW		Switching of Interface Mode	10.2
	[3]	PRTSWP	RW		Switching sequential order of Input Port	10.3
	[5:4]	PINSWP	RW		Switching sequential order of Input Lane	10.3
	[7:6]	PN_POL	RW		Switching Polarity of Input Lane.	10.3
0x05	[3]	DITHEREN	RW		Dithering processing or invalid.	10.13
	[4]	FORMAT_SEL_DATA	RW		YCbCr format selection, (444 or 422)	10.2
0x06	[0]	OTPDG_REGEN	RW		White chromaticity adjustment	10.11
	[2]	OTPCALDAC_REGEN	RW		Luminance adjustment	10.10
	[6]	HD_POL	RW		Hsync polarity 0: Negative 1: Positive	—
	[7]	VD_POL	RW		Vsync polarity 0: Negative 1: Positive	—
0x07	[2:0]	C_SLOPE	RW		Speed of luminance transition	10.9
	[6]	HD_FILTER	RW		HSYNC filter width 0: 1MCLK 1: 3MCLK	—
	[7]	VD_FILTER	RW		VSYNC filter width 0: 1MCLK 1: 3MCLK	—

Address	DATA	Register	R/W	Synchronized with VSync	Function	Related Items
0x09	[0]	REF_MAPSEL	RW	○	Register map selection, A or B.	10.1.5
0x0A	[0]	MAPWRITE_SEL	RW		Write register map selection	10.1.5
0x0B	[0]	RD_MAPSEL	RW		Read register map selection	10.1.5
0x0C	[6:0]	RD_SEL	RW		Read register address for dual map	10.1.5
0x0D	[7:0]	MAPRD_DATA	R		Read register value for dual map	10.1.5
0x11	[0]	L_AT_CALEN	RW		Validation for Direct Luminance change and Luminance transition speed control.	10.8 10.9
	[1]	L_SEAMLESSEN	RW		Luminance Change	10.9
	[2]	WB_CALEN	RW		Auto-Adjustment of White Balance	10.8
0x13	[6:0]	REQUEST_LV	RW	○	Luminance for Direct setting	10.8
0x15	[6:0]	DRGAMMA1	RW	○	Digital Gamma Red 8 gray level adjustment	10.12
0x16	[7:0]	DRGAMMA2	RW	○	Digital Gamma Red 16 gray level adjustment	10.12
0x17	[7:0]	DRGAMMA3	RW	○	Digital Gamma Red 32 gray level adjustment	10.12
0x18	[7:0]	DRGAMMA4	RW	○	Digital Gamma Red 64 gray level adjustment	10.12
0x19	[7:0]	DRGAMMA5	RW	○	Digital Gamma Red 96 gray level adjustment	10.12
0x1A	[7:0]	DRGAMMA6	RW	○	Digital Gamma Red 128 gray level adjustment	10.12
0x1B	[6:0]	DRGAMMA7	RW	○	Digital Gamma Red 192 gray level adjustment	10.12
0x1C	[6:0]	DGGAMMA1	RW	○	Digital Gamma Green 8 gray level adjustment	10.12
0x1D	[7:0]	DGGAMMA2	RW	○	Digital Gamma Green 16 gray level adjustment	10.12
0x1E	[7:0]	DGGAMMA3	RW	○	Digital Gamma Green 32 gray level adjustment	10.12
0x1F	[7:0]	DGGAMMA4	RW	○	Digital Gamma Green 64 gray level adjustment	10.12
0x20	[7:0]	DGGAMMA5	RW	○	Digital Gamma Green 96 gray level adjustment	10.12
0x21	[7:0]	DGGAMMA6	RW	○	Digital Gamma Green 128 gray level adjustment	10.12
0x22	[6:0]	DGGAMMA7	RW	○	Digital Gamma Green 192 gray level adjustment	10.12
0x23	[6:0]	DBGAMMA1	RW	○	Digital Gamma Blue 8 gray level adjustment	10.12
0x24	[7:0]	DBGAMMA2	RW	○	Digital Gamma Blue 16 gray level adjustment	10.12
0x25	[7:0]	DBGAMMA3	RW	○	Digital Gamma Blue 32 gray level adjustment	10.12
0x26	[7:0]	DBGAMMA4	RW	○	Digital Gamma Blue 64 gray level adjustment	10.12
0x27	[7:0]	DBGAMMA5	RW	○	Digital Gamma Blue 96 gray level adjustment	10.12
0x28	[7:0]	DBGAMMA6	RW	○	Digital Gamma Blue 128 gray level adjustment	10.12
0x29	[6:0]	DBGAMMA7	RW	○	Digital Gamma Blue 192 gray level adjustment	10.12
0x2A	[0]	FORMAT_SEL_H	RW		Horizontal resolution selection	10.4
	[5:4]	FORMAT_SEL_V	RW		Vertical resolution selection	10.4
	[6]	OESW	RW		120Hz scan mode selection	10.5
	[7]	VDR120MODE	RW-		Validation of 120Hz Mode	10.5

Address	DATA	Register	R/W	Synchronized with VSync	Function	Related Items
0x2B	[0]	CONT[8]	RW	○	Contrast Adjustment	10.11.1
0x2C	[7:0]	CONT[7:0]				
0x2D	[7:0]	RCONT	RW	○	Red sub-contrast adjustment	10.11.1
0x2E	[7:0]	GCONT	RW	○	Green sub-contrast adjustment	10.11.1
0x2F	[7:0]	BCONT	RW	○	Blue sub-contrast adjustment	10.11.1
0x30	[7:0]	BRT	RW	○	Brightness adjustment	10.11.2
0x31	[7:0]	RBRT	RW	○	Red sub-contrast adjustment	10.11.2
0x32	[7:0]	GBRT	RW	○	Green sub-contrast adjustment	10.11.2
0x33	[7:0]	BBRT	RW	○	Blue sub-contrast adjustment	10.11.2
0x34	[1:0]	H_ACT_U[9:8]	RW		Horizontal active area start position (MCLK counts)※	10.4
0x35	[7:0]	H_ACT_U[7:0]				
0x34	[5:4]	H_ACT_D[9:8]	RW		Horizontal active area end position (MCLK counts)※	10.4
0x36	[7:0]	H_ACT_D[7:0]				
0x37	[1:0]	V_ACT_U[9:8]	RW		Vertical active area start position (HSYNC counts)※	10.4
0x38	[7:0]	V_ACT_U[7:0]				
0x37	[5:4]	V_ACT_D[9:8]	RW		Vertical active area end position (HSYNC counts)	10.4
0x39	[7:0]	V_ACT_D[7:0]				
0x3A	[1:0]	DE_U[9:8]	RW		Horizontal signal start position (MCLK counts)※	10.4
0x3B	[7:0]	DE_U[7:0]				
0x3A	[5:4]	DE_D[9:8]	RW		Horizontal signal end position (MCLK counts)※	10.4
0x3C	[7:0]	DE_D[7:0]				
0x3D	[2:0]	WSST1_U[10:8]	RW		Lighting start pulse rise position (HSYNC counts)※	10.4
0x3E	[7:0]	WSST1_U[7:0]				
0x3D	[6:4]	WSST1_D[10:8]	RW		Lighting end pulse fall position (HSYNC counts)※	10.4
0x3F	[7:0]	WSST1_D[7:0]				
0x41	[2:0]	WSST2_U[10:8]	RW		Lighting end pulse rise position (HSYNC counts)※	10.4
0x3E	[7:0]	WSST2_U[7:0]				
0x40	[6:4]	WSST2_D[10:8]	RW		Lighting end pulse fall position (HSYNC counts)※	10.4
0x42	[7:0]	WSST2_D[7:0]				
0x43	[7:0]	CALDAC[8:1]	RW	○	Luminance Calibration setting	10.10
0x44	[0]	CALDAC[0]				
0x46	[1:0]	WSEN1_U[9:8]	RW		Timing setting register※	10.4
0x47	[7:0]	WSEN1_U[7:0]				

Address	DATA	Register	R/W	Synchronized with VSync	Function	Related Items
0x48	[7:0]	WSEN1_W[7:0]	RW		Timing setting register※	10.4
0x49	[1:0]	WSEN2_U[9:8]	RW		Timing setting register※	10.4
0x4A	[7:0]	WSEN2_U[7:0]				
0x4B	[7:0]	WSEN2_W[7:0]	RW		Timing setting register※	10.4
0x4C	[1:0]	WSEN3_U[9:8]	RW		Timing setting register※	10.4
0x4D	[7:0]	WSEN3_U[7:0]				
0x4E	[7:0]	WSEN3_W[7:0]	RW		Timing setting register※	10.4
0x4F	[1:0]	DSEN_U[9:8]	RW		Timing setting register※	10.4
0x50	[7:0]	DSEN_U[7:0]				
0x4F	[5:4]	DSEN_W[9:8]	RW		Timing setting register※	10.4
0x51	[7:0]	DSEN_W7:0]				
0x52	[1:0]	VCK_U[9:8]	RW		Timing setting register※	10.4
0x53	[7:0]	VCK_U[7:0]				
0x52	[5:4]	VCK_W[9:8]	RW		Timing setting register※	10.4
0x54	[7:0]	VCK_W7:0]				
0x55	[1:0]	AZEN_U[9:8]	RW		Timing setting register※	10.4
0x56	[7:0]	AZEN_U[7:0]				
0x55	[5:4]	AZEN_W[9:8]	RW		Timing setting register※	10.4
0x57	[7:0]	AZEN_W7:0]				
0x59	[3:0]	SIGSELREF_U	RW		Timing setting register※	10.4
	[7:4]	SIGSELOFS_U	RW		Timing setting register※	10.4
0x5A	[7:0]	SIGSELREF_W	RW		Timing setting register※	10.4
0x5B	[7:0]	SIGSELOFS_W	RW		Timing setting register※	10.4
0x5C	[7:0]	SIGSEL_W	RW		Timing setting register※	10.4
0x5E	[3:0]	SELREF_U	RW		Timing setting register※	10.4
	[7:4]	SELOFS_U	RW		Timing setting register※	10.4
0x5F	[7:0]	SELREF_W	RW		Timing setting register※	10.4
0x60	[7:0]	SELOFS_W	RW		Timing setting register※	10.4
0x61	[3:0]	SEL_U	RW		Timing setting register※	10.4
0x62	[7:0]	SEL_W	RW		Timing setting register※	10.4
0x80	[0]	RD_ON	RW		Register read on / off	10.1.4
0x81	[7:0]	RD_ADDR	RW		Read register address	10.1.4

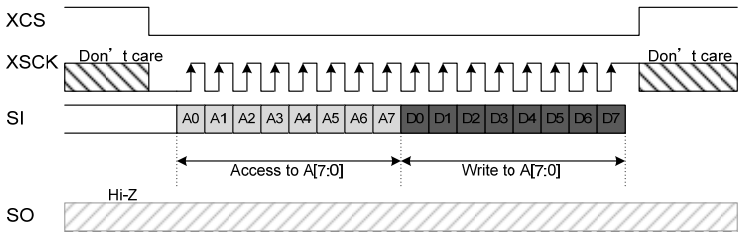
※Setting values should be submitted separately.

10.1.3. Serial I/F Write Access

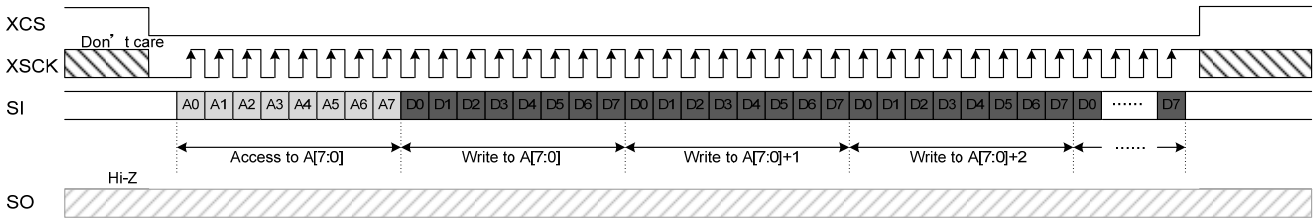
Serial communication of normal / burst transfer, LSB first is supported for write operation.

Input an address of the target register from SI (pin #10), then input data to the address.

The timing of write access is shown in below.



Write Access Normal Transfer (LSB First)



Write Access Burst Transfer (LSB First)

・Data capturing starts at XCS fall position.

・During XCS is low status, Data should be captured at 16th XCS rise position.

・The first 8bit data are recognized as the address, and next coming 8bit are recognized as the write value.

・During XCS is low status, Data can't be captured and are invalid If the number of XCS pulse is less than 15 times.

・During XCS is low status, if changing to burst transfer mode and data capturing for address A should complete along with 16^{th} XSCK rising timing. After 16^{th} XSCK pulse, , from 17th to 24th data should be captured for address A+1, from 25th to 32nd data for address A+2. After that, such increment of the address is automatically applied.

・Only 8xN (N is an integer greater than or equal to 2) data should be captured If the number of XCS pulse is not equal to the multiple of 8.

10.1.4. Serial I/F Read Access

In Read mode, serial communication support both normal and burst transfer mode, based on LSB first mode.

◆Register Settings

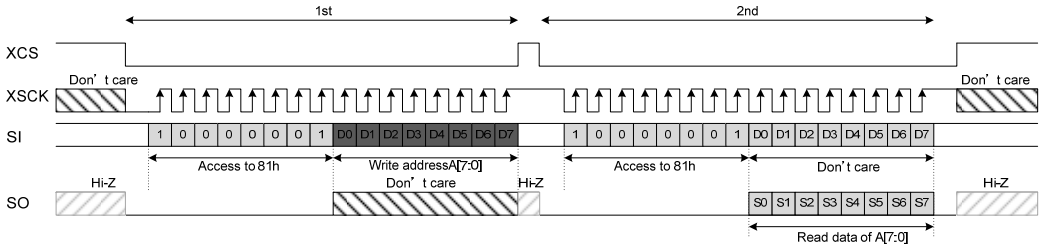
Address	DATA	Register name	Function
0x80	[0]	RD_ON	Register read on / off 0: Off (Default) 1: On
0x81	[7:0]	RD_ADDR	Register read address setting

Setting "RD_ON" to 1, and then execute 2 times serial communication.

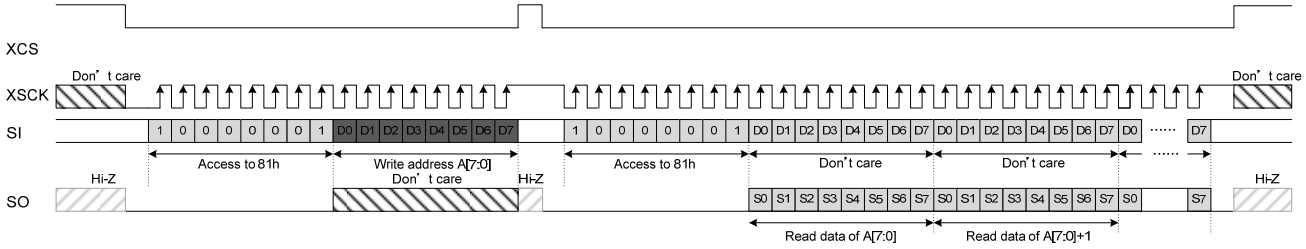
1st serial communication: Write the address of the target register to "RD_ADDR".

2nd serial communication: Read the data of the target register from SO pin (#11) after accessing to the "RD_ADDR".

The timing of read access is shown in below.



Read Access Normal Transfer (LSB First)

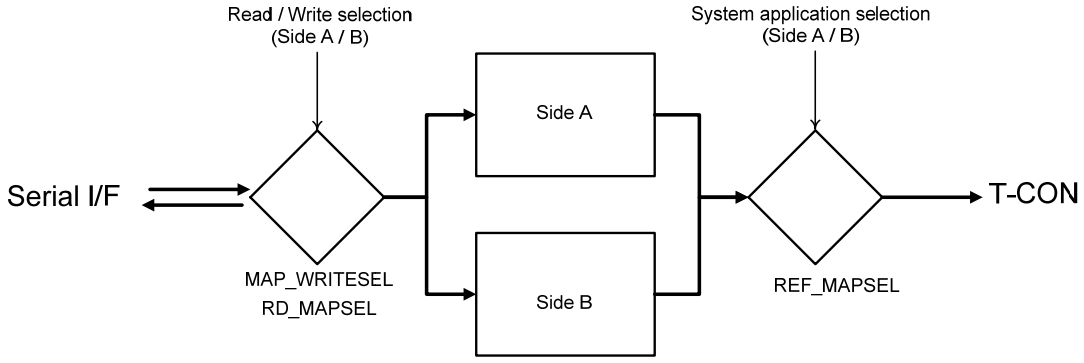


Read Access Burst Transfer (LSB First)

Unless XCS status is high, transfer mode is recognized as burst and the target address should automatically be incremented for every 8 data.

10.1.5. Register Structure (Dual Register Mapping)

This module has the dual register mapping structure which enables register changing without being attention to vertical blanking timing. The dual register can switch display setting with just one frame unit by storage different setting data for each Side A and B register.



・The dual register mapping structure is valid for the registers in address from 0x15 to 0x6A.

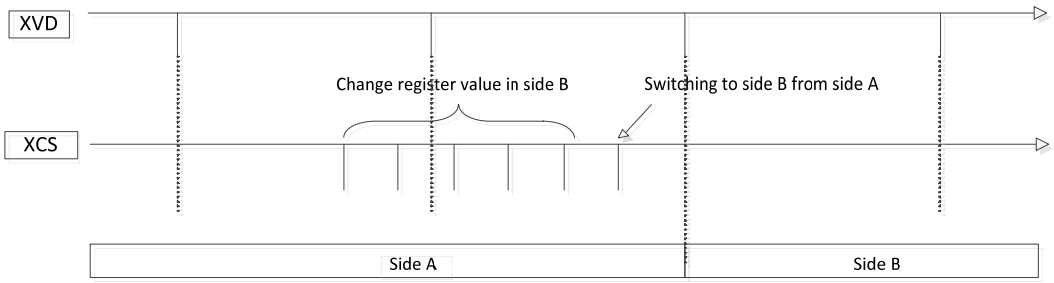
・The registers in the side (A or B) which is not applied to the system can be changed without affecting to the display image.

・Maintain different register contents in both sides (A and B) allows to immediately change register contents even during operation.

◆Register setting

Address	DATA	Register	Function
0x09	[0]	REF_MAPSEL	Dual register map selection 0: Side A 1: Side B
0x0A	[0]	MAPWRITE_SEL	Write register map selection 0: Side A 1: Side B
0x0B	[0]	RD_MAPSEL	Read register map selection 0: Side A 1: Side B
0x0C	[6:0]	RD_SEL	Read register address for dual map
0x0D	[7:0]	MAPRD_DATA	Read register value for dual map

◆Register setting changing sequence



10.1.6. Serial I/F Access for the Dual Mapping Structure

◆Write Access

Setting “MAP_WRITE_SEL” appropriately (1b0: side A, 1b1: side B) and execute the write access following 10.1.3 Serial I/F Write Access procedure.

◆Read Access

Setting “RD_MAPSEL” appropriately (0: side A, 1: side B).

Write the address of target register to “RD_SEL”. Pay attention that valid register address has to take account off-set from writing register address. The off-set is minus 21, so valid register address should be minus 21 from writing register address. Please refer to “◆Register address” for RD_SEL below.

Read the register value by accessing to “MAPRD_DATA” based on “10.1.4 Serial I/F Read Access procedure”.

◆Register address for RD_SEL

Address		DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Side A	**Side B RD_SEL**								
0x15	**0x00**	0	DRGAMMA1[6:0]						
0x16	**0x01**	DRGAMMA2[7:0]							
0x17	**0x02**	DRGAMMA3[7:0]							
0x18	**0x03**	DRGAMMA4[7:0]							
0x19	**0x04**	DRGAMMA5[7:0]							
0x1A	**0x05**	DRGAMMA6[7:0]							
0x1B	**0x06**	0	DRGAMMA7[6:0]						
0x1C	**0x07**	0	DGGAMMA1[6:0]						
0x1D	**0x08**	DGGAMMA2[7:0]							
0x1E	**0x09**	DGGAMMA3[7:0]							
0x1F	**0x0A**	DGGAMMA4[7:0]							
0x20	**0x0B**	DGGAMMA5[7:0]							
0x21	**0x0C**	DGGAMMA6[7:0]							
0x22	**0x0D**	0	DGGAMMA7[6:0]						
0x23	**0x0E**	0	DBGAMMA1[6:0]						
0x24	**0x0F**	DBGAMMA2[7:0]							
0x25	**0x10**	DBGAMMA3[7:0]							
0x26	**0x11**	DBGAMMA4[7:0]							
0x27	**0x12**	DBGAMMA5[7:0]							
0x28	**0x13**	DBGAMMA6[7:0]							
0x29	**0x14**	0	DBGAMMA7[6:0]						
0x2A	**0x15**	VDR120MODE	OESW	FORMAT_SEL_V[1:0]		0	0	0	FORMAT_SEL_H
0x2B	**0x16**	0	0	0	0	0	0	0	CONT[8]
0x2C	**0x17**	CONT[7:0]							
0x2D	**0x18**	RCONT[7:0]							
0x2E	**0x19**	GCONT[7:0]							
0x2F	**0x1A**	BCONT[7:0]							
0x30	**0x1B**	BRT[7:0]							
0x31	**0x1C**	RBRT[7:0]							
0x32	**0x1D**	GBRT[7:0]							
0x33	**0x1E**	BBRT[7:0]							
0x34	**0x1F**	0	0	H_ACT_D[9:8]		0	0	H_ACT_U[9:8]	
0x35	**0x20**	H_ACT_U[7:0]							
0x36	**0x21**	H_ACT_D[7:0]							
0x37	**0x22**	0	V_ACT_D[10:8]			0	V_ACT_U[10:8]		
0x38	**0x23**	V_ACT_U[7:0]							

Address		DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Side A	Side B RD_SEL								
0x39	**0x24**	V_ACT_D[7:0]							
0x3A	**0x25**	0	0	DE_D[9:8]		0	0	DE_U[9:8]	
0x3B	**0x26**	DE_U[7:0]							
0x3C	**0x27**	DE_D[7:0]							
0x3D	**0x28**	0	WSST1_D[10:8]			0	WSST1_U[10:8]		
0x3E	**0x29**	WSST1_U[7:0]							
0x3F	**0x2A**	WSST1_D[7:0]							
0x40	**0x2B**	0	WSST2_D[10:8]			0	WSST2_U[10:8]		
0x41	**0x2C**	WSST2_U[7:0]							
0x42	**0x2D**	WSST2_D[7:0]							
0x43	**0x2E**	CALDAC[8:1]							
0x44	**0x2F**	0	0	0	0	0	0	0	CALDAC[0]
0x45	**0x30**	0	0	0	0	0	0	0	0
0x46	**0x31**	0	0	0	0	0	0	WSEN1_U[9:8]	
0x47	**0x32**	WSEN1_U[7:0]							
0x48	**0x33**	WSEN1_W[7:0]							
0x49	**0x34**	0	0	0	0	0	0	WSEN2_U[9:8]	
0x4A	**0x35**	WSEN2_U[7:0]							
0x4B	**0x36**	WSEN2_W[7:0]							
0x4C	**0x37**	0	0	0	0	0	0	WSEN3_U[9:8]	
0x4D	**0x38**	WSEN3_U[7:0]							
0x4E	**0x39**	WSEN3_W[7:0]							
0x4F	**0x3A**	0	0	DSEN_W[9:8]		0	0	DSEN_U[9:8]	
0x50	**0x3B**	DSEN_U[7:0]							
0x51	**0x3C**	DSEN_W[7:0]							
0x52	**0x3D**	0	0	VCK_W[9:8]		0	0	VCK_U[9:8]	
0x53	**0x3E**	VCK_U[7:0]							
0x54	**0x3F**	VCK_W[7:0]							
0x55	**0x40**	0	0	AZEN_D[9:8]		0	0	AZEN_U[9:8]	
0x56	**0x41**	AZEN_U[7:0]							
0x57	**0x42**	AZEN_D[7:0]							
0x58	**0x43**	0	0	0	0	0	0	0	0
0x59	**0x44**	SIGSELOFS_U[3:0]				SIGSELREF_U[3:0]			
0x5A	**0x45**	SIGSELREF_W[7:0]							
0x5B	**0x46**	SIGSELOFS_W[7:0]							
0x5C	**0x47**	SIGSEL_W[7:0]							
0x5D	**0x48**	1	1	0	0	0	0	0	0
0x5E	**0x49**	SELOFS_U[3:0]				SELREF_U[3:0]			
0x5F	**0x4A**	SELREF_W[7:0]							
0x60	**0x4B**	SELOFS_W[7:0]							
0x61	**0x4C**	0	0	0	0	SEL_U[3:0]			
0x62	**0x4D**	SEL_W[7:0]							
0x63	**0x4E**	0	0	0	0	1	0	1	0
0x64	**0x4F**	0	0	0	0	0	0	0	0
0x65	**0x50**	0	0	0	0	0	0	0	0
0x66	**0x51**	0	0	0	0	0	0	0	0
0x67	**0x52**	0	0	0	0	0	0	0	0
0x68	**0x53**	0	0	0	0	0	0	0	0
0x69	**0x54**	0	0	0	0	0	0	0	0
0x6A	**0x55**	0	0	0	0	0	0	0	0

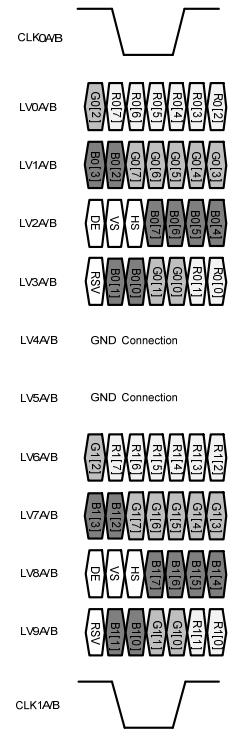
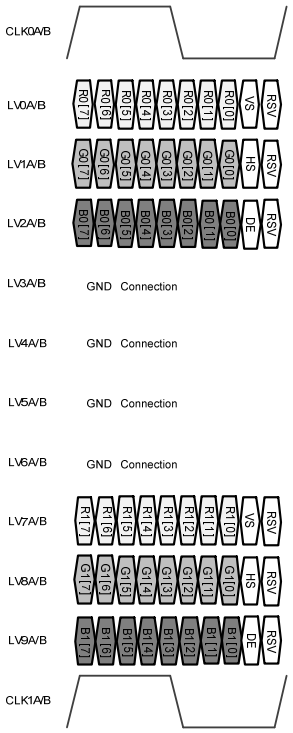
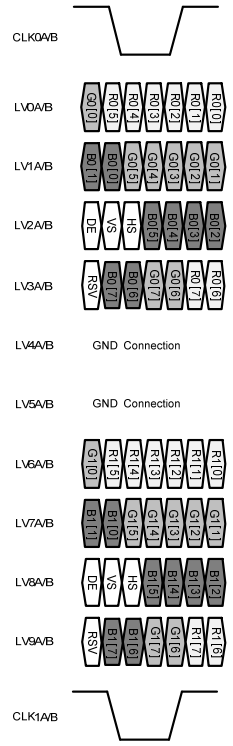
10.2. Video Signal Transfer Format

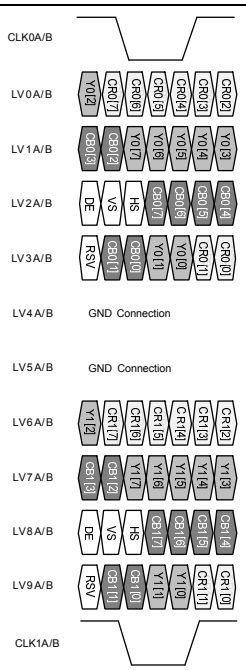
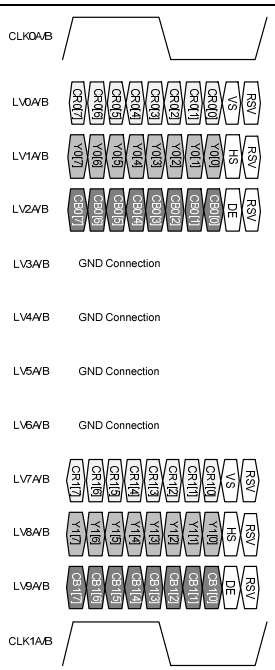
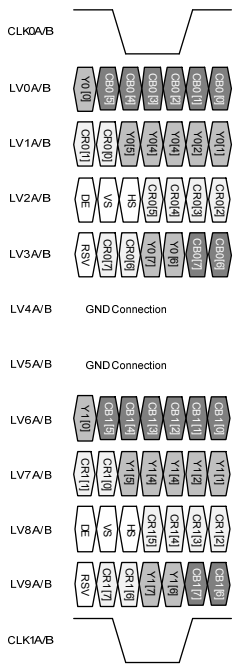
Setting the registers appropriately for the video signal transfer format based on table in below.

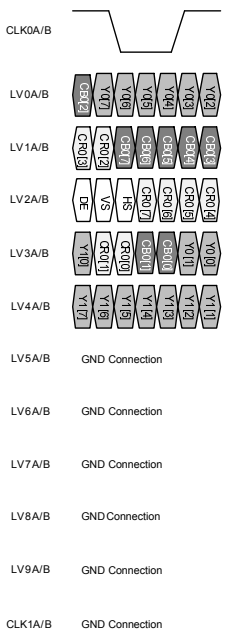
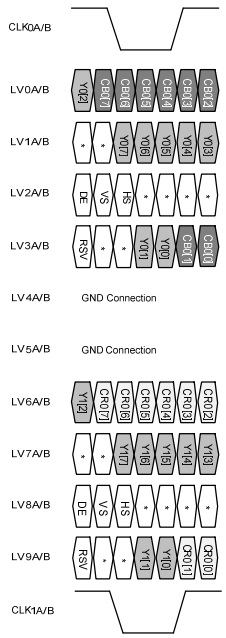
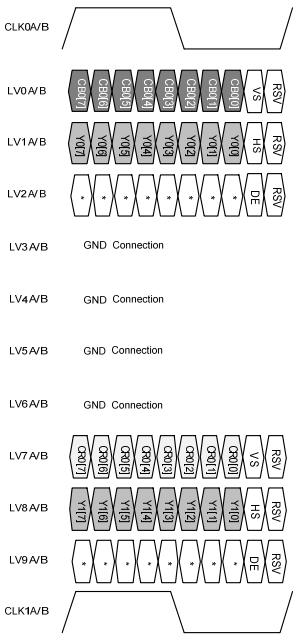
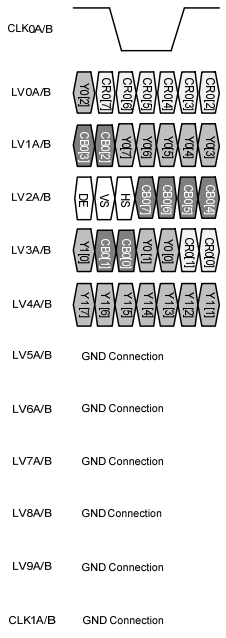
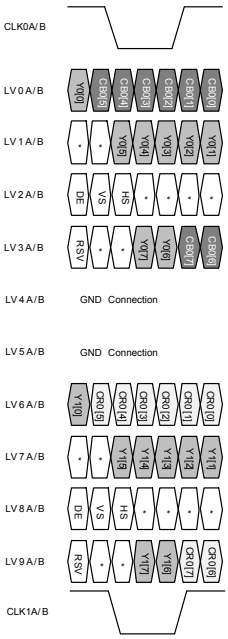
◆Register Settings

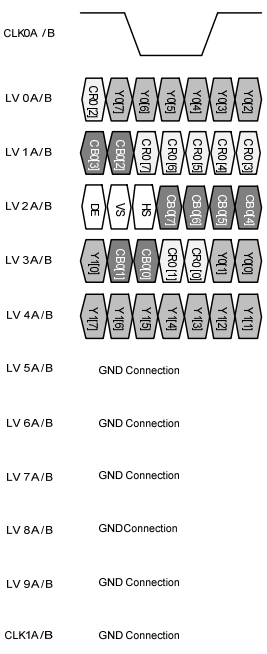
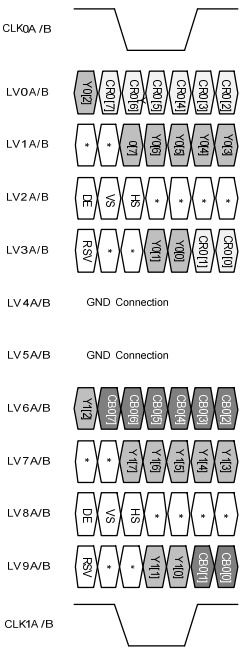
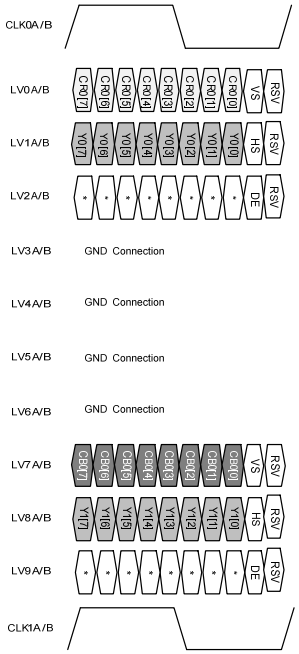
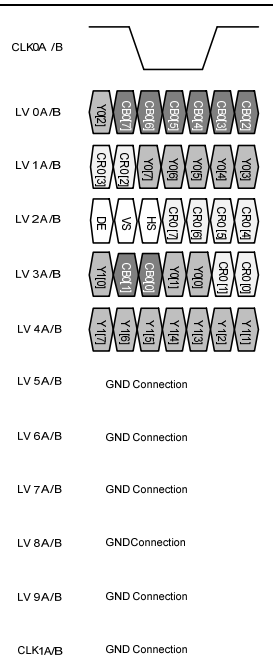
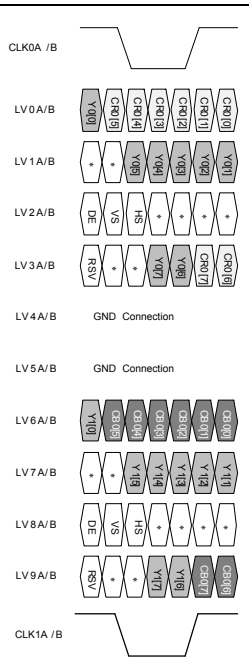
Address	DATA	Register	Function
0x00	[4]	YCB_OFSET	YCbCr Input offset selection 0: Complement on 2 (-128～127) 1: Positive value(0～255)
	[5]	YCB_CMPLE	4:2:2 CbCr input interpolation selection 0: Linear interpolation 1: Preliminary interpolation
	[6]	YCB_DEC	Selection of YCbCr / YPbPr conversion 0: YCbCr (BT. 601) (default) 1: YPbPr (BT. 709)
	[7]	RGB_YCB	Selection of RGB / YCbCr (YPbPr) format 0: RGB (default) 1: YCbCr and YPbPr
0x01	[1]	LVDS_MAP	Selection of LVDS data mapping 0: Based on JEITA 1: Based on VESA
	[4]	YCB_P	Selection of YCbCr (YPbPr) input pattern 0: Cb and Pb first (default) 1: Cr and Pr first
0x04	[2:0]	IFSW	Selection of Interface input mode 000: Reserved（Don't use this mode） 001: Reserved（Don't use this mode） 010: Reserved（Don't use this mode） 011: 4lanes×2 100: 5lanes×1 101: Reserved（Don't use this mode） 110: 3lanes×2 111: Reserved（Don't use this mode）
0x05	[4]	FORMAT_SEL_DATA	YCbCr format selection 0: 4:4:4 (24bit) 1: 4:2:2 (16bit)

◆Register setting and transfer data format in case for YCB_DEC=0. (In case of YCB_DEC=1, Cb should be Pb and Cr shoud be Pr.)

RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes (IFSW=100)	4Lanes (IFSW=011)	3Lanes (IFSW=110)
0	—	—	0			
			1			

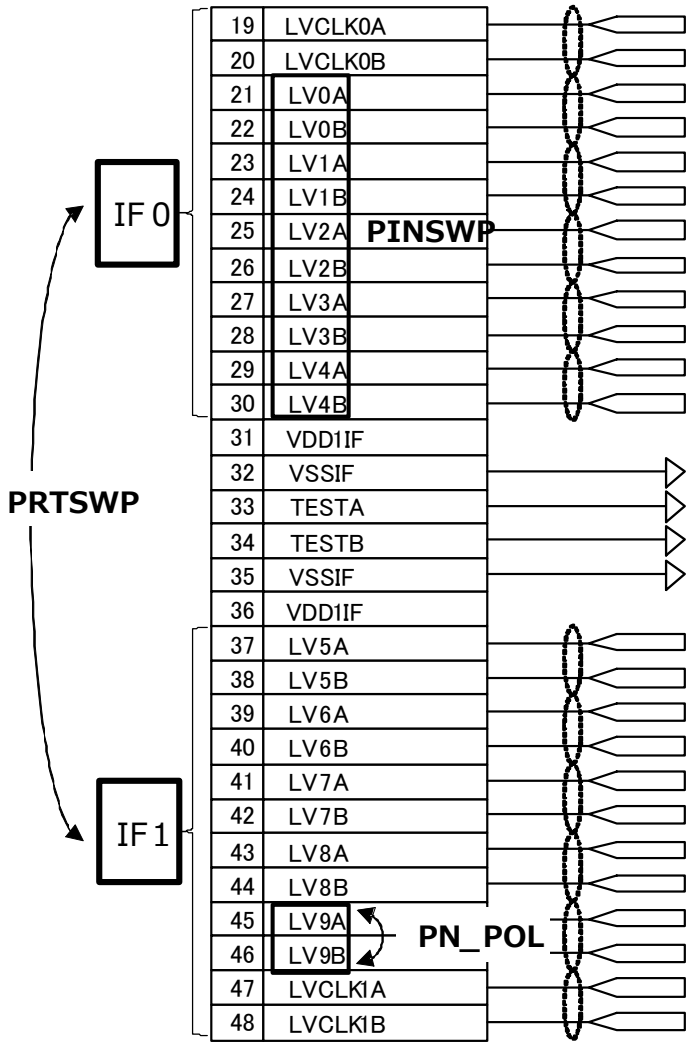
RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes (IFSW=100)	4Lanes (IFSW=011)	3Lanes (IFSW=110)
1	—	0	0			
			1			

RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes (IFSW=100)	4Lanes (IFSW=011)	3Lanes (IFSW=110)
1	0	1	0			
			1			

RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes (IFSW=100)	4Lanes (IFSW=011)	3Lanes (IFSW=110)
1	1	1	0			
			1			

10.3 Swapping function

This function can swap input lanes and their polarity. There are three commands to swap, input port order and input lane order, their polarity.

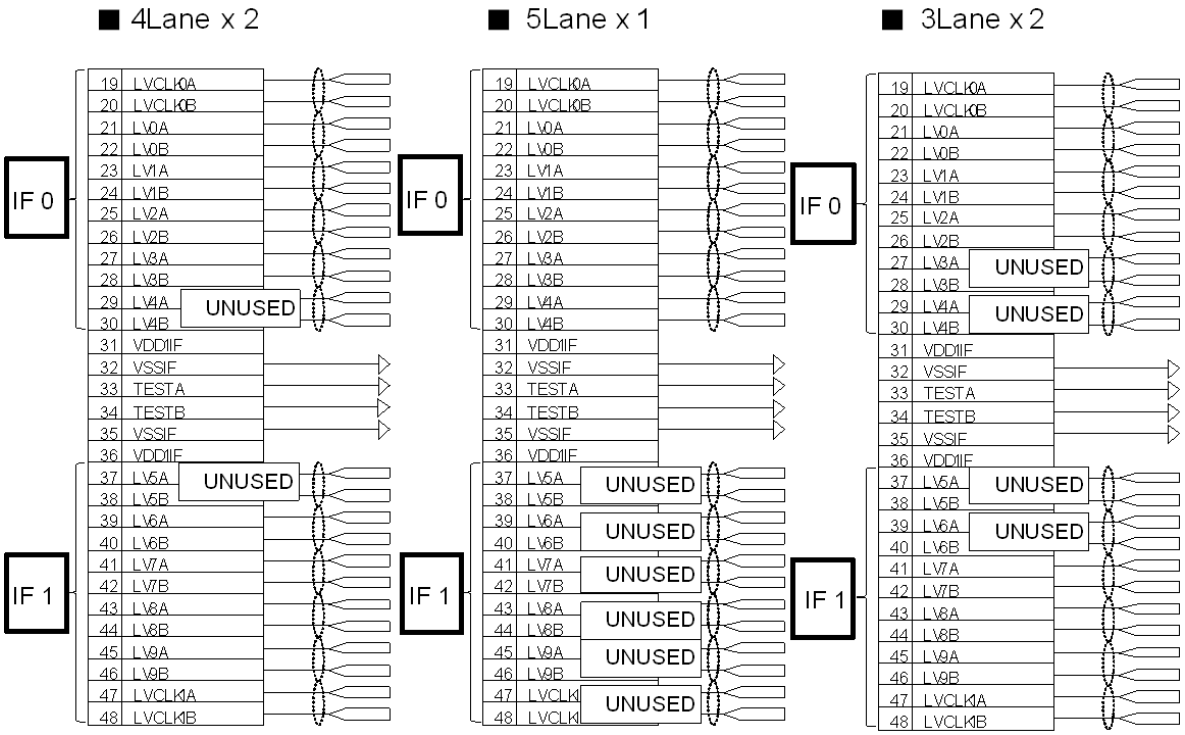


◆Register setting

Address	DATA	Register description	Function
0x04	[3]	PRTSWP	Selection of Input port order 0: Data input IF0 at first and then IF1 (※) 1: Data input IF1 at first and then IF0.
	[5:4]	PINSWP	Selection of Input lane order 00: IF0 Ascending order (LV0 to LV4) and IF1 Ascending order (LV5 to LV9) 01: IF0 Descending order (LV4 to LV0) and IF1 Ascending order (LV5 to LV9) 10: IF0 Ascending order (LV0 to LV4) and IF1 Descending order (LV9 to LV5) 11: IF0 Descending order (LV4 to LV0) and IF1 Descending order (LV9 to LV5)
	[7:6]	PN_POL	Selection of Input lane polarity 00: IF0 A=P B=N, IF1 A=P B=N 01: IF0 A=N B=P, IF1 A=P B=N 10: IF0 A=P B=N, IF1 A=N B=P 11: IF0 A=N B=P, IF1 A=N B=P

※ IF0: (LV0～LV4)、IF1: (LV5～LV9)

With this function usage, please pay attention about non-used PIN for each lane setting. And, please be noted that swapping function is invalid for un-used PIN, they are fixed.



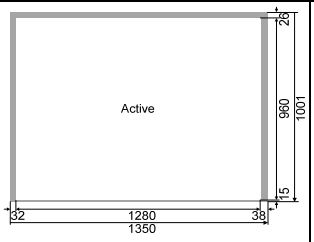
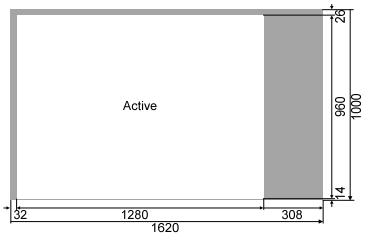
10.4. Input Signal Data Format

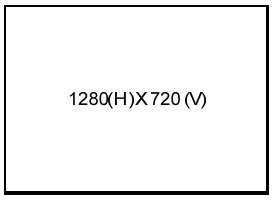
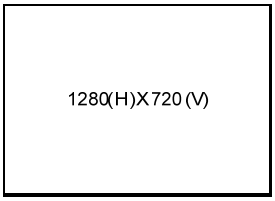
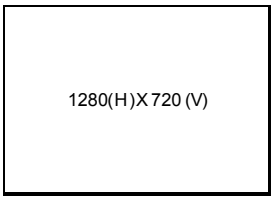
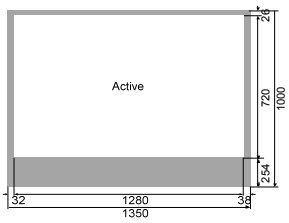
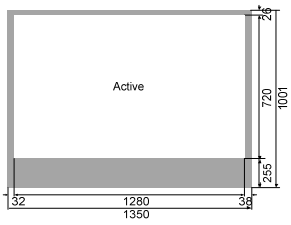
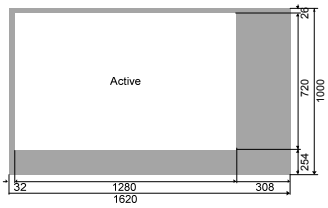
Set the panel timing registers appropriately for the input signal data format.

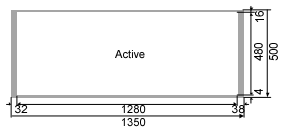
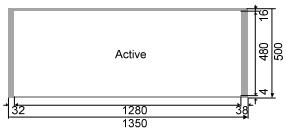
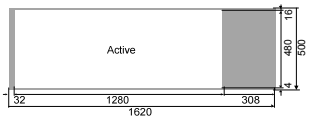
◆Register Settings

Address	DATA	Register description	Function
0x2A	[0]	FORMAT_SEL_H	Selection of Horizontal lines 0: 1280 1: Not Used
	[5:4]	FOEMAT_SEL_V	Selection of Vertical lines 00: 960 01: 720 10: Not Used 11: Not Used
0x34 | 0x62	-	H_ACT_D | SEL_W	For timing adjustment, according to each display format ①-⑨. Setting values should be submitted separately.

◆Panel Display Modes, and Input Formats

		①QVGA 60Hz Frame Rate	②QVGA 59.94Hz Frame Rate	③QVGA 50Hz Frame Rate
Panel Display Modes		1280(H) X 960(V)	1280(H) X 960(V)	1280(H) X 960(V)
Input Formats				
FORMAT_SEL_H		0		
FORMAT_SEL_V		00		
Active	H	1280		
	V	960		
Total	H	1350	1350	1620
	V	1000	1001	1000
FP	H	38	38	308
	V	14	15	14
SYNC	H	16	16	16
	V	6	6	6
BP	H	16	16	16
	V	20	20	20
BP+SYNC	H	32	32	32
	V	26	26	26
fv	Hz	60	59.94	50
Th	μs	16.667	16.667	20
Pixel Clock	MHz	81	80.999	81

		④720p 60Hz Frame Rate	⑤720p 59.94Hz Frame Rate	⑥720p 50Hz Frame Rate
Panel Display Modes				
Input Formats				
FORMAT_SEL_H		0		
FORMAT_SEL_V		01		
Active	H	1280		
	V	720		
Total	H	1350	1350	1620
	V	1000	1001	1000
FP	H	38	38	308
	V	254	255	254
SYNC	H	16	16	16
	V	6	6	6
BP	H	16	16	16
	V	20	20	20
BP+SYNC	H	32	32	32
	V	26	26	26
fv	Hz	60	59.94	50
Th	µs	16.667	16.667	20
Pixel Clock	MHz	81	80.9999	81

Panel Display Modes		⑦QVGA 120Hz Frame Rate 1280(H) X 480(V)	⑧QVGA 119.88Hz Frame Rate 1280(H) X 480(V)	⑨QVGA 100Hz Frame Rate 1280(H) X 480(V)
Input Formats				
Active	H	1280	1280	1280
	V	480x2	480x2	480x2
Total	H	1350	1350	1620
	V	500	500	500
FP	H	38	38	308
	V	8	8	8
SYNC	H	16	16	16
	V	6	6	6
BP	H	16	16	16
	V	6	6	6
BP+SYNC	H	32	32	32
	V	12	12	12
fv	Hz	120	119.88	100
Th	µs	16.667	16.683	20
Pixel Clock	MHz	81	80.919	81

※In case of 120Hz frame rate mode, pixel shifting area of orbit function is limited. Please refer “10.14.3. Pixel shifting area limitation in case of 120Hz frame rate” for more detailed.

10.5. 120Hz Mode

This product has 120Hz frame rate function which writes the same data in two vertical lines simultaneously.

Due to the same data writing in two vertical lines, V effective resolution becomes a half of its original input resolution. .

The 120 Hz mode consists of 2 modes, “Doubler” and “MALS (Motion-based Alternative Lighting Signal)”.

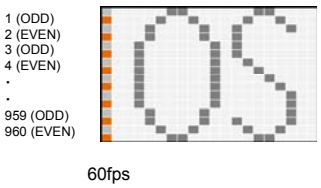
Doubler: Writing 2 vertical lines simultaneously and display “ODD” and “EVEN” field alternately..

MALS: Writing 2 vertical lines simultaneously and displaying “ODD” and “EVEN” field alternately. In MALS mode case, vertical data of “ODD” filed is 1 line shifted from that of EVEN field. This driving method improves sacrifice of effective resolution in case of Doubler mode.

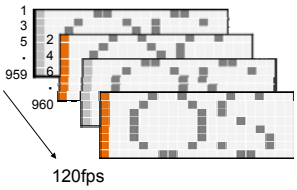
◆Register setting

Address	DATA	Register	Function
0x2A	[7]	VDR120MODE	Selection of 120Hz Mode or not 0: Invalid 1: Valid
0x2A	[6]	OESW	Selection of 120Hz Mode scan mode 0: Doubler 1: MALS

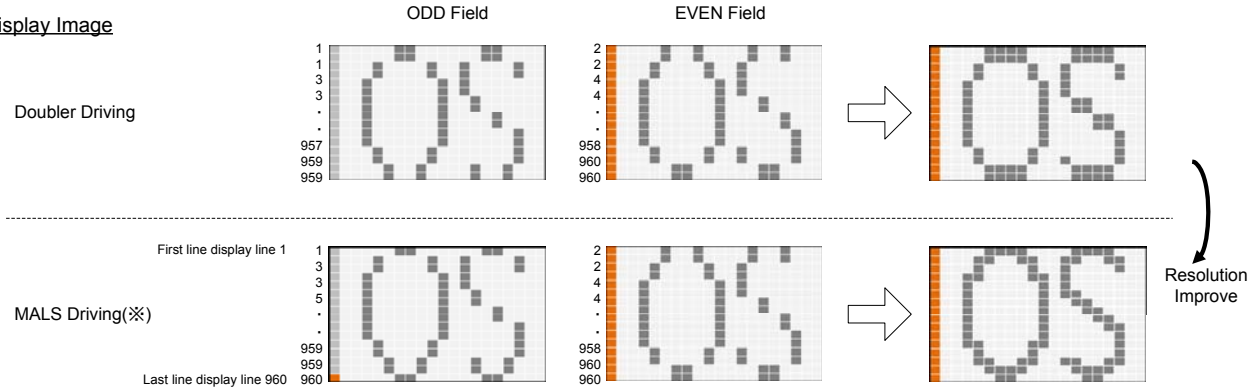
Original Video Image



Input Image （ODD／EVEN Divided）

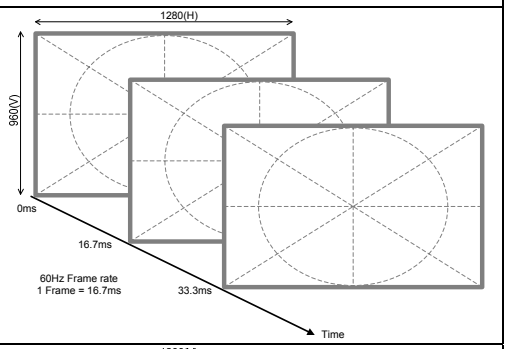
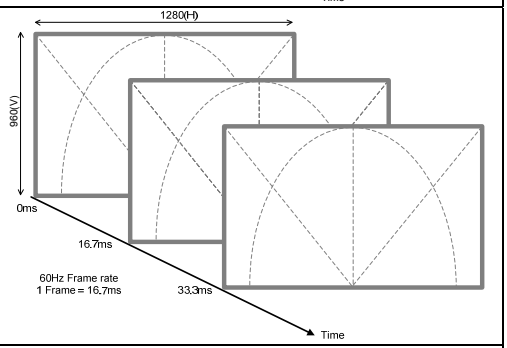
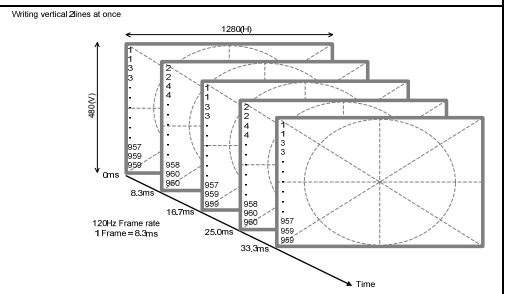
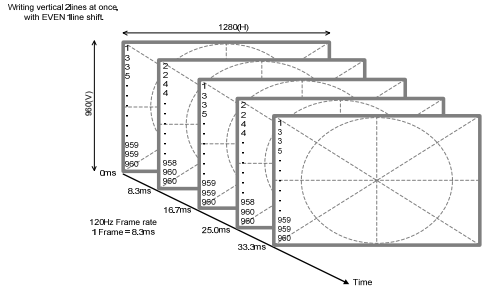


Display Image



※MALS: Motion-based Alternative Lighting Signal

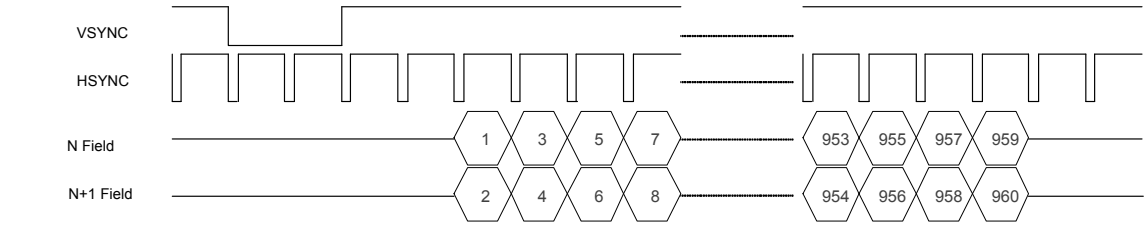
◆Input format and panel display image

Input format	VDR120MODE	OESW	Panel display image
①1280x960 60Hz ②1280x960 59.94Hz ③1280x960 50Hz 1280(H) X 960(V)	0:Invalid	Don't care	
	1 : Valid		
⑦1280x480 120Hz ⑧1280x480 119.88Hz ⑨1280x480 100Hz ODD 1280(H) X 480(V) EVEN 1280(H) X 480(V)	1 : Valid	0 : Doubler	
	1 : Valid	1 : MALS	

◆Input format

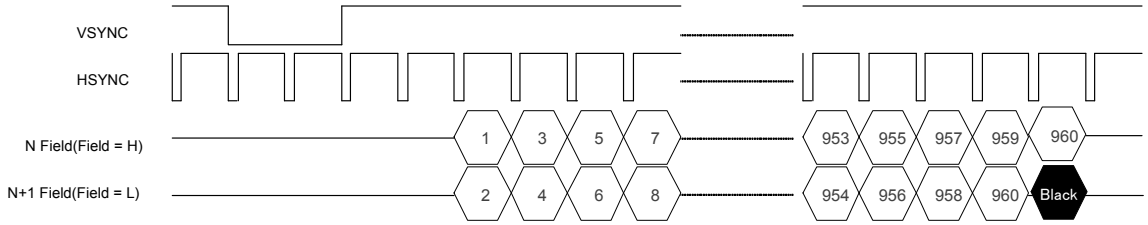
Doubler Driving

Writing 2Lines simultaneously



MALS Driving

Writing 2Lines simultaneously with 1line shift



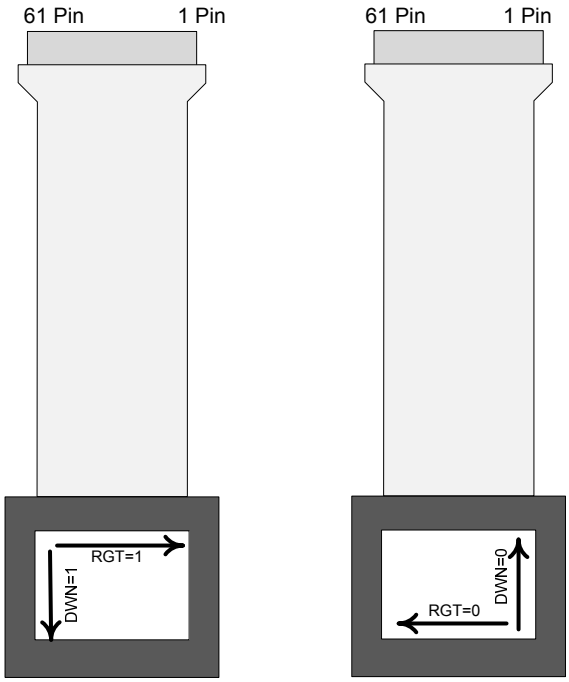
Please be noted that firstly ODD field is displayed after PS (Power Save) mode off.

10.6. Up/down and Right/left Inversion Function

Up/down and right/left inverse display of the panel are set by the registers RGT and DWN, respectively.

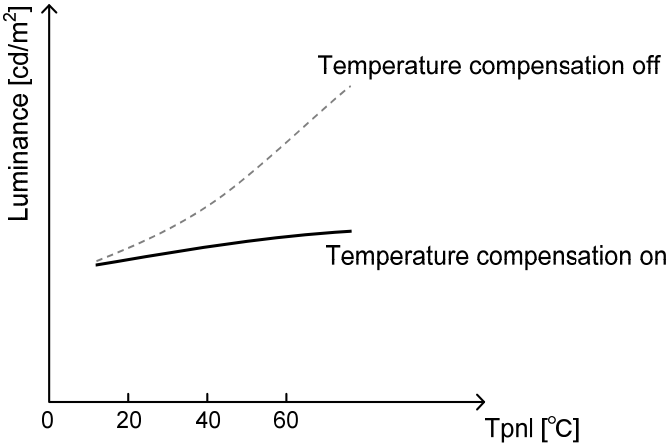
◆Register settings

Address	DATA	Register	Function
0x00	[2]	RGT	Selection of rightward / leftward scan 0: Leftward scan 1: Rightward scan (Default)
	[3]	DWN	Selection of upward / downward scan 0: Upward scan 1: Downward scan (Default)



10.7. Luminance Temperature Compensation Function

In general, luminance of OLED depends on display panel temperature as show in below. This module integrates luminance compensation function against panel temperature variation. This function allows to sustain relatively constant luminance even if panel temperature changing as shown in below.



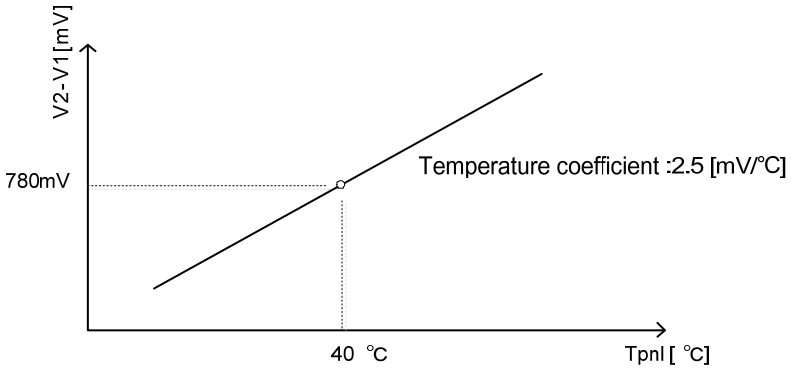
◆Register Settings

Address	DATA	Register	Function
0x01	[3:2]	CALSESL	VCAL(pin# 55) output selection 00: 0.1*VDD2 01: 0.25*VDD2 10: V1 output(*) 11: V2 output(*)
0x01	[6:5]	T_SLOPE	Temperature compensation gain selection 00: Mode A (Default) 01: Not used 10: Not used 11: Not used

◆ How to detect panel temperature

The temperature sensor voltage can be received from VCAL pin (#55).

Setting the register CALSEL as noted in above, and read the “V1” and “V2” outputs. Actual panel temperature can be calculated by subtracting V1 from V2, refer figure in below



10.8. Luminance direct setting function

In previous modules, luminance can be set by “CALDAC” register. Luminance is set with “CALDAC” value, not direct luminance value. Along with ECX337, luminance can be set with luminance value directly. It should be more simple process than previous modules. Still, “CALDAC” value control is available besides this approach.

◆Register Setting

Address	DATA	Register	Function
0x11	[0]	L_AT_CALEN	Luminance direct setting function 0:Invalid 1:Valid
	[2]	WB_CALEN	Auto adjustment of white balance in case this function is Valid. 0:Invalid 1:Valid
0x13	[6:0]	REQUEST_LV	Luminance setting register（Range ; 50cd/m^2～1000cd/m^2 , Step ; 10cd/m^2） 0000101: 50cd/m^2 | 0001111: 150cd/m^2 (Default) | 1100100: 1000cd/m^2

※Still CALDAC register is valid to control luminance.

10.9. Luminance changing speed

When luminance is changed by luminance direct setting command, dynamic changing speed (slope) is selectable, “slow” to “fast” with 7 slopes. Prompt luminance change can be noticeable. It is available to select adequate slope based on customer application and usage condition.

◆Register setting

Address	DATA	Register	Function
0x11	[1]	L_SEAMLESSEN	Luminance change speed function 0:Invalid 1:Valid
0x07	[2:0]	C_SLOPE	Luminance change speed synchronized with Vertical signal 000(0) : Prompt Transition (Default) 001(1) : Slow Speed | 111(7) : Fast Speed

10.10. Luminance control function

Available to control luminance based on “CALDAC” register writing. In order to valid this function, Set with “1” for “OTPCALDAC_REGEN” along with setting “0” for “L_AT_CALEN”

◆Register setting

Address	DATA	Register	Function
0x11	[0]	L_AT_CALEN	Luminance direct setting function 0:Invalid 1:Valid
0x06	[2]	OTPCALDAC_REGEN	Luminance control function 0: Invalid (Default) 1: Valid
0x43	[7:0]	CALDAC[8:1]	Luminance control value 000000000 (0):Lowest luminance | 100000000 (256): Default | 111111111 (511):Highest luminance
0x44	[0]	CALDAC[0]	

10.11. White Balance Adjustment Function

10.11.1. Contrast / Sub Contrast

White balance can be adjusted by two ways. One is to independently define of Red, Green, Blue luminance. Another is to simultaneously define them at once. Available to execute both ways at once, please refer example 2 in below. This function can be valid when “OTPDG_REGEN”=1.

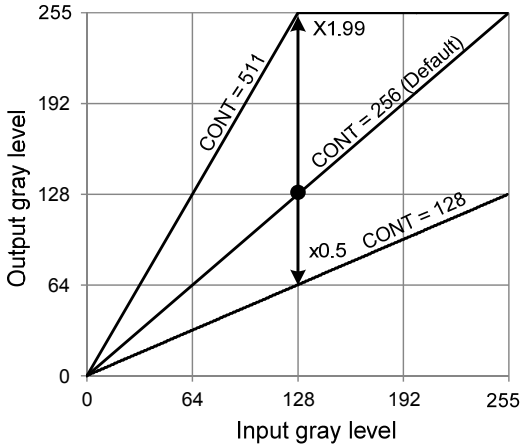
◆ Register Settings

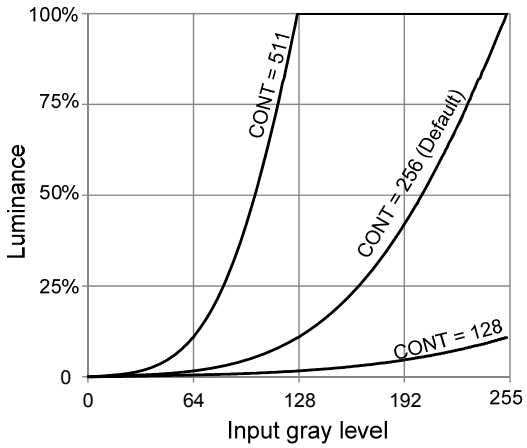
Address	DATA	Register	Function
0x06	[0]	OTPDG_REGEN	White chromaticity adjustment 0: Preset mode valid 1: Preset mode invalid (CONT/BRT adjustment)
0x2B	[0]	CONT[8]	Contrast (gain) setting to RGB input signal 000000000 (0): x0 | 100000000 (256): x1 | 111111111 (511): x2
0x2C	[7:0]	CONT[7:0]	
0x2D	[7:0]	RCONT	R sub-contrast setting relative to CONT 00000000 (0): x0.5 | 10000000 (128): x1 | 11111111 (255): x1.5
0x2E	[7:0]	GCONT	G sub-contrast setting relative to CONT 00000000 (0): x0.5 | 10000000 (128): x1 | 11111111 (255): x1.5
0x2E	[7:0]	BCONT	B sub-contrast setting relative to CONT 00000000 (0): x0.5 | 10000000 (128): x1 | 11111111 (255): x1.5

◆Contrast Adjustment (RGB Simultaneous Adjustment)

R, G and B output signal are adjusted simultaneously corresponding to the input signal using the register “CONT”. Setting value is 0 to 511 (decimal notation). Output gray level can be adjusted based on table in below.

CONT setting value	0	…	128	…	256 (Default)	…	384	…	511
Output gray level (to input)	× 0	…	× 0.5	…	× 1	…	× 1.5	…	× 1.99



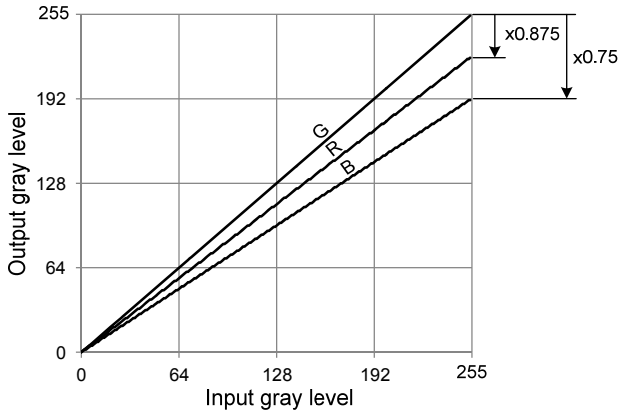


◆Sub Contrast Adjustment (RGB independent adjustment)

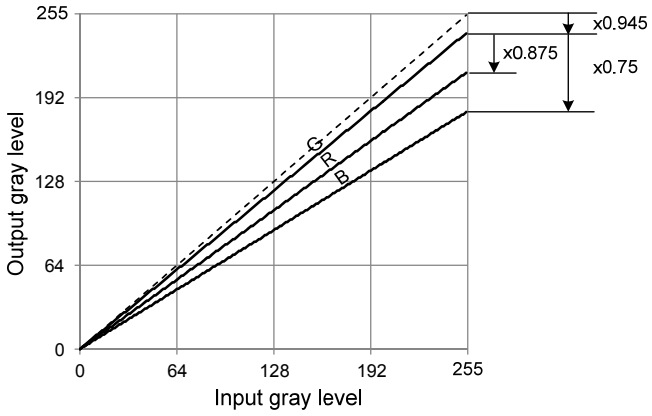
R, G and B output signal are adjusted separately using RCONT, GCONT and BCONT registers respectively, besides the register “CONT” The R, G and B output signal depends on both “RCONT, GCONT, BCONT” and “CONT”, as shown in examples in below. Gain for output and input is determined with multiple of “RCONT or GCONT or BCONT” and “CONT”. The “RCONT, GCONT, BCONT” setting range is 0 to 255 (decimal notation).

R/G/BCONT setting value	0	…	64	…	128 (Default)	…	192	…	255
Output gray level (to CONT)	× 0.5	…	× 0.75	…	× 1	…	× 1.25	…	× 1.49

Ex. 1
CONT = 256 (x1)
RCONT = 96 (x0.875)
GCONT = 128 (x1)
BCONT = 64 (x0.75)



Ex. 2
CONT = 242 (x0.945)
RCONT = 96 (x0.875)
GCONT = 128 (x1)
BCONT = 64 (x0.75)



10.11.2. Brightness Adjustment

There are two ways to adjust brightness. One is RGB simultaneous adjustment. Another is R, G and B independent brightness adjustment. Both ways can be applicable at once.
This function is valid when “OTPDG_REGEN”=1.

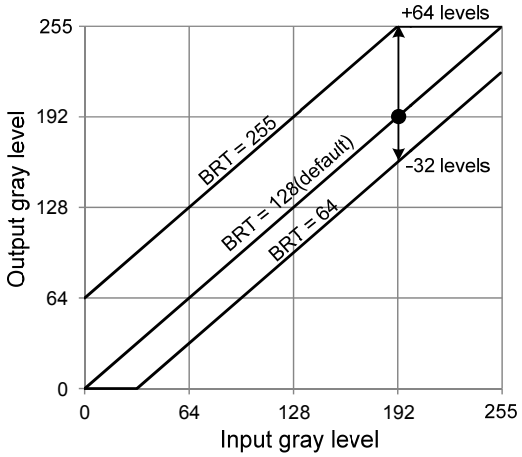
◆Register Settings

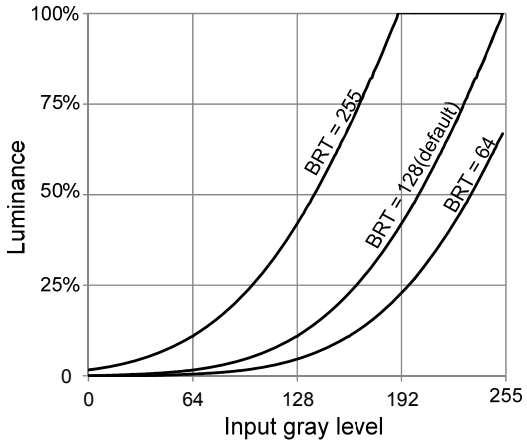
Address	DATA	Register	Function
0x06	[0]	OTPDG_REGEN	White chromaticity adjustment 0: Preset mode valid 1: Preset mode invalid (CONT/BRT adjustment)
0x30	[7:0]	BRT	Brightness (bias) setting to RGB input signal 00000000 (0): -64 gray level | 10000000 (128): 0 | 11111111 (255): +64 gray level
0x31	[7:0]	RBRT	R sub-brightness setting relative to BRT 00000000 (0): -64 gray level | 10000000 (128): 0 | 11111111 (255): +64 gray level
0x32	[7:0]	GBRT	G sub-brightness setting relative to BRT 00000000 (0): -64 gray level | 10000000 (128): 0 | 11111111 (255): +64 gray level
0x33	[7:0]	BBRT	B sub-brightness setting relative to BRT 00000000 (0): -64 gray level | 10000000 (128): 0 | 11111111 (255): +64 gray level

◆Brightness Adjustment (RGB simultaneous Adjustment)

R, G and B of input signal can be adjusted simultaneously using register BRT. The setting value is 0 to 255 (decimal notation).

BRT setting value	0	…	64	…	128(Default)	…	192	…	255
Output gray level(to input)	-64	…	-32	…	0	…	+32	…	+63





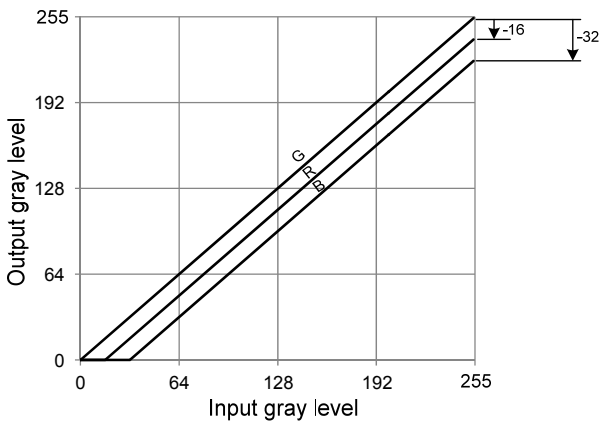
◆Sub Brightness Adjustment (RGB independent adjustment)

R, G and B output signal are adjusted separately using registers “RBRT, GBRT and BBRT” respectively, besides the register “BRT”

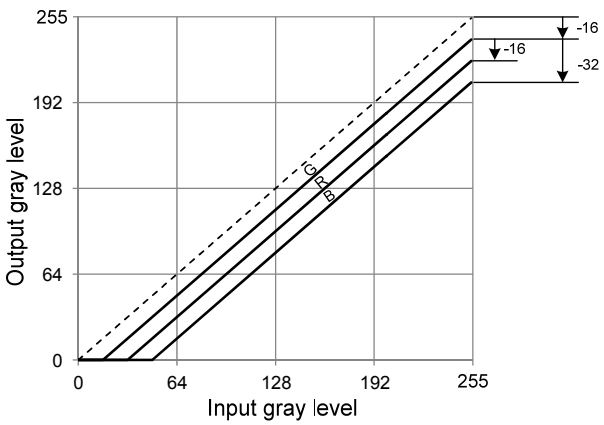
The R, G and B output signal depends on both “RBRT, GBRT, BBRT” and “BRT”, as shown in example in below. Offset between output and input is determined with sum of “RBRT or GBRT or BBRT” and “BRT”. The “RBRT, GBRT, BBRT” setting range is 0 to 255 (decimal notation).

R/G/BBRT setting value	0	…	64	…	128 (Default)	…	192	…	255
Output gray level (to BRT)	-64	…	-32	…	0	…	+32	…	+63

Ex. 1
BRT = 128 (0)
RBRT = 96 (-16 gray level)
GBRT = 128 (0)
BBRT = 64 (-32 gray level)



Ex. 2
BRT = 96 (-16 gray level)
RBRT = 96 (-16 gray level)
GBRT = 128 (0)
BBRT = 64 (-32 gray level)



10.12. RGB gray level tuning function

It is availavle to adjust 8, 16, 32, 64, 96, 128 and 192 gray level of input RGB signal.

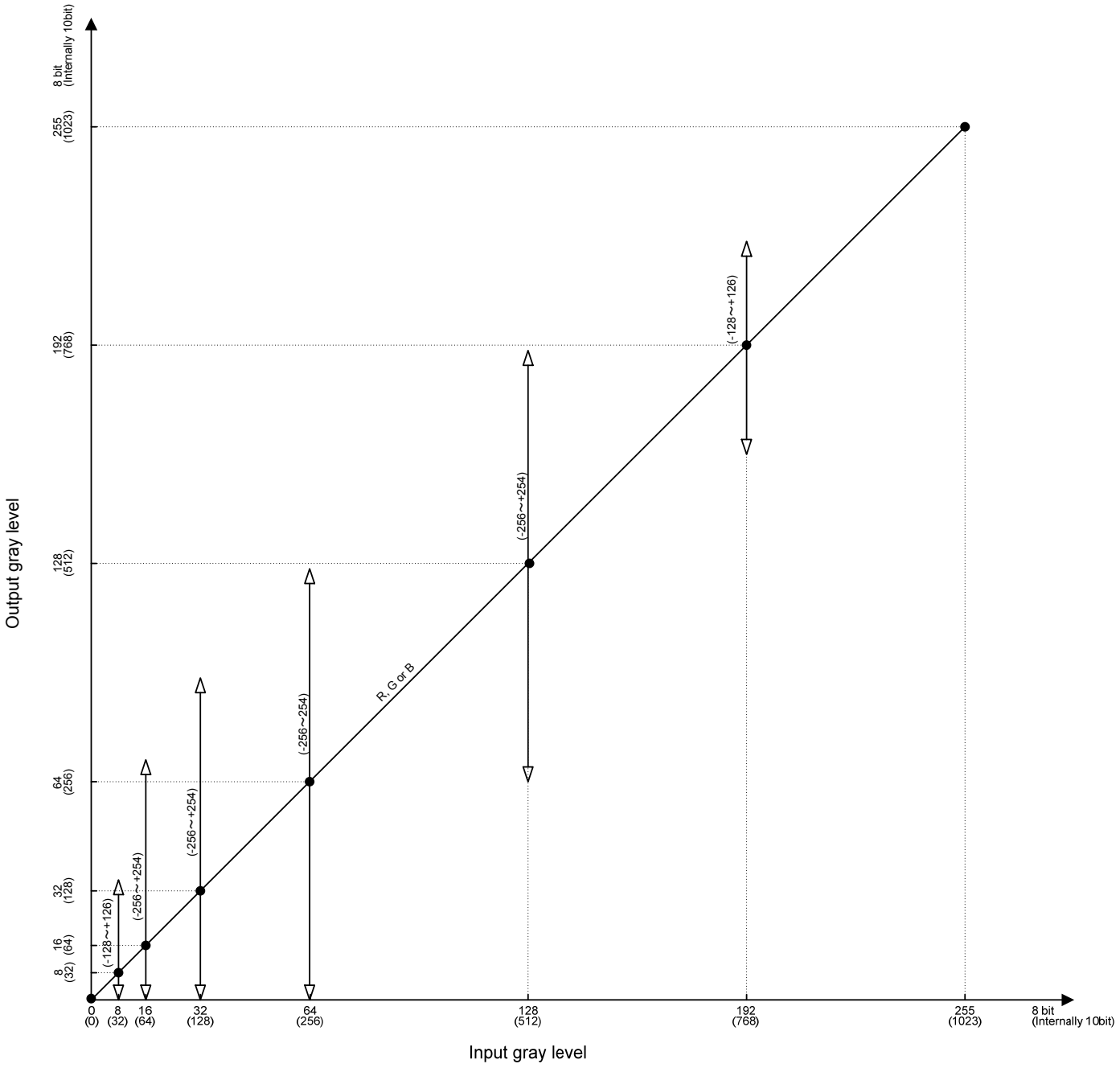
This function enables fine tuning of white balance at gray level..

Each gray level between one and another (8 and 16 16 and 32, 32 and 64, 64 and 96, 96 and 128, 128 and 192) are interpolated automatically.

In this module, the function is operated based on 10 bit calculation. That's reason why output gray level described based on 10bit base.

◆Register settings

Address	DATA	Register	Function
0x15 0x1C 0x23	[6:0] [6:0] [6:0]	DRGAMMA1 DGGAMMA1 DBGAMMA1	Digital gamma R/G/B 8 gray level adjustment 1000000 (-64): -128 gray level : 0000000 (0): 0 : 0111111 (+63): +126 gray level
0x16 0x1D 0x24	[7:0] [7:0] [7:0]	DRGAMMA2 DGGAMMA2 DBGAMMA2	Digital gamma R/G/B 16 gray level adjustment 10000000 (-128): -256 gray level : 00000000 (0): 0 : 01111111 (+127): +254 gray level
0x17 0x1E 0x25	[7:0] [7:0] [7:0]	DRGAMMA3 DGGAMMA3 DBGAMMA3	Digital gamma R/G/B 32 gray level adjustment 10000000 (-128): -256 gray level : 00000000 (0): 0 : 01111111 (+127): +254 gray level
0x18 0x1F 0x26	[7:0] [7:0] [7:0]	DRGAMMA4 DGGAMMA4 DBGAMMA4	Digital gamma R/G/B 64 gray level adjustment 10000000 (-128): -256 gray level : 00000000 (0): 0 : 01111111 (+127): +254 gray level
0x19 0x20 0x27	[7:0] [7:0] [7:0]	DRGAMMA5 DGGAMMA5 DBGAMMA5	Digital gamma R/G/B 96 gray level adjustment 10000000 (-128): -256 gray level : 00000000 (0): 0 : 01111111 (+127): +254 gray level
0x1A 0x21 0x28	[7:0] [7:0] [7:0]	DRGAMMA6 DGGAMMA6 DBGAMMA6	Digital gamma R/G/B 128 gray level adjustment 10000000 (-128): -256 gray level : 00000000 (0): 0 : 01111111 (+127): +254 gray level
0x1B 0x22 0x29	[6:0] [6:0] [6:0]	DRGAMMA7 DGGAMMA7 DBGAMMA7	Digital gamma R/G/B 192 gray level adjustment 1000000 (-64): -128 gray level : 0000000 (0): 0 : 0111111 (+63): +126 gray level



10.13. Dithering Function

This function expresses quasi-gradations between original gradations based on FRC (Frame Rate Control) technology This function can compensate the loss of the number of gray level due to gray level sacrifice for contrast and brightness adjustment. In terms of the gray level sacrifice, please refer “10.8 Luminance adjustment function” and “10.9 White balance adjustment function”.

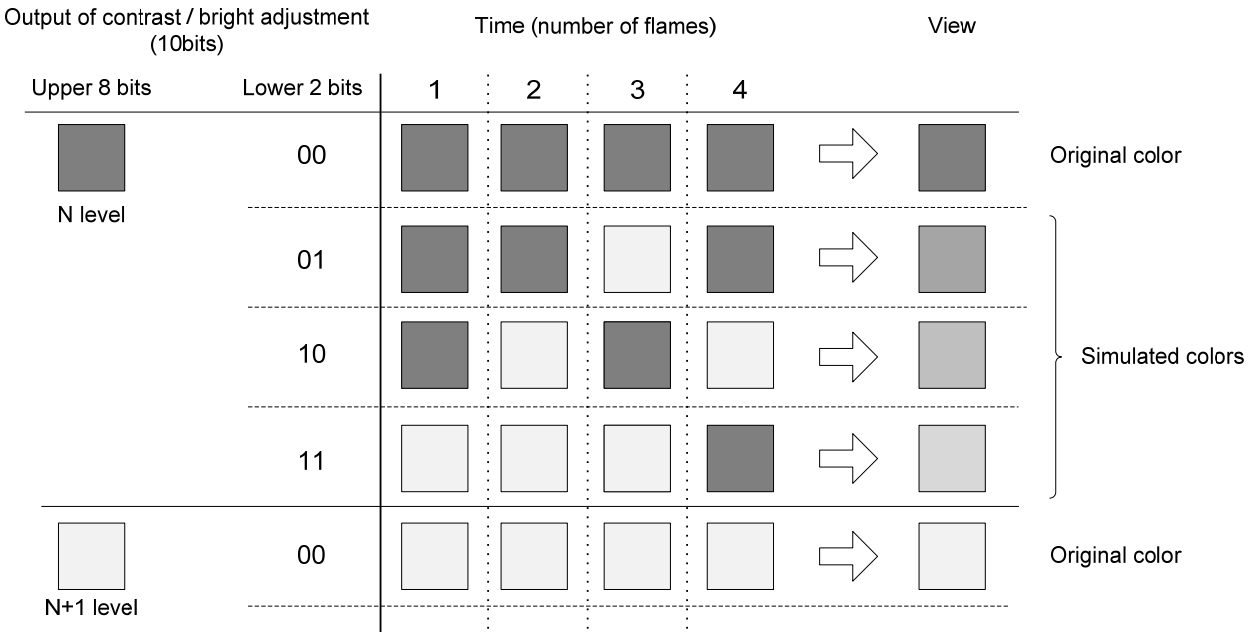
◆Register Settings

Address	DATA	Register	Function
0x05	[3]	DITHEREN	Dithering processing 0: Off 1: On

10.13.1. FRC (Frame Rate Control)

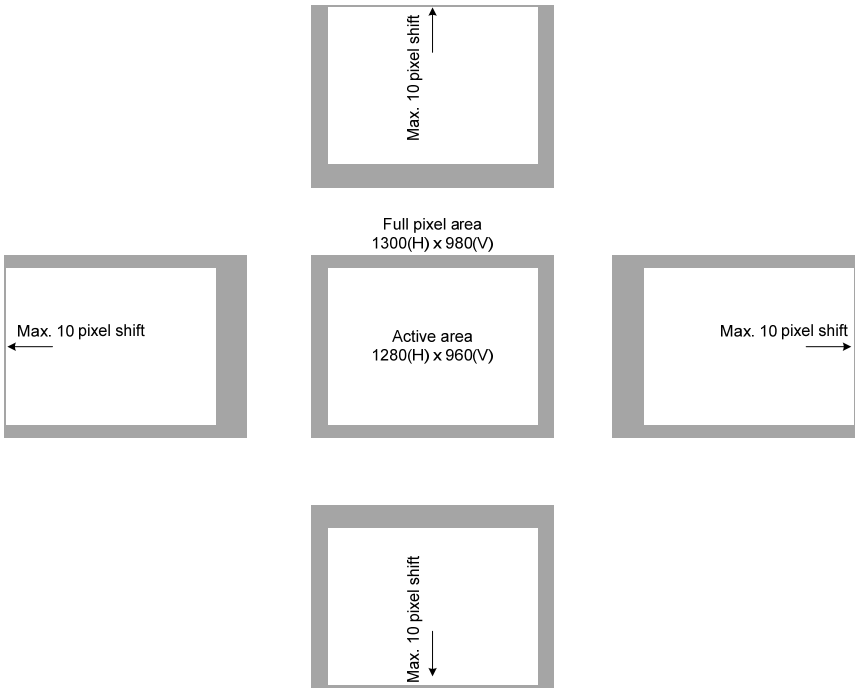
This function based on FRC technology. FRC can create quasi-gray levels between tangible gray levels based on time-resolution operation. Human eyes can percept brightness as average of time-wise in case displaying different brightness image under enough fast frame rate, as shown in below figure. The figure in below is case of 2bit FRC. When two gray levels are switching alternately in high-speed, human eyes can effectively percept average brightness of those two brightness levels as quasi-gray level. The quasi-gray level can be added besides original colors by changing data in 4-frame cycle making use of this property (2 bit FRC).

Quasi-gray level creation of 2bit FRC is shown in below, with assumption of one pixel.



10.14. Orbit Function

Scanning start position of data image can be changed. This enables reducing of unwanted noticeability of local luminance drop, so called bun-in. As other wording, this function is called “Pixel Shifting” or “Pixel Orbit”. This approach is common technic to alleviate burn-in for self-emitting display.



◆Register Settings

Address	DATA	Register	Function
0x02	[5:0]	ORBIT_H	Horizontal orbit adjustment 110110: -10 pixels | 000000: center(Default) | 001010: +10 pixels
0x03	[5:0]	ORBIT_V	Vertical orbit adjustment 110110: -10 pixels | 000000: center(Default) | 001010: +10 pixels

10.14.1. Horizontal Display Position Shift

The horizontal display start positon can be changed by the register ORBIT_H. The variable range is ± 10 pixels.

ORBIT_H setting value	-10	…	-1	0 (Default)	1	…	10
Register input value (Two’s compllement)	110110		111111	000000	000001		001010
Number of pixels shifted	Leftward 10-pixel	…	Leftward 1-pixel	Center	Rightward 1-pixel	…	Rightward 10-pixel

10.14.2. Vertical Display Position Shift

The vertical display start position can be changed by the register ORBIT_V. The variable range is ± 10 pixels.

ORBIT_V setting value	-10	…	-1	0 (Default)	1	…	10
Register input value (Two's compllement)	110110		111111	000000	000001		001010
Number of pixels shifted	Upward 10-pixels	…	Upward 1-pixel	Center	Downward 1-pixel	…	Downward 10-pixel

10.14.3. Pixel shifting area limitation in case of 120Hz frame rate

In case of 120Hz mode, pixel shifting range is limited. It is available from "-2" to "3" as V direction shifting range.

ORBIT_V Registor	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10
50, 60Hz Pixel shift	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10
120Hz mode Pixel shift	Invalid						-2		-1		0		1		2		3		Invalid		

11. Optical Characteristics

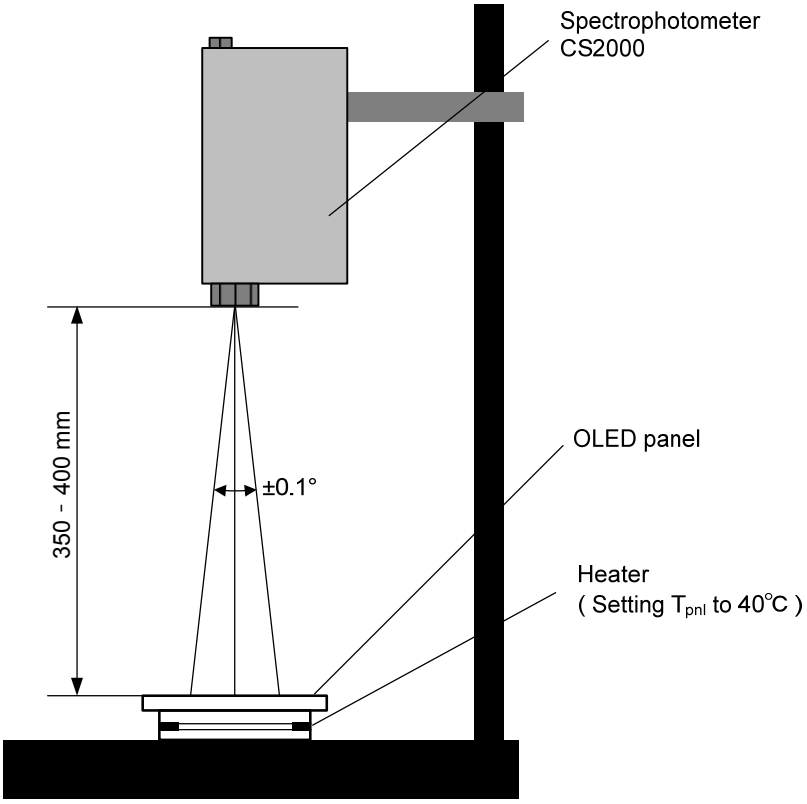
11.1. Optical Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
Luminance tolerance (255Level)	120～200 cd/m^2	LL	-20		+20	%
	200～600 cd/m^2	LM	-15		+15	%
	600～1,000 cd/m^2	LH	-20		+20	%
White Chromaticity tolerance (255 level)	120～200 cd/m^2	WLx	0.295	0.310	0.325	CIE
		WLy	0.305	0.320	0.335	CIE
	200～600 cd/m^2	WMx	0.298	0.310	0.322	CIE
		WMy	0.308	0.320	0.332	CIE
	600～1,000 cd/m^2	WHx	0.295	0.310	0.325	CIE
		WHy	0.305	0.320	0.335	CIE
White Chromaticity tolerance (192, 128 level)	300 cd/m^2	WGx	0.298	0.310	0.322	CIE
		WGy	0.308	0.320	0.332	CIE
Monochrome chromaticity	Red	Rx	0.620	0.640	0.660	CIE
		Ry	0.310	0.330	0.350	CIE
	Green	Gx	0.255	0.275	0.295	CIE
		Gy	0.625	0.645	0.665	CIE
	Blue	Bx	0.125	0.145	0.165	CIE
		By	0.040	0.060	0.080	CIE
Contrast Ratio		CR	10,000	—	—	

11.2. Measurement System and Measurement Condition

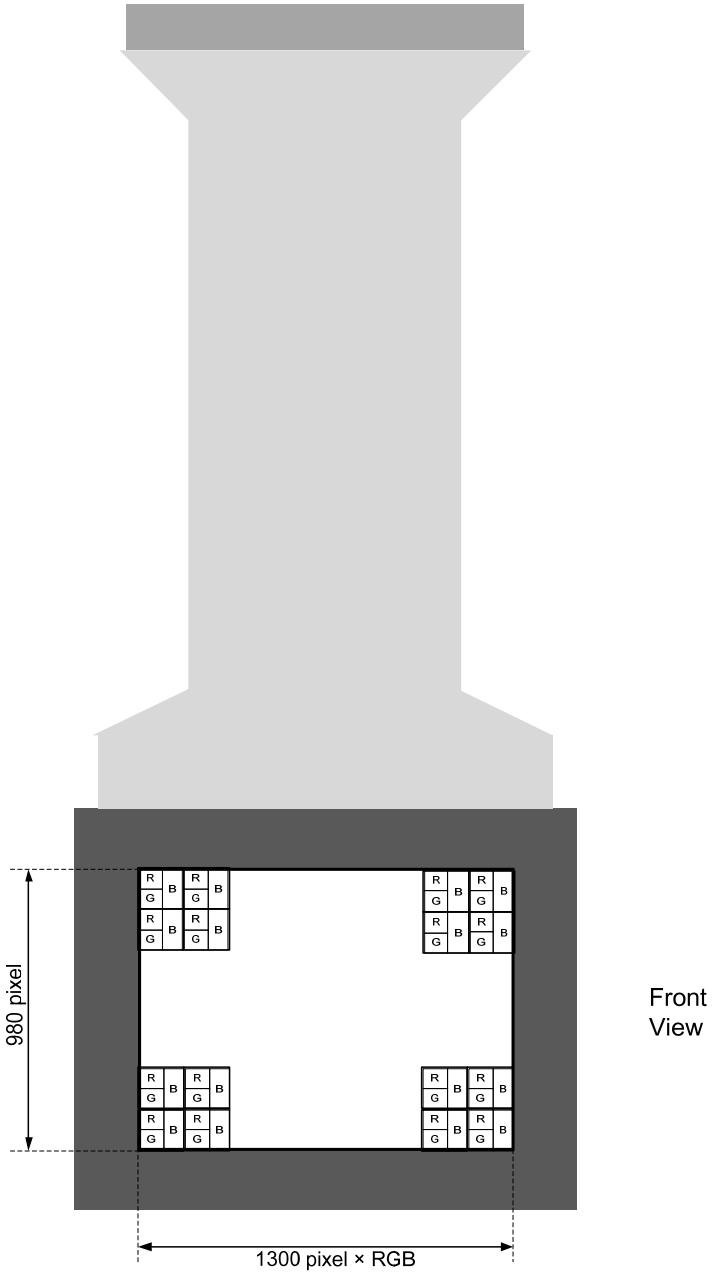
Measurement temperature: T_{pnl} = 40°C
Measurement point: One point on the screen center
Register setting: “OTPCALDAC_REGEN” = 0、”OTPDG_REGEN” = 0 (preset mode valid)

Item		Pattern	Luminance	Gray Level	Measurement Condition
Luminance / White chromaticity (255 level)	LL, WLx, WLy	Raster	120～200cd/m^2,	R=255 Level G=255 Level B=255 Level	Measured by system A
	LM, WMx, WMy		200～600cd/m^2,		
	LH, WHx, WHy		600～1000cd/m^2,		
White chromaticity (192 level)	WGx, WGy	Raster	300cd/m^2	R=192 Level G=192 Level B=192 Level	Measured by system A
White chromaticity (128 level)				R=128 Level G=128 Level B=128 Level	



Measurement system A

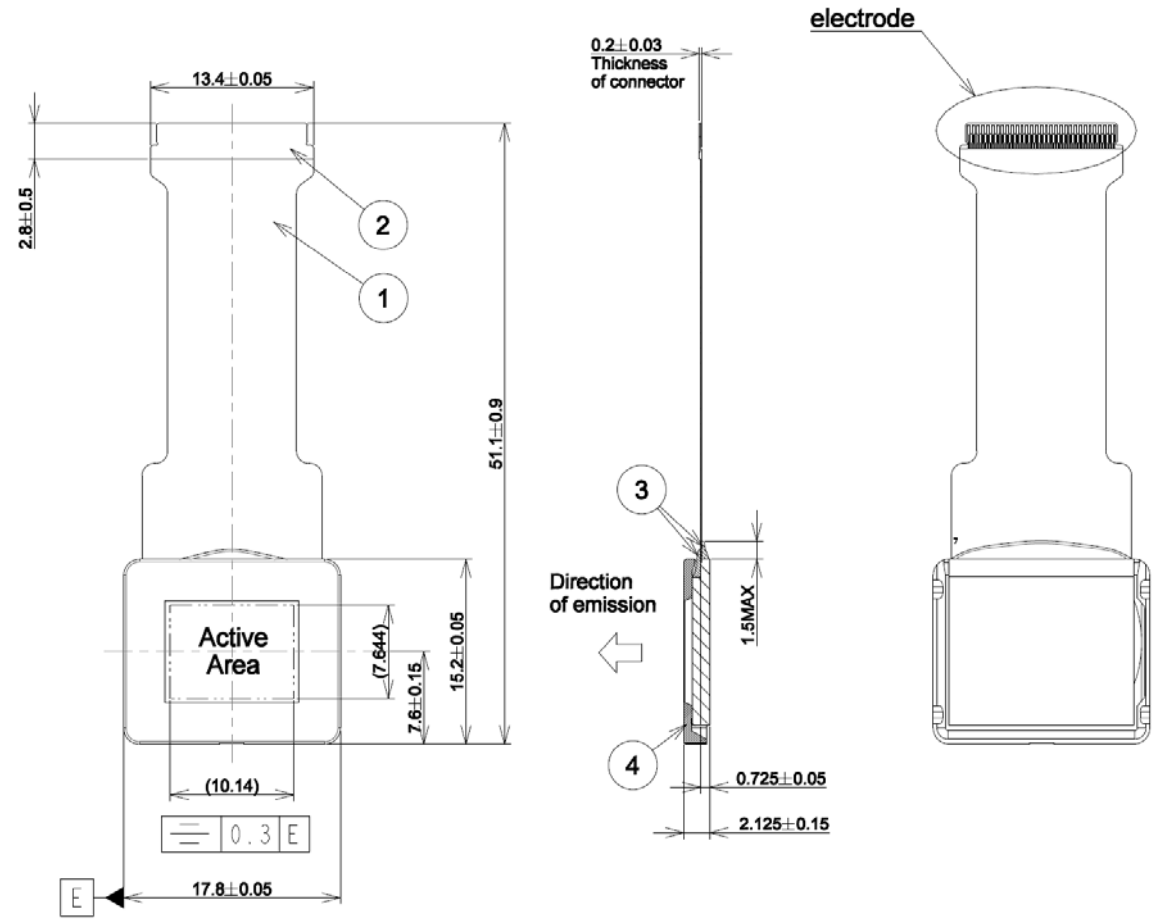
12. Pixel Alignment

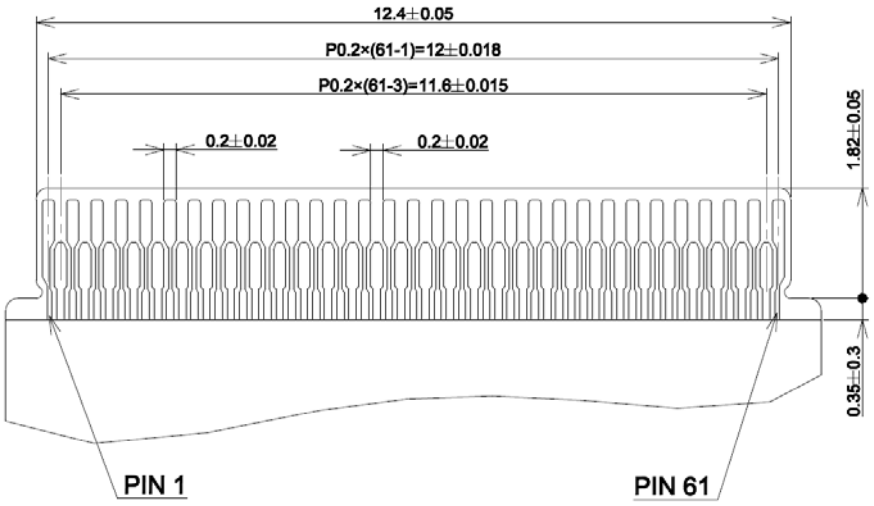


※Including Orbit pixels

13. Module Outline （Nagasaki 200mm wafer）

(Unit : mm)





No	Description
1	FPC
2	Stiffener
3	Reinforcing material
4	Outside frame

Mass 1.1g

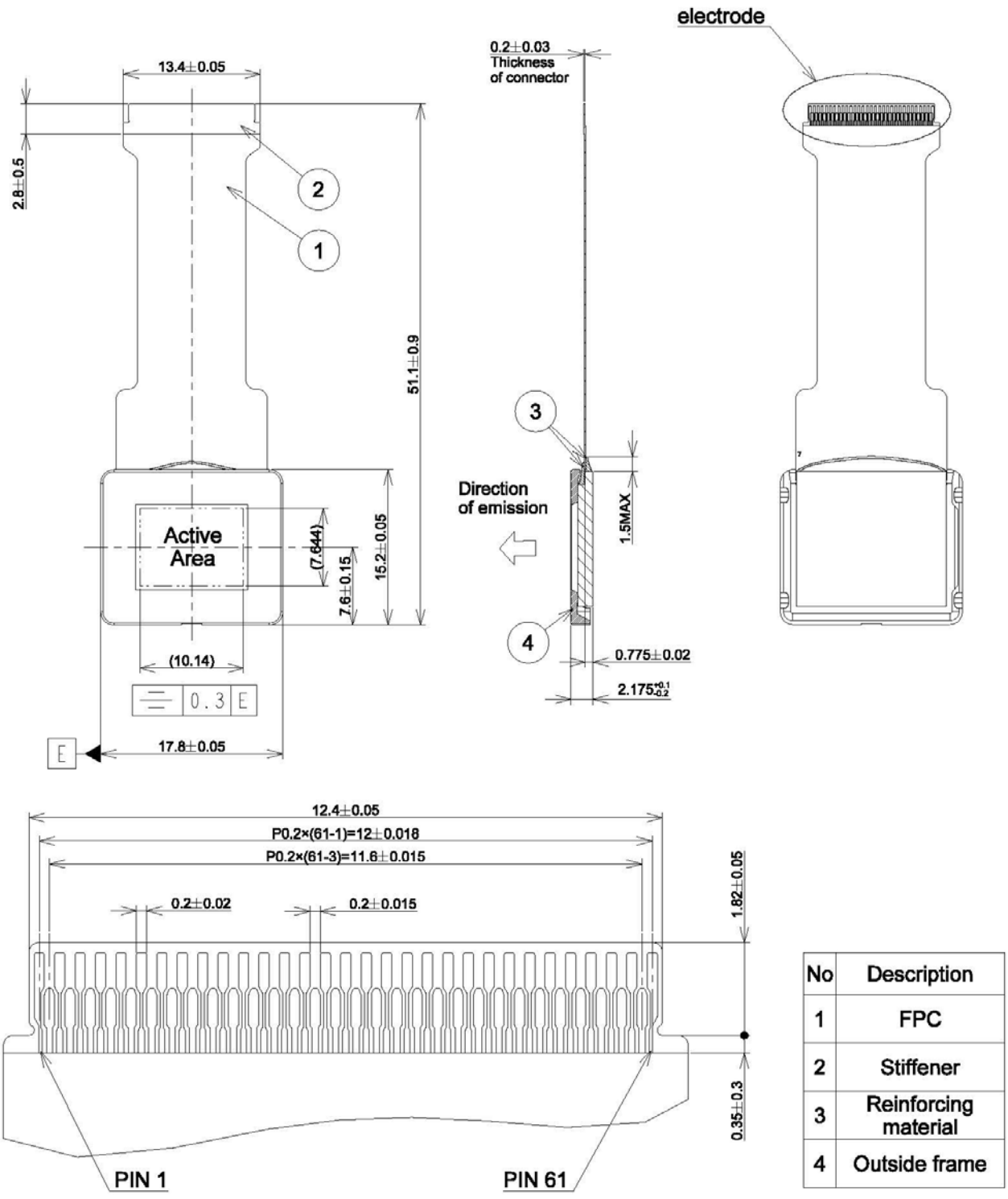
electrode(enlarged)

Recommended Connector

Manufacturer	JST Connector
Part Number	61FVXS-RSM1-GAN-TF

Module Outline （Kumamoto 300mm wafer） Tentative

(Unit : mm)



No	Description
1	FPC
2	Stiffener
3	Reinforcing material
4	Outside frame

Electrode(enlarged)

Mass 1.1g

Recommended Connector

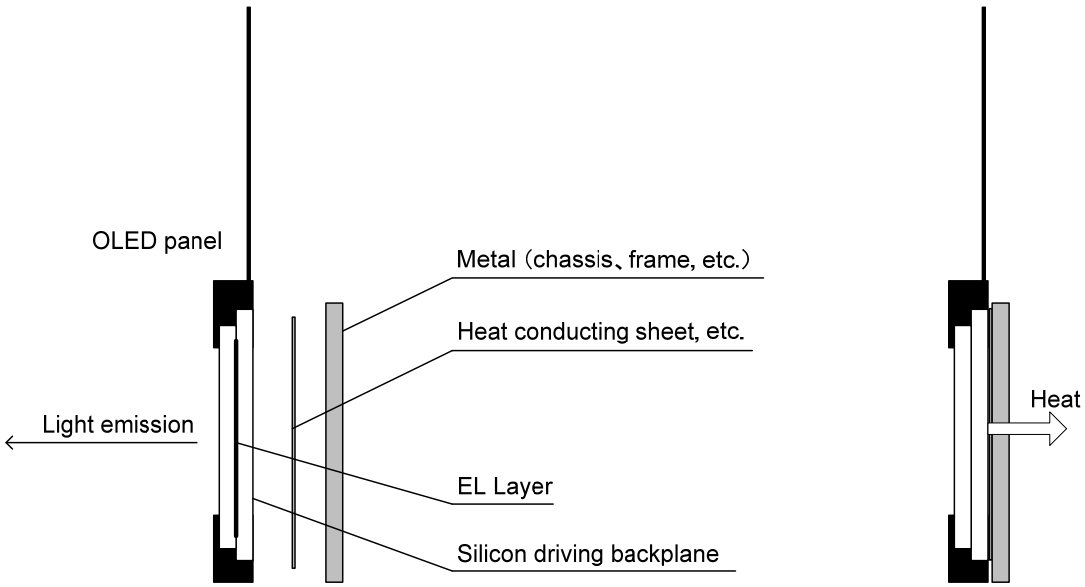
Manufacturer	JST Connector
Part Number	61 FVXS-RSM1-GAN-TF

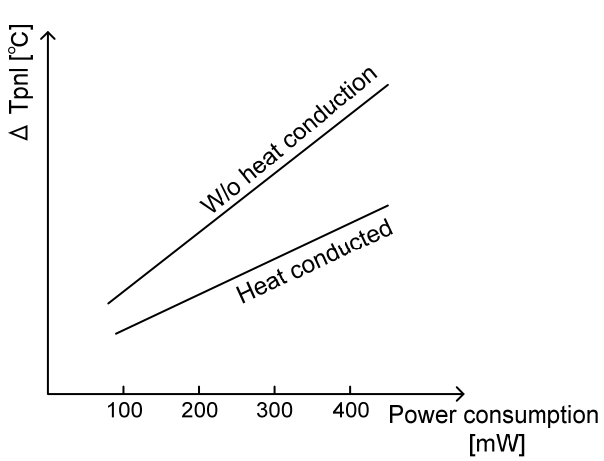
14. Recommended Items

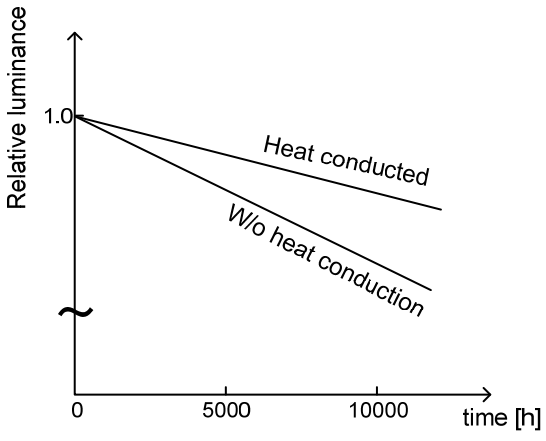
14.1. Suppression of the Panel Temperature

Temperature of organic EL panel tends to rise due to power consumption (heat generation) by the EL emissive layer and the integrated silicon drive circuits. The temperature rise may cause luminance drop over time.

The temperature rise in panel can be suppressed by establishing a thermal connection between panel rear surface (silicon substrate surface) and metal (chassis, frame, etc.) at panel mount area So, highly recommend the heat conductive sheet between them as show in below.







15. Notes on handling module

15.1. Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves or handle with bare hands.

(2) Use a wrist strap connecting ground when handling.

(3) Do not touch any electrodes on the panel.

(4) Wear non-chargeable clothes and conductive shoes.

(5) Install grounded conductive mats on the working floor and working table.

(6) Keep the panel away from any charged materials.

15.2. Protection from dust and dirt

(7) Operate in a clean environment.

(8) Do not touch the panel surface. The surface is easily scratched.
When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.

(9) Use ionized air to blow dust off the panel surface.

15.3. Others

(10) Not hold FPC (Flexible Printed Circuit) , not twist the FPC, not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.

(11) The minimum fold radius of the FPC is 1.0 mm, So, do not fold the FPC less than 1.0mm radius.

(12) Do not drop the module.

(13) Do not twist or bend the module .

(14) Keep the module away from heat sources.

(15) Not be close the module to water or other solvents.

(16) Do not store or use the module at high temperatures or high humidity circumstance, as the circumstance may affect module specifications. .

(17) When disposing of this, regard it as industrial waste and please comply with related regulations.

(18) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications. .

(19) This module is supposed to be delivered in a degassed aluminum laminated bag.
When storing this panel again after once unsealing the bag, please take following action. Put it into the aluminum laminated bag again.. Put in desiccant into the aluminum bag and the opening of the aluminum bag should be folded and seal the bag with tape. .