SONY

1.0 cm (Type 0.39) Active Matrix Color OLED Panel

# ECX334AF

## Description

The ECX334AF is a 1.0 cm (type 0.39) diagonal, 1024 (RGB) × 768 dots active matrix color OLED panel module using single-crystal silicon transistors. This panel incorporates panel driver and logic driver, and realizes small size, light weight and high definition.
(Applications: View finders, head mounted displays, very small monitors, etc.)

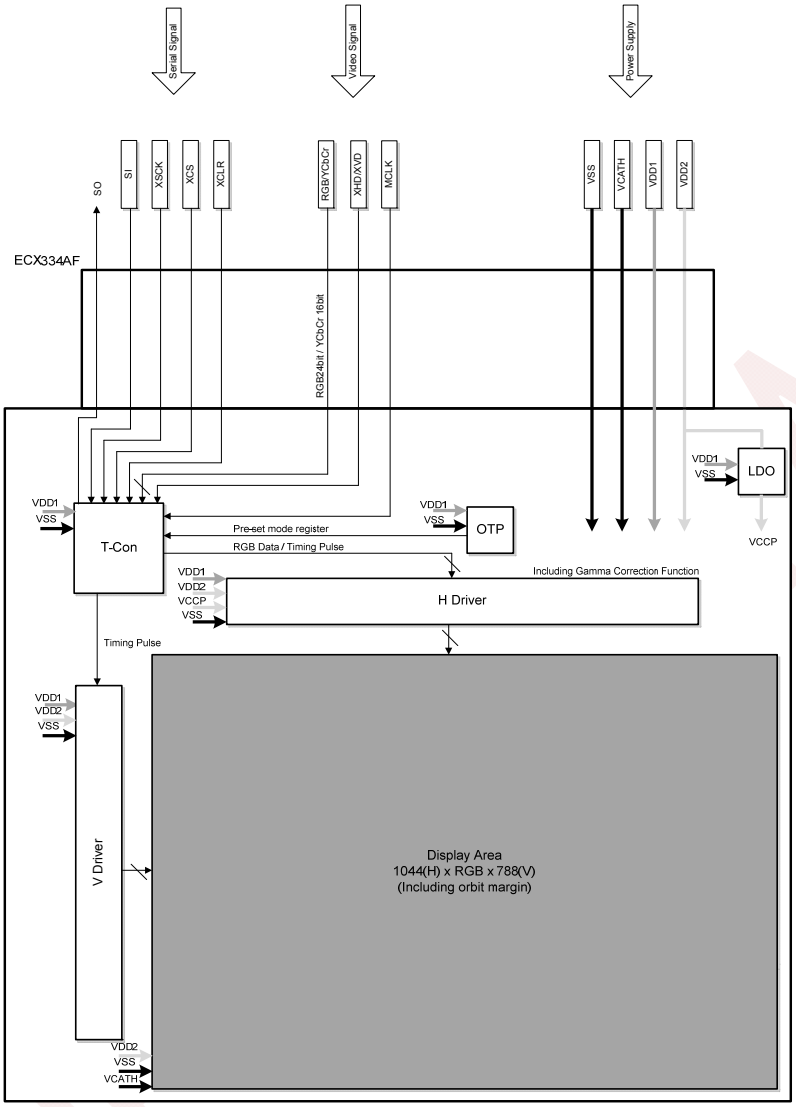
## Features

- Small-size, high-definition-type 0.39 XGA display dots 1024 (RGB) × 768 = 2.38M dots
- High contrast
- Wide color reproduction range
- High-speed response
- Thin type and light weight
- Power-saving function
- Up/down and/or right/left inverse display function
- Orbit supported
- Input interface that supports parallel RGB 24-bit and YCbCr 16-bit input

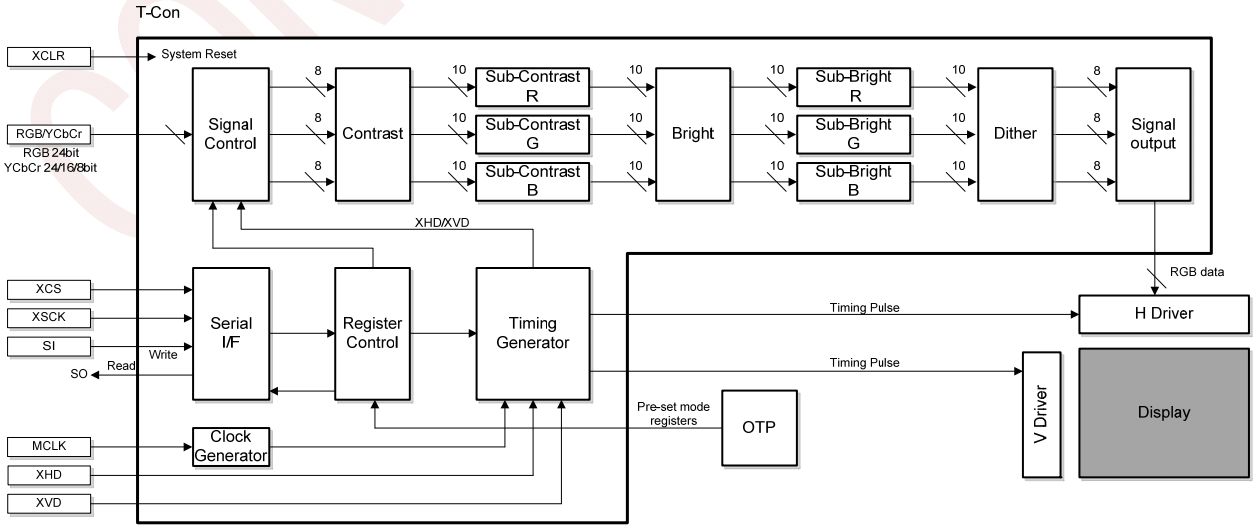
## Element Structure

Active matrix color OLED display element with on-chip driver using single-crystal silicon transistors

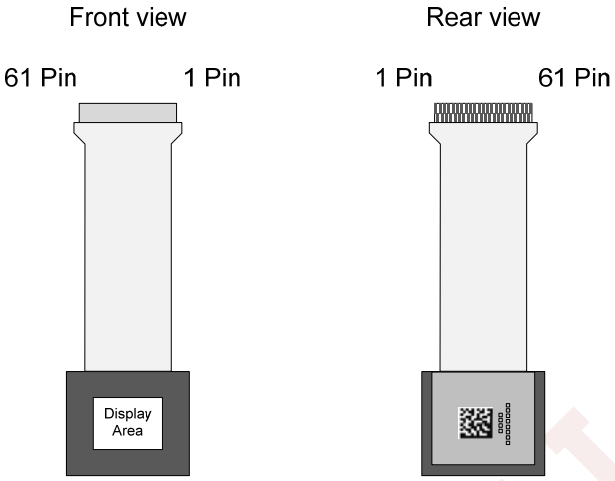
## Block Diagram




Details of T-Con



## Pin Assignment




## Pin Description

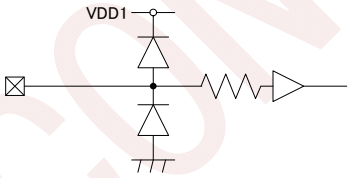
| Pin No. (connector side) | Symbol | Type | Pin Description | Equivalent circuit |
|---|---|---|---|---|
| 1 | TEST | Input | GND | |
| 2 | VCCP | Power supply | VCCP power supply | |
| 3 | VDD2 | Power supply | 10V power supply | |
| 4 | VSS | Power supply | GND | |
| 5 | VSS | Power supply | GND | |
| 6 | Vcath | Power supply | EL cathode power supply | |
| 7 | VSS | Power supply | GND | |
| 8 | VDD1 | Power supply | 1.8V power supply | |
| 9 | MCLK | Input | Clock | *1 |
| 10 | XHD | Input | Horizontal sync signal (negative polarity) | *1 |
| 11 | XVD | Input | Vertical sync signal (negative polarity) | *1 |
| 12 | XCLR | Input | System reset | *2 |
| 13 | Rin7/ GND | Input | (RGB input mode) Digital R signal/ (YCbCr input mode) GND | *1 |
| 14 | Rin6/ GND | Input | (RGB input mode) Digital R signal/ (YCbCr input mode) GND | *1 |
| 15 | Rin5/ GND | Input | (RGB input mode) Digital R signal/ (YCbCr input mode) GND | *1 |
| 16 | Rin4/ GND | Input | (RGB input mode) Digital R signal/ (YCbCr input mode) GND | *1 |
| 17 | Rin3/ GND | Input | (RGB input mode) Digital R signal/ (YCbCr input mode) GND | *1 |
| 18 | Rin2/ | Input | (RGB input mode) Digital R signal/ | *1 |

| Pin No. (connector side) | Symbol | Type | Pin Description | Equivalent circuit |
|---|---|---|---|---|
| | GND | | (YCbCr input mode) GND | |
| 19 | Rin1/ GND | Input | (RGB input mode) Digital R signal/ (YCbCr input mode) GND | *1 |
| 20 | Rin0/ GND | Input | (RGB input mode) Digital R signal/ (YCbCr input mode) GND | *1 |
| 21 | Gin7/ Yin7 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 22 | Gin6/ Yin6 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 23 | Gin5/ Yin5 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 24 | Gin4/ Yin4 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 25 | Gin3/ Yin3 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 26 | Gin2/ Yin2 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 27 | Gin1/ Yin1 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 28 | Gin0/ Yin0 | Input | (RGB input mode) Digital G signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 29 | VDD 1 | Power supply | 1.8V power supply | |
| 30 | VSS | Power supply | GND | |
| 31 | Bin7/ CbCrin7 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 32 | Bin6/ CbCrin6 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 33 | Bin5/ CbCrin5 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 34 | Bin4/ CbCrin4 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 35 | Bin3/ CbCrin3 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 36 | Bin2/ CbCrin2 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 37 | Bin1/ CbCrin1 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 38 | Bin0/ CbCrin0 | Input | (RGB input mode) Digital B signal/ (YCbCr input mode) Digital luminance signal | *1 |
| 39 | TEST (SCAN_MODE) | Input | Test pin (connect to GND) | *3 |
| 40 | TEST (TEN) | Input | Test pin (connect to VDD1) | *2 |
| 41 | TEST(PSCNT) | Input | Test pin (connect to GND) | *2 |
| 42 | XCS | Input | Serial communication Chip select | *2 |
| 43 | XSCK | Input | Serial communication Serial clock | *2 |
| 44 | SI | Input | Serial communication Data input | *2 |
| 45 | SO | Output | Serial communication Data output | *4 |
| 46 | TEST(DDEN) | Output | Test pin (DD converter enable) | *4 |

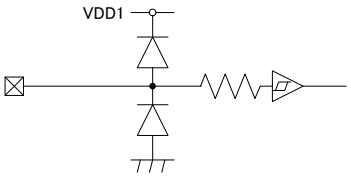
| Pin No. (connector side) | Symbol | Type | Pin Description | Equivalent circuit |
|---|---|---|---|---|
| 47 | TEST (VFUSE) | Power supply | Test pin (connect to GND) | *5 |
| 48 | VSS | Power supply | GND | |
| 49 | VDD1 | Power supply | 1.8V power supply | |
| 50 | VCAL | Output | Correction voltage output in temperature compensation circuit | *6 |
| 51 | TEST | Output | Test pin | *6 |
| 52 | TEST | Output | Test pin | *6 |
| 53 | VG255 | Output | Gamma top reference voltage (255 gray scale) | *6 |
| 54 | VG0 | Output | Gamma bottom reference voltage (0 gray scale) | *6 |
| 55 | VOFS | Power supply | Vofs voltage | *6 |
| 56 | Vcath | Power supply | EL cathode power supply | |
| 57 | VSS | Power supply | GND | |
| 58 | VSS | Power supply | GND | |
| 59 | VDD2 | Power supply | 10V power supply | |
| 60 | VCCP | Power supply | VCCP power supply | |
| 61 | VSS | Power supply | GND | |

## Equivalent Circuit

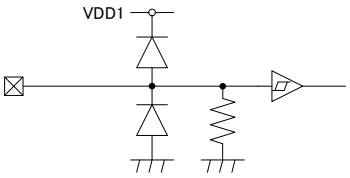
*1
Pin No. 9,10,11 & RGB Data



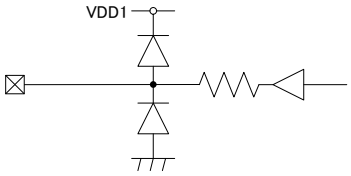

*2(Schmitt)
Pin No. 12,40,41,42,43 & 44



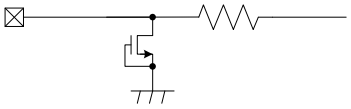

*3(Schmitt)
Pin No. 39



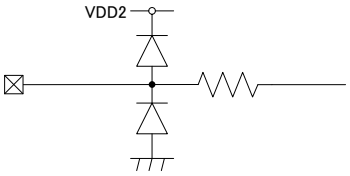

*4
Pin No. 45 & 46




*5
Pin No. 47



*6
Pin No. 50,51,52,53,54 & 55



## Absolute Maximum Ratings

| Item | Symbol | Min. | Maximum Ratings | Unit |
|---|---|---|---|---|
| 1.8V power supply | VDD1 | -0.3 | 2.0 | V |
| 10V power supply | VDD2 | -0.3 | 12.0 | V |
| EL cathode voltage | Vcath | -0.3 | 0.3 | V |
| Logic input voltage | Vi | -0.3 | VDD1+ 0.3 | V |
| Storage temperature | Tpnl | -30 | +80 | °C |

## Recommended Operating Conditions

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| 1.8V power supply | VDD1 | 1.62 | 1.8 | 1.98 | V |
| 10V power supply | VDD2 | 9,7 | 10.0 | 10.3 | V |
| EL cathode voltage | Vcath | -0.3 | 0 | 0.3 | V |
| Operating temperature range | Tpnl | -10 | | 70 | °C |

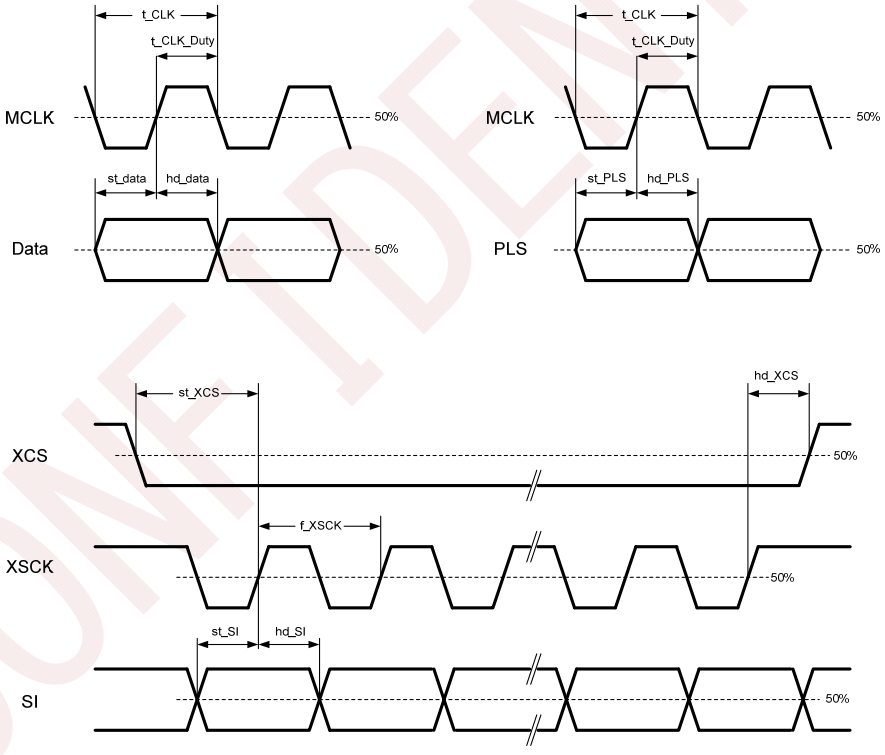
## Electrical Characteristics

### 1. DC Characteristics

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High level input voltage | VIH | | 0.7VDD1 | | VDD1 | V |
| Low level input voltage | VIL | | 0 | | 0.3VDD1 | V |
| High level input voltage | Vt+ | Schmitt input | 0.7VDD1 | | VDD1 | V |
| Low level input voltage | Vt- | Schmitt input | 0 | | 0.3VDD1 | V |
| Vt+ - Vt- | Vhys | Schmitt input | | 0.50 | | V |
| Logic high level output voltage | VOH | | VDD1-0.4 | | | V |
| Logic low level output voltage | VOL | | | | 0.4 | V |

## 2. AC Characteristics

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock pulse cycle | t_CLK | | 18.3 | 18.5 | | ns |
| Clock duty | t_CLK_duty | All mode (54 MHz) common | 40 | 50 | 60 | % |
| Data setup time | st_Data | Vi = 1.62 to 1.98 V | 2.5 | | | ns |
| Data hold time | hd_Data | Vi = 1.62 to 1.98 V | 1.8 | | | ns |
| Control pulse setup time | st_PLS | Vi = 1.62 to 1.98 V | 2.5 | | | ns |
| Control pulse hold time | hd_PLS | Vi = 1.62 to 1.98 V | 1.8 | | | ns |
| XSCK frequency | f_SCLK | | | 0.8 | 2.5 | MHz |
| XCS setup time | st_XCS | | 0.4 | | | µs |
| XCS hold time | hd_XCS | | 0.2 | | | µs |
| SI setup time | st_SI | | 0.2 | | | µs |
| SI hold time | hd_SI | | 0.2 | | | µs |




## 3. Power Consumption

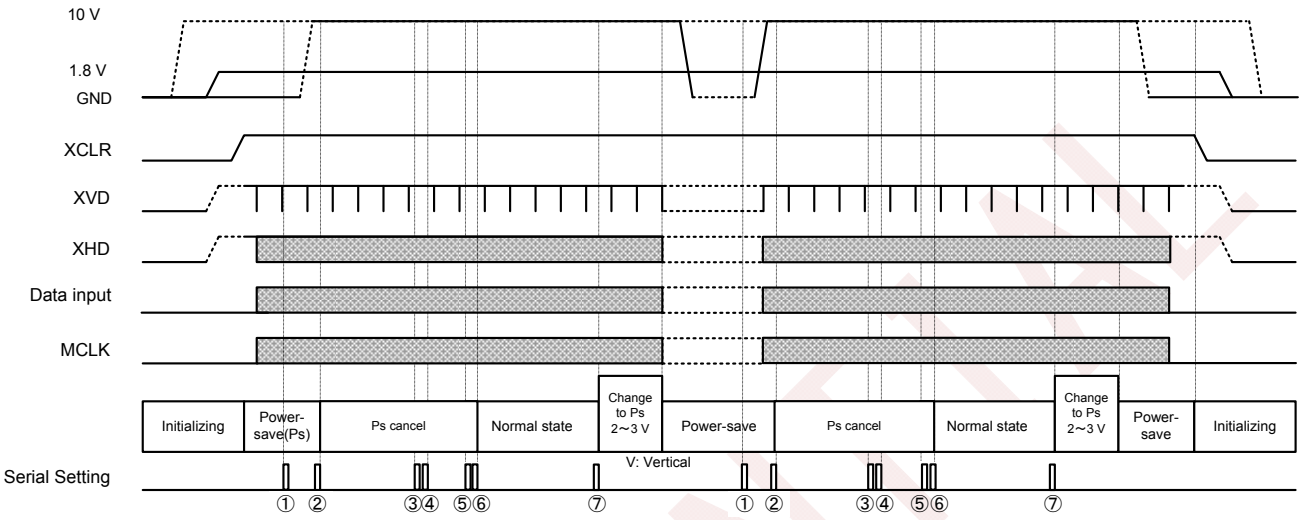
| Item | Symbol | Conditions | Typ. | | | Unit |
|---|---|---|---|---|---|---|
| | | | 300cd/m$^2$ | 200cd/m$^2$ | Standby | |
| VDD1 power consumption | DIDD1 | Tpnl = 40°C (*) | 11 | | 0 | mW |
| VDD2 power consumption | DIDD2 | | 235 | 195 | 2 | mW |
| Total | DITTL | | 246 | 206 | 2 | mW |

*: All white raster display, clock frequency=54MHz, frame rate=60Hz

## Power Supply Sequence

Be sure to follow the power supply sequences noted below to prevent panel damage due to abnormal currents to the panel internal circuits.

### 1. Sequence Diagram




| Serial Setting① | |
|---|---|
| Address | Data (Hex) |
| 0x00 | |
| 0x03 | 80 |
| 0x04 | 5F |
| 0x53 | 02 |
| 0x54 | E7 |
| 0x5B | 4F |
| 0x5C | 4D |

| Serial Setting② | |
|---|---|
| Address | Data (Hex) |
| 0x00 | 0F |
| | |
| | |
| | |
| | |
| | |
| | |

| Serial Setting③ | |
|---|---|
| Address | Data (Hex) |
| | |
| | |
| 0x04 | 1F |
| | |
| | |
| | |
| | |

| Serial Setting④ | |
|---|---|
| Address | Data (Hex) |
| | |
| | |
| | |
| | |
| | |
| 0x5B | 00 |
| 0x5C | 00 |

| Serial Setting⑤ | |
|---|---|
| Address | Data (Hex) |
| | |
| | |
| | |
| 0x53 | 00 |
| 0x54 | E0 |
| | |
| | |

| Serial Setting⑥ | |
|---|---|
| Address | Data (Hex) |
| | |
| 0x03 | 00 |
| | |
| | |
| | |
| | |
| | |

| Serial Setting⑦ | |
|---|---|
| Address | Data (Hex) |
| 0x00 | 0E |
| | |
| | |
| | |
| | |
| | |
| | |

### 2. Power On Sequence

1. Set XCLR to low and turn on 1.8V power supply, then the panel is initialized.
2. Set XCLR to high 1msec after 1.8V turning on completion, then the panel is in power-saving mode.
3. Perform the serial setting ①
4. Set power -saving mode off (serial setting ②).
5. Perform the serial setting ③ later than 4V(Vertical) after power-saving mode off setting ② completion.
6. Perform the serial setting ④ later than 3ms after serial setting ③ completion.
7. Perform the serial setting ⑤ later than 1V(Vertical) after the serial setting ④ completion.
8. Perform the serial setting ⑥

Complete turning on of 1.8V and 10V power supply before power saving mode off setting ②, while the order of turning on of 1.8V and 10V power supply is not restricted.

### 3. Power Off Sequence

1. Set power-saving on (serial setting ⑦).

2. After power-saving mode starts, set XCLR to low and turn off 1.8V and 10V power supplies.

Complete turning off of 1.8V power supply after setting XCLR to low, while the order of turning off of 1.8V and 10V power supply is not restricted.

## Description of Functions

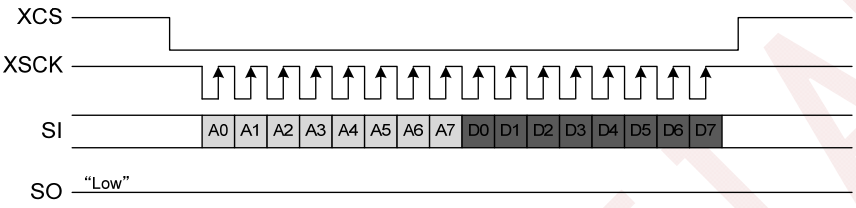
### 1. Tcon Block

#### 1.1. Serial I/F Transfer Timing

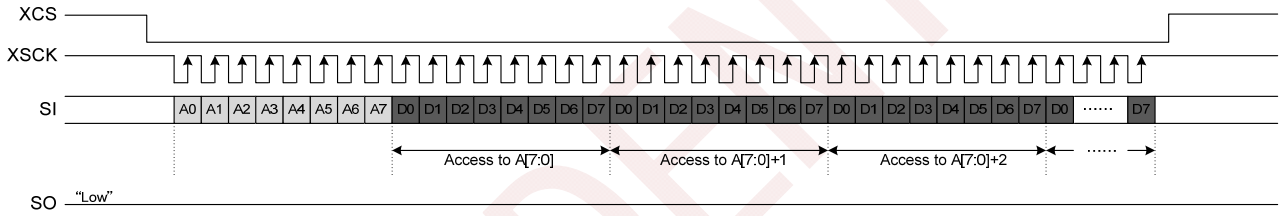
◆Write

Serial communication (normal / burst transfer, LSB first) is supported for write operation.

Timing is shown below.




Write access normal transfer (LSB First)




Write access burst transfer (LSB First)

◆ Read

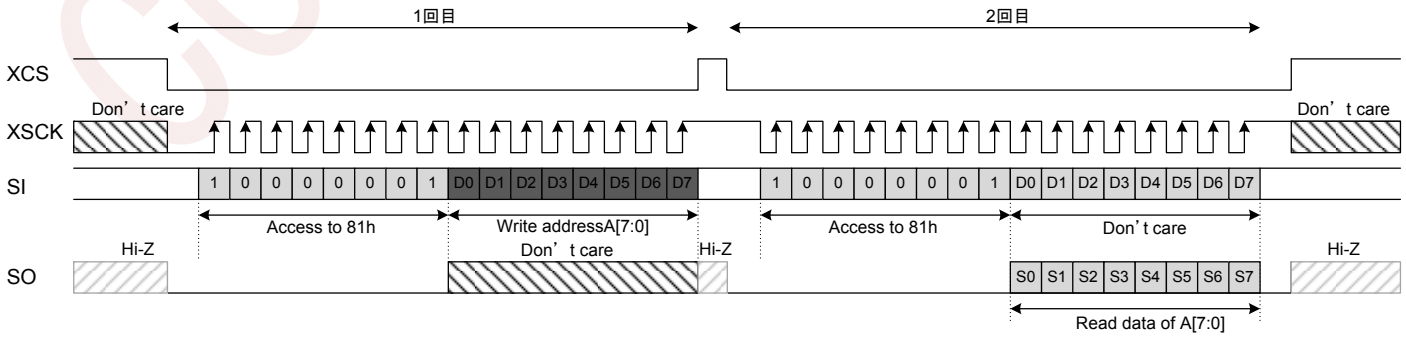
Serial communication (normal transfer, LSB first) is supported for read operation.

Set RD_ON(0x80) to 1, and then perform 2 times serial communication.

1st: Write the address of read data on RD_ADDR (0x81).

2nd: Read data is output from SO (pin no.45) after data access.

Timing is shown below




Read access normal transfer (LSB First)

### 1.3. Register Map

| | Addr. | DATA7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | +0x00 | RGB_YCB | YCB_DEC | 0 | 0 | DWN | RGT | MCLKPOL | PS0 |
| 1 | +0x01 | VCAL_MON | CALSEL[1:0] | | YCB_P | 0 | 0 | 0 | 0 |
| 2 | +0x02 | 1 | 1 | 0 | ORBIT_H[4:0] | | | | |
| 3 | +0x03 | TMPEN | T_SLOPE | DITHER_ON | ORBIT_V[4:0] | | | | |
| 4 | +0x04 | 0 | LDOEXT | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | +0x05 | 0 | 0 | 0 | 0 | 1 | LUMINANCE[2:0] | | |
| 6 | +0x06 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | +0x07 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | +0x08 | 0 | 0 | 0 | 0 | 0 | OTPCALDAC_REGDIS | 0 | OTPDG_REGDIS |
| 9 | +0x09 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| A | +0x0A | 0 | 0 | 0 | DRGAMMA32[4:0] | | | | |
| B | +0x0B | 0 | 0 | 0 | DRGAMMA64[4:0] | | | | |
| C | +0x0C | 0 | 0 | 0 | DRGAMMA128[4:0] | | | | |
| D | +0x0D | 0 | 0 | 0 | DRGAMMA256[4:0] | | | | |
| E | +0x0E | 0 | 0 | 0 | DGGAMMA32[4:0] | | | | |
| F | +0x0F | 0 | 0 | 0 | DGGAMMA64[4:0] | | | | |
| 10 | +0x10 | 0 | 0 | 0 | DBGAMMA32[4:0] | | | | |
| 11 | +0x11 | 0 | 0 | 0 | DBGAMMA64[4:0] | | | | |
| 12 | +0x12 | 0 | 0 | 0 | DBGAMMA128[4:0] | | | | |
| 13 | +0x13 | 0 | 0 | 0 | DBGAMMA256[4:0] | | | | |
| 14 | +0x14 | CONT[7:0] | | | | | | | |
| 15 | +0x15 | CONT[8] | RCONT[6:0] | | | | | | |
| 16 | +0x16 | 0 | GCONT[6:0] | | | | | | |
| 17 | +0x17 | 0 | BCONT[6:0] | | | | | | |
| 18 | +0x18 | BRT[7:0] | | | | | | | |
| 19 | +0x19 | 0 | RBRT[6:0] | | | | | | |
| 1A | +0x1A | 0 | GBRT[6:0] | | | | | | |
| 1B | +0x1B | 0 | BBRT[6:0] | | | | | | |
| 1C | +0x1C | 0 | 0 | 0 | LDOSEL[4:0] | | | | |
| 1D | +0x1D | CALDAC[7:0] | | | | | | | |
| 1E | +0x1E | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1F | +0x1F | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 20 | +0x20 | H_ACT_U[7:0] | | | | | | | |
| 21 | +0x21 | H_ACT_U[8] | 0 | V_ACT_D[9:8] | | 0 | H_ACT_D[10:8] | | |
| 22 | +0x22 | H_ACT_D[7:0] | | | | | | | |
| 23 | +0x23 | V_ACT_U[7:0] | | | | | | | |
| 24 | +0x24 | V_ACT_D[7:0] | | | | | | | |
| 25 | +0x25 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 26 | +0x26 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 27 | +0x27 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28 | +0x28 | 0 | DE_D[10:8] | | | 0 | DE_U[10:8] | | |
| 29 | +0x29 | DE_U[7:0] | | | | | | | |
| 2A | +0x2A | DE_D[7:0] | | | | | | | |
| 2B | +0x2B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2C | +0x2C | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2D | +0x2D | 0 | 0 | WSST1_D[9:8] | | 0 | 0 | WSST1_U[9:8] | |
| 2E | +0x2E | WSST1_U[7:0] | | | | | | | |
| 2F | +0x2F | WSST1_D[7:0] | | | | | | | |
| 30 | +0x30 | 0 | 0 | WSST2_D[9:8] | | 0 | 0 | WSST2_U[9:8] | |
| 31 | +0x31 | WSST2_U[7:0] | | | | | | | |
| 32 | +0x32 | WSST2_D[7:0] | | | | | | | |
| 33 | +0x33 | WSEN1_U[7:0] | | | | | | | |
| 34 | +0x34 | WSEN1_W[7:0] | | | | | | | |
| 35 | +0x35 | 0 | 0 | 0 | 0 | 0 | WSEN2_U[10:8] | | |
| 36 | +0x36 | WSEN2_U[7:0] | | | | | | | |
| 37 | +0x37 | WSEN2_W[7:0] | | | | | | | |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 38 | +0x38 | WSEN3_U[7:0] | | | | | | | |
| 39 | +0x39 | WSEN3_W[7:0] | | | | | | | |
| 3A | +0x3A | DSEN_U[7:0] | | | | | | | |
| 3B | +0x3B | 0 | 0 | 0 | 0 | 0 | DSEN_W[10:8] | | |
| 3C | +0x3C | DSEN_W[7:0] | | | | | | | |
| 3D | +0x3D | 0 | 0 | VCK_W[9:8] | | 0 | 0 | VCK_U[9:8] | |
| 3E | +0x3E | VCK_U[7:0] | | | | | | | |
| 3F | +0x3F | VCK_W[7:0] | | | | | | | |
| 40 | +0x40 | 0 | 0 | 0 | 0 | 0 | 0 | SIGSELREF_U[9:8] | |
| 41 | +0x41 | SIGSELREF_U[7:0] | | | | | | | |
| 42 | +0x42 | SIGSELREF_W[7:0] | | | | | | | |
| 43 | +0x43 | 0 | 0 | 0 | 0 | SIGSELOFS_U[3:0] | | | |
| 44 | +0x44 | SIGSELOFS_W[7:0] | | | | | | | |
| 45 | +0x45 | 0 | 0 | SGISEL_W[9:8] | | SIGSEL_U[3:0] | | | |
| 46 | +0x46 | SIGSEL_W[7:0] | | | | | | | |
| 47 | +0x47 | 0 | 0 | 0 | 0 | 0 | 0 | SELREF_U[9:8] | |
| 48 | +0x48 | SELREF_U[7:0] | | | | | | | |
| 49 | +0x49 | SELREF_W[7:0] | | | | | | | |
| 4A | +0x4A | SELOFS_U[7:0] | | | | | | | |
| 4B | +0x4B | SELOFS_W[7:0] | | | | | | | |
| 4C | +0x4C | 0 | 0 | SEL_W[9:8] | | 0 | 0 | SEL_U[9:8] | |
| 4D | +0x4D | SEL_U[7:0] | | | | | | | |
| 4E | +0x4E | SEL_W[7:0] | | | | | | | |
| 4F | +0x4F | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 50 | +0x50 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 51 | +0x51 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 52 | +0x52 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 53 | +0x53 | 120MODE | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 54 | +0x54 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 55 | +0x55 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 56 | +0x56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 57 | +0x57 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 58 | +0x58 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 59 | +0x59 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5A | +0x5A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5B | +0x5B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5C | +0x5C | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5D | +0x5D | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5E | +0x5E | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5F | +0x5F | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 60 | +0x60 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 61 | +0x61 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 62 | +0x62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 63 | +0x63 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 64 | +0x64 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 65 | +0x65 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 66 | +0x66 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 67 | +0x67 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | | | | | | | | | |
| 80 | +0x80 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RD_ON |
| 81 | 0x81 | RD_ADDR[7:0] | | | | | | | |

### 1.4. Description of Registers

| Register name | Number of bits | V sync | Function |
|---|---|---|---|
| PS0 | 1 | | Power Save Mode<br>0: Power Save on<br>1: Power Save off |
| MCLKPOL | 1 | | MCLK polarity switching<br>0: Negative polarity<br>1: Positive polarity |
| RGT | 1 | | 0: Left scan<br>1: Right scan |
| DWN | 1 | | 0: Upper scan<br>1: Lower scan |
| YCB_DEC | 1 | | YCbCr/YPbPr conversion switching<br>0: YCbCr (conforms to BT601)<br>1: YPbPr (conforms to BT709) |
| RGB_YCB | 1 | | RGB/YCbCr input format selection<br>0: RGB<br>1: YCbCr/YPbPr |
| YCB_P | 1 | ○ | YCbCr/YPbPr input pattern switching<br>0: Cb/Pb First (Mode A)<br>1: Cr/Pr First (Mode B) |
| CALSEL | 2 | | VCAL output selection<br>01: V1 output<br>10: V2 output<br>11: VOUT attenuate output (VGAM4 × 0.25[V]) |
| VCAL_MON | 1 | | Temperature sensing circuit monitoring<br>0: Invalid<br>1: Valid |
| ORBIT_H | 5 | ○ | Horizontal orbit adjustment<br>-10 to 0 to +10,<br>Default: 0x00 |
| ORBIT_V | 5 | ○ | Vertical orbit adjustment<br>-10 to 0 to +10,<br>Default: 0x00 |
| DITHERON | 1 | | Dithering On/Off<br>0: Dithering Off<br>1: Dithering On |
| LDOEXT | 1 | | LDO external / internal selection<br>0: Internal (normally fixed to 0)<br>1: External |
| LUMINANCE | 3 | | Luminance and white chromaticity preset mode selection |
| OTPDG_REGDIS | 1 | | White chromaticity adjustment<br>0: Preset mode valid<br>1: Preset mode invalid (CONT/BRT adjustment) |
| OTPCALDAC_REGDIS | 1 | | Luminance adjustment<br>0: Preset mode valid<br>1: Preset mode invalid (CALDAC adjustment) |
| DRGAMMA32 | 5 | | Red 32 gray scale chromaticity adjustment |
| DRGAMMA64 | 5 | | Red 64 gray scale chromaticity adjustment |
| DRGAMMA128 | 5 | | Red 128 gray scale chromaticity adjustment |
| DRGAMMA256 | 5 | | Red 256 gray scale chromaticity adjustment |
| DGGAMMA32 | 5 | | Green 32 gray scale chromaticity adjustment |
| DGGAMMA64 | 5 | | Green 64 gray scale chromaticity adjustment |

| Register name | Number of bits | V sync | Function |
|---|---|---|---|
| DBGAMMA32 | 5 | | Blue 32 gray scale chromaticity adjustment |
| DBGAMMA64 | 5 | | Blue 64 gray scale chromaticity adjustment |
| DBGAMMA128 | 5 | | Blue 128 gray scale chromaticity adjustment |
| DBGAMMA256 | 5 | | Blue 256 gray scale chromaticity adjustment |
| CONT | 9 | | Contrast adjustment |
| RCONT | 7 | | R sub-contrast adjustment |
| GCONT | 7 | | G sub-contrast adjustment |
| BCONT | 7 | | B sub-contrast adjustment |
| BRT | 8 | | Brightness adjustment |
| RBRT | 7 | | R sub-brightness adjustment |
| GBRT | 7 | | G sub-brightness adjustment |
| BBRT | 7 | | B sub-brightness adjustment |
| LDOSEL | 5 | | LDO output voltage adjustment |
| CALDAC | 8 | | Luminance adjustment setting<br>7mV/step |
| H_ACT_U | 8 | | Input signal exchange position |
| H_ACT_D | 11 | | Input signal exchange position |
| V_ACT_U | 8 | | Input signal exchange position |
| V_ACT_D | 10 | | Input signal exchange position |
| DE_U | 11 | | Timing setting register |
| DE_D | 11 | | Timing setting register |
| WSST1_U | 10 | | Timing setting register |
| WSST1_D | 10 | | Timing setting register |
| WSST2_U | 10 | | Timing setting register |
| WSST2_D | 10 | | Timing setting register |
| WSEN1_U | 8 | | Timing setting register |
| WSEN1_W | 8 | | Timing setting register |
| WSEN2_U | 11 | | Timing setting register |
| WSEN2_W | 8 | | Timing setting register |
| WSEN3_U | 8 | | Timing setting register |
| WSEN3_W | 8 | | Timing setting register |
| DESN_U | 8 | | Timing setting register |
| DSEN_W | 11 | | Timing setting register |
| VCK_U | 10 | | Timing setting register |
| VCK_W | 10 | | Timing setting register |
| SIGSELREF_U | 10 | | Timing setting register |

| Register name | Number of bits | V sync | Function |
|---|---|---|---|
| SIGSELREF_W | 8 | | Timing setting register |
| SIGSELOFS_U | 4 | | Timing setting register |
| SIGSELOFS_W | 8 | | Timing setting register |
| SIGSEL_U | 4 | | Timing setting register |
| SIGSEL_W | 10 | | Timing setting register |
| SELREF_U | 10 | | Timing setting register |
| SELREF_W | 8 | | Timing setting register |
| SELOFS_U | 8 | | Timing setting register |
| SELOFS_W | 8 | | Timing setting register |
| SEL_U | 10 | | Timing setting register |
| SEL_W | 10 | | Timing setting register |
| 120MODE | 1 | | 120Hz mode |
| RD_ON | 1 | | Register read<br>0: Invalid<br>1: Valid |
| RD_ADDR | 8 | | Register read address setting |

## 2. Video Signal Transfer Format

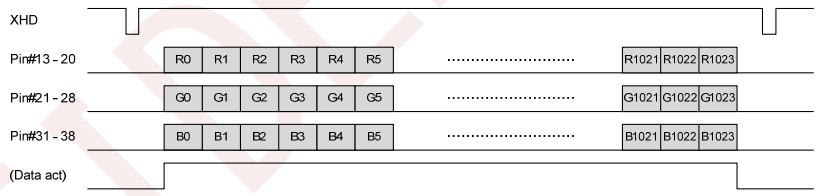
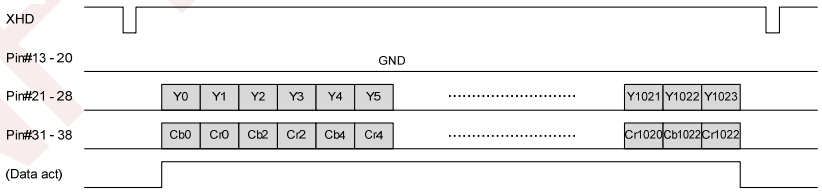
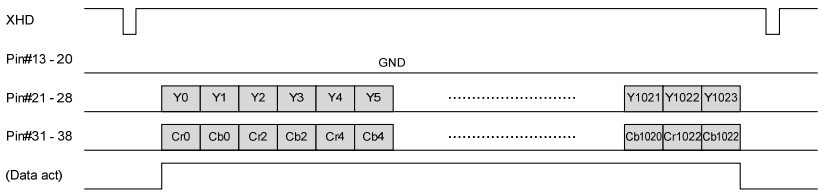
Set the registers appropriately for the video signal transfer format according to the table below.

◆Register Settings

| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x00h | RGB_YCB | 1 | Selection of RGB / YCbCr (YPbPr) format<br>0: RGB (default)<br>1: YCbCr and YPbPr |
| 0x00h | YCB_DEC | 1 | Selection of YCbCr / YPbPr conversion<br>0: YCbCr (BT. 601) (default)<br>1: YPbPr (BT. 709) |
| 0x01h | YCB_P | 1 | Selection of YCbCr (YPbPr) input pattern<br>0: Cb and Pb first (default)<br>1: Cr and Pr first |

◆Register settings for each video signal transfer formats when YCB_DEC=0.

*Cb and Cr are replaced by Pb and Pr respectively when YCB_DEC=1.

<table>
<tr><th colspan="2">Register Setting</th><th rowspan="2">Video signal transfer format</th></tr>
<tr><th>RGB_YCB</th><th>YCB_P</th></tr>
<tr><td>0</td><td>—</td><td> 
</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td> 
</td></tr>
<tr><td>1</td><td> 
</td></tr>
</table>

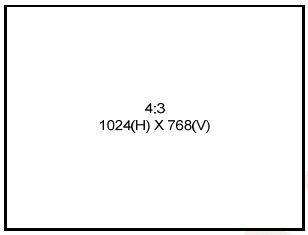
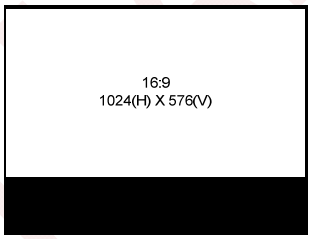
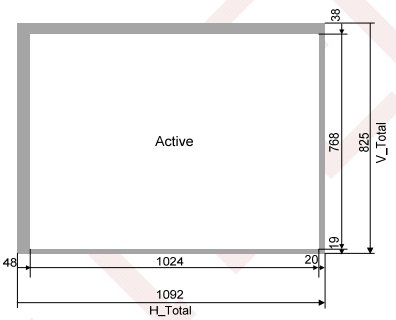
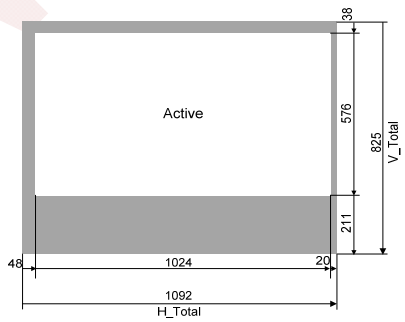
### 3. Input Signal Format and Timing Settings

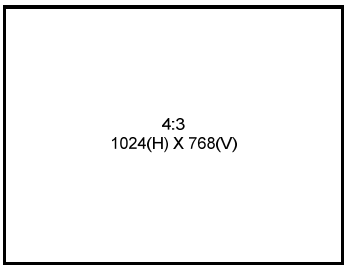
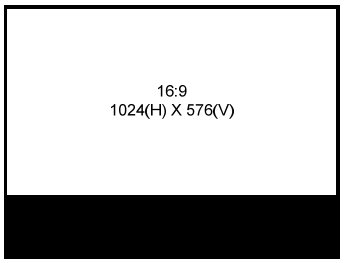
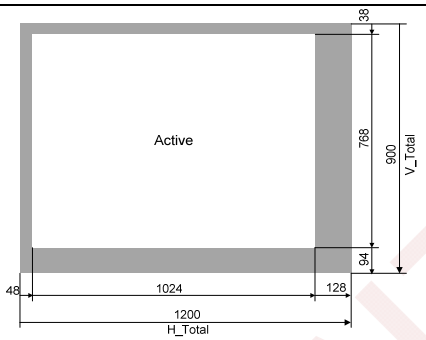
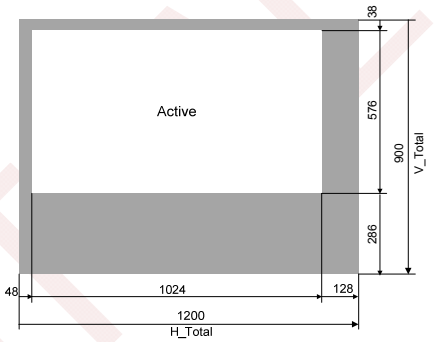
Set the panel timing in accordance with the input signal format.

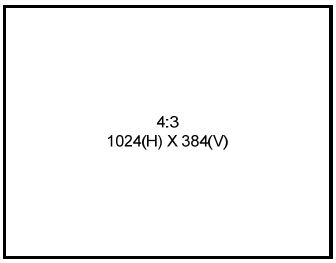
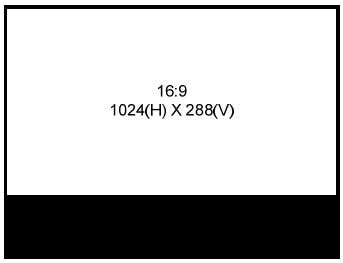
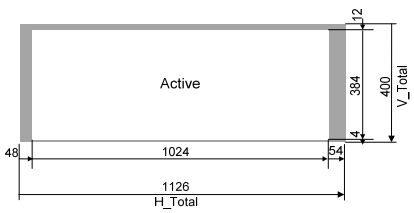
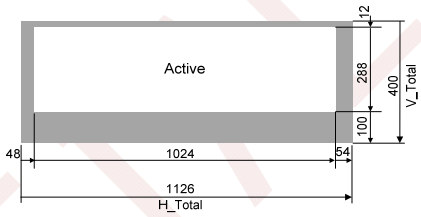
◆Register Settings

| Address | Register name | Bits | Function |
|---|---|---|---|
| 0x20h<br>\|<br>0x4Eh | H_ACT_U<br>\|<br>SEL_W | | Timing setting registers.<br>Should be set appropriately for the input signal data format.<br>Setting values are separately presented. |

◆Panel Display Modes and Input Supported Formats

| | | ①4:3<br>59.94Hz Frame Rate | ②16:9<br>59.94Hz Frame Rate |
|---|---|---|---|
| Panel Display Mode | |  |  |
| Input Supported Format | |  |  |
| Active | H | 1024 | 1024 |
| | V | 768 | 576 |
| Total | H | 1092 | 1092 |
| | V | 825 | 825 |
| FP | H | 20 | 20 |
| | V | 19 | 211 |
| SYNC | H | 16 | 16 |
| | V | 6 | 6 |
| BP | H | 32 | 32 |
| | V | 32 | 32 |
| BP+SYNC | H | 48 | 48 |
| | V | 38 | 38 |
| fv | Hz | 59.94 | 59.94 |
| Th | μs | 20.2 | 20.2 |
| Clock | MHz | 54 | 54 |

| | | ③4:3<br>50Hz Frame Rate | ④16:9<br>59.94Hz Frame Rate |
|---|---|---|---|
| Panel Display Mode | |  |  |
| Input Supported Format | |  |  |
| Active | H | 1024 | 1024 |
| | V | 768 | 576 |
| Total | H | 1200 | 1200 |
| | V | 900 | 900 |
| FP | H | 128 | 128 |
| | V | 94 | 286 |
| SYNC | H | 16 | 16 |
| | V | 6 | 6 |
| BP | H | 32 | 32 |
| | V | 32 | 32 |
| BP+SYNC | H | 48 | 48 |
| | V | 38 | 38 |
| fv | Hz | 50 | 50 |
| Th | µs | 22.2 | 22.2 |
| Clock | MHz | 54 | 54 |

| | | ⑤4:3<br>119.88Hz Frame Rate | ⑥16:9<br>119.88Hz Frame Rate |
|---|---|---|---|
| Panel Display mode | |  |  |
| Input Supported Format | |  |  |
| Active | H | 1024 | 1024 |
| | V | 384 | 288 |
| Total | H | 1126 | 1126 |
| | V | 400 | 400 |
| FP | H | 54 | 54 |
| | V | 4 | 100 |
| SYNC | H | 16 | 16 |
| | V | 1 | 1 |
| BP | H | 32 | 32 |
| | V | 11 | 11 |
| BP+SYNC | H | 48 | 48 |
| | V | 12 | 12 |
| fv | Hz | 119.88 | 119.88 |
| Th | µs | 20.9 | 20.9 |
| Clock | MHz | 53.99 | 53.99 |

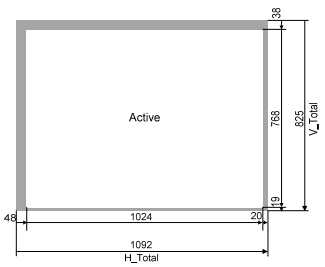
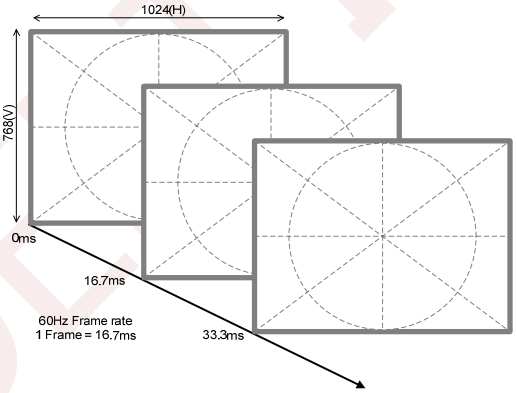
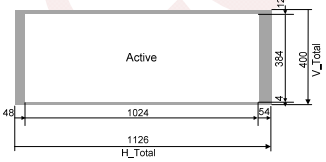
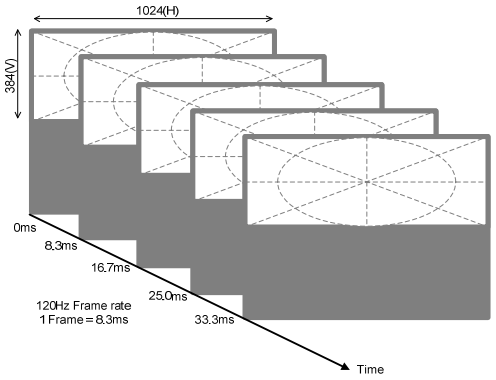
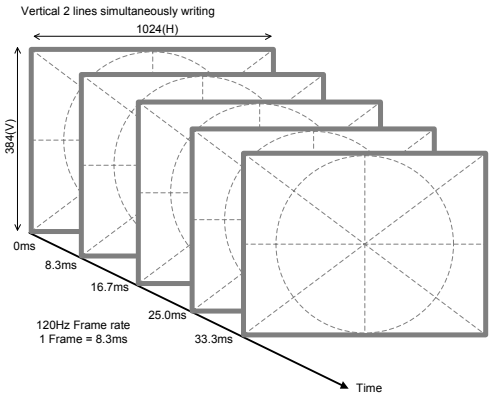
## 4. 120Hz mode

In order to reduce latency and to alleviate motion-blur effect, there is 120Hz mode in this panel module. With this 120Hz mode, it is available to display as 120Hz refresh rate. In this case, vertical resolution should be half of full scan lines because writing 2line simultaneously with same data. Please refer input format ⑤ and ⑥ in table below.

◆Register setting

| Address | Register | Bit | Function |
|---|---|---|---|
| 0x53h | 120MODE | 1 | 120Hz mode<br>0: Off<br>1: On |

◆Input format and display image

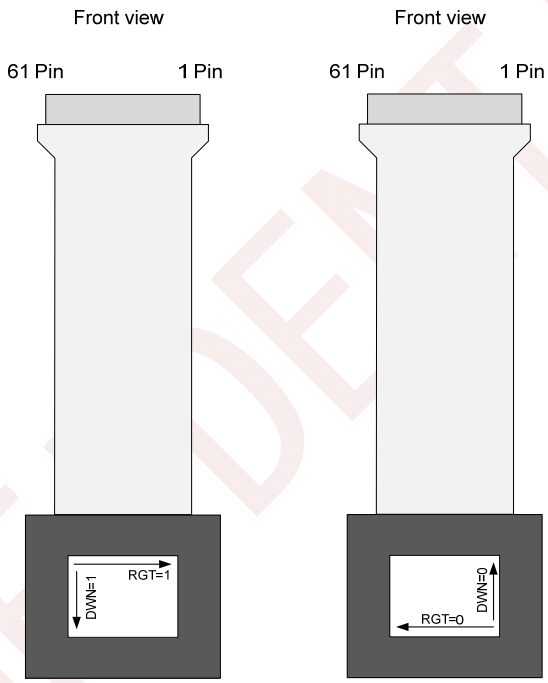
| Input format | 120MODE | Display image |
|---|---|---|
| ①1024 x 768 59.94Hz   | 0:Off |   |
| ⑤ 1024 x 384 119.88Hz   | 0:Off |   |
| | 1:On |   |

### 5. Up/down and/or Right/left Inversion Function

Up/down and right/left inverse display of the panel are set by the registers RGT and DWN, respectively.

◆Register Settings

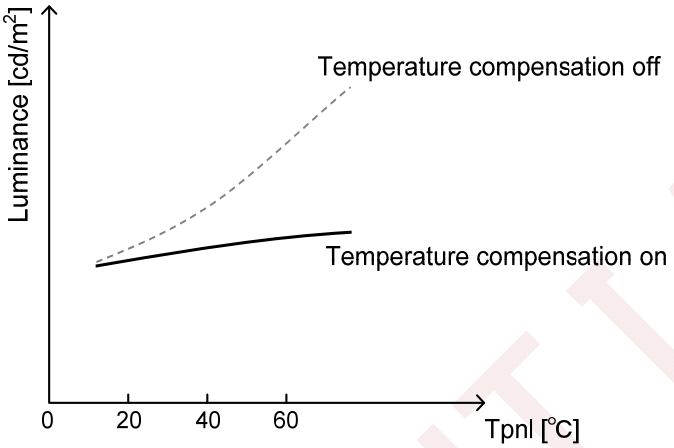
| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x00h | RGT | 1 | 0: Left scan<br>1: Right scan |
| 0x00h | DWN | 1 | 0: Upper scan<br>1: Lower scan |



## 6. Luminance Temperature Compensation Function

Organic EL panels have characteristics such that the luminance changes according to the temperature.

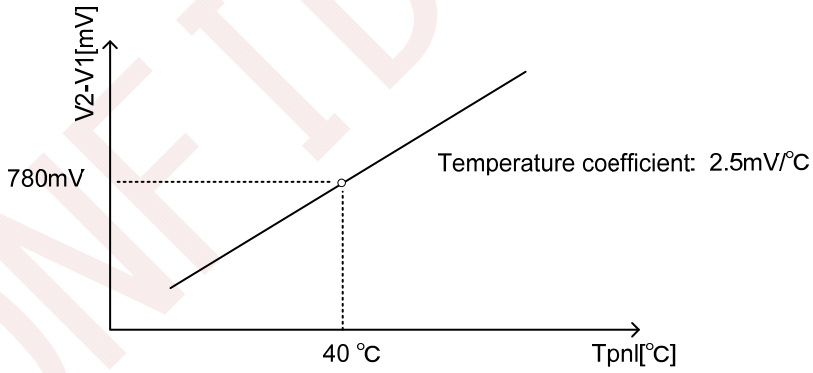
This product has a function that compensates the temperature dependence of the panel luminance.




◆Method of Checking the Panel Temperature

The temperature sensor output voltage can be output from VCAL (output pin 50).

Set the register VCAL_MON to 1: valid, set the register CALSEL as noted above, and read the V1 and V2 outputs. The temperature can be calculated by subtracting V1 from V2.




◆Register Settings

| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x01h | VCAL_MON | 1 | Temperature sensor monitoring<br>0: Invalid<br>1: Valid |
| 0x01h | CALSEL[1:0] | 2 | VCAL output selection<br>01: V1 output<br>10: V2 output<br>11: VOUT attenuate output (TBD) |

## 7. Luminance Adjustment Function

This function adjusts the gamma top voltage according to the register CALDAC setting to adjust the luminance.

◆Register Settings

| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0×1Dh | CALDAC[7:0] | 8 | Luminance adjustment<br>setting value: 1 to 255 (in decimal notation) |

## 8. White Balance Adjustment Function

### 8.1. Contrast/Sub-contrast

This function sets the contrast (gain) of the input signal. RGB simultaneous adjustment and R, G and B separate adjustment can be set.

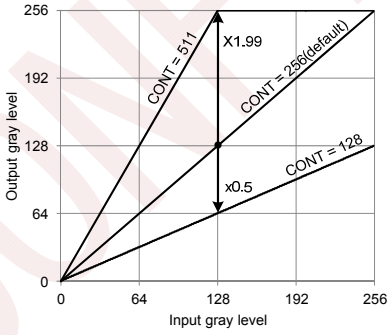
◆ Register Settings

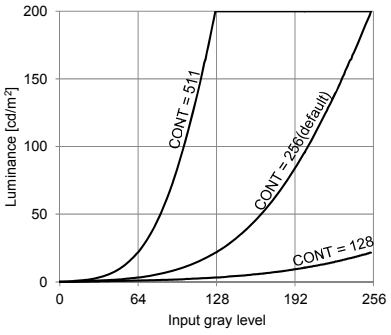
| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x14h, 0x15h | CONT | 9 | To RGB input signal, × 0 ... × 1 (Default) ... × 1.99 |
| 0x15h | RCONT | 7 | Sets R relative to CONT to × 0.75 ... × 1 (Default) ... × 1.24 |
| 0x16h | GCONT | 7 | Sets G relative to CONT to × 0.75 ... × 1 (Default) ... × 1.24 |
| 0x17h | BCONT | 7 | Sets B relative to CONT to ×0.75 ... × 1 (Default) ... ×1.24 |

◆Contrast Adjustment

R, G and B are adjusted simultaneously relative to the input signal using the register CONT. The setting value is 0 to 511 (decimal notation).

| CONT setting value | 0 | … | 128 | … | 256 (Default) | … | 384 | … | 511 |
|---|---|---|---|---|---|---|---|---|---|
| Gain (to input) | × 0 | … | × 0.5 | … | × 1 | … | × 1.5 | … | × 1.99 |



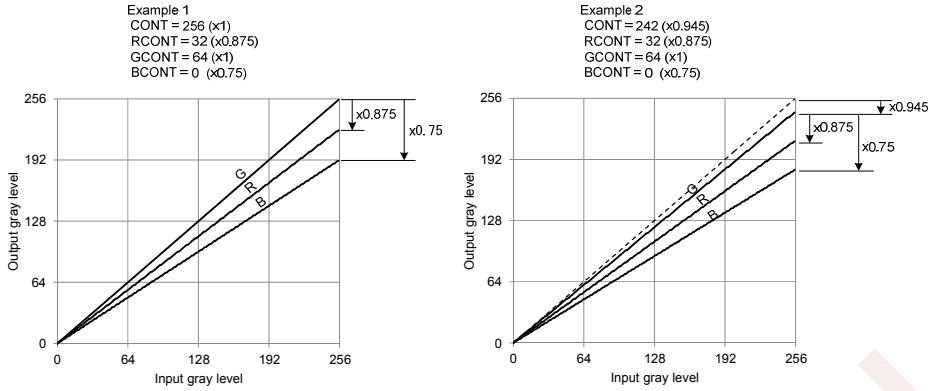




◆Sub Contrast Adjustment

R, G and B are adjusted separately using the registers RCONT, GCONT and BCONT, respectively.

The R, G and B gains can be set separately relative to the main CONT setting. The setting range is 0 to 127 (decimal notation).

| R/G/BCONT setting value | 0 | … | 32 | … | 64 (Default) | … | 96 | … | 127 |
|---|---|---|---|---|---|---|---|---|---|
| Gain (to CONT) | × 0.75 | … | × 0.875 | … | × 1 | … | × 1.125 | … | × 1.24 |




### 8.2. Bright/Sub Bright

This sets the brightness level of the input signal. RGB simultaneous adjustment and R, G and B separate adjustment can be set.

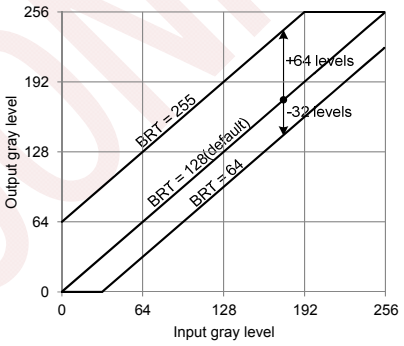
◆Register Settings

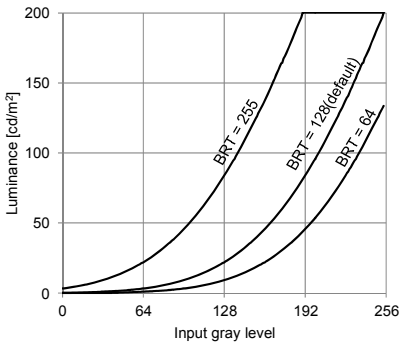
| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x18h | BRT | 8 | To RGB input signal, -64 ... 0 (Default) ... +63 gradations |
| 0x19h | RBRT | 7 | Sets R relative to BRT to -32 ... 0 (Default) ... +31 gradations |
| 0x1Ah | GBRT | 7 | Sets G relative to BRT to -32 ... 0 (Default) ... +31 gradations |
| 0x1Bh | BBRT | 7 | Sets B relative to BRT to -32 ... 0 (Default) ... +31 gradations |

◆Brightness Adjustment

R, G and B are adjusted simultaneously relative to the input signal using register BRT. The setting value is 0 to 255 (decimal notation).

| BRT setting value | 0 | … | 64 | … | 128(Default) | … | 192 | … | 255 |
|---|---|---|---|---|---|---|---|---|---|
| Output gradations (to input) | -64 | … | -32 | … | 0 | … | +32 | … | +63 |



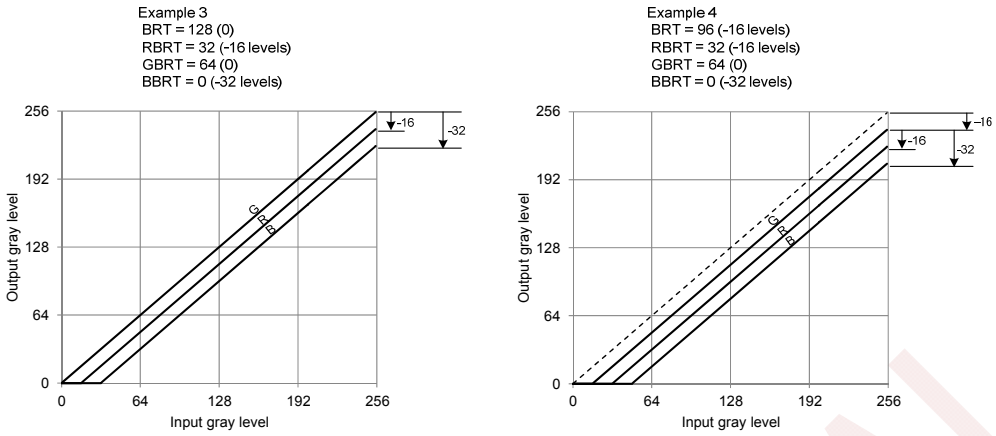




◆Sub Brightness Adjustment

R, G and B are adjusted separately using registers RBRT, GBRT and BBRT, respectively.

The R, G and B adjustments can be set separately relative to the main BRT setting. The setting range is 0 to 127 (decimal notation).

| R/G/BBRT setting value | 0 | … | 32 | … | 64(Default) | … | 96 | … | 127 |
|---|---|---|---|---|---|---|---|---|---|
| Output gradations (to BRT) | -32 | … | -16 | … | 0 | … | +16 | … | +31 |




## 9. Luminance and White Balance Preset Mode

This product has 2 luminance and white balance preset modes.

By selecting the mode according to the register LUMINANCE, the luminance and the white chromaticity are adjusted to preset value.

◆Register Settings

| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x08h | OTPCALDAC_REGDIS | 1 | Luminance adjustment<br>0: Preset mode valid<br>1: Preset mode invalid (CALDAC adjustment) |
| 0x08h | OTPDG_REGDIS | 1 | White chromaticity adjustment<br>0: Preset mode valid<br>1: Preset mode invalid (CONT/BRT adjustment) |
| 0x05h | LUMINANCE[2:0] | 3 | Luminance and white chromaticity preset mode selection<br>0: 200cd/$m^2$, (0.31,0.31)<br>3: 300cd/$m^2$, (0.31,0.31) |

## 10. Dithering Function

This function expresses simulated gradations between the original gradations by using FRC.

This is used to interpolate gradations that decrease due to contrast or brightness adjustment.

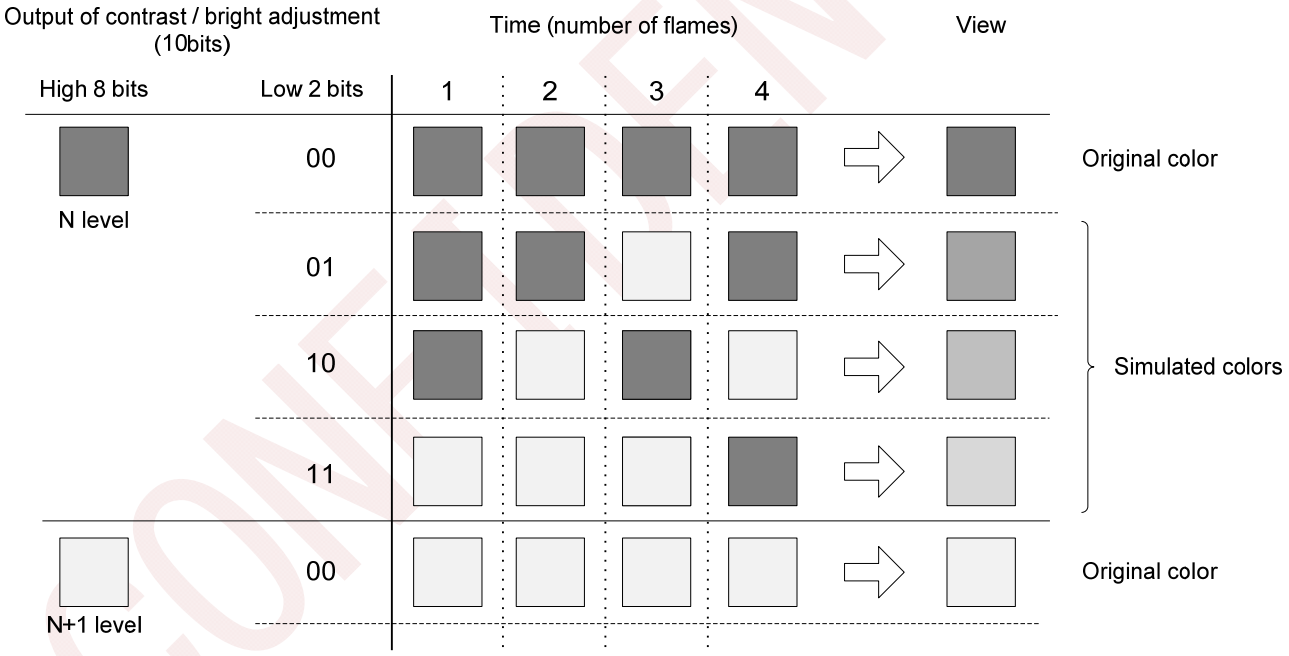
◆Register Settings

| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x03h | DITHERON | 1 | Dithering processing<br>0: Off<br>1: On |

### 10.1. FRC (Frame Rate Control)

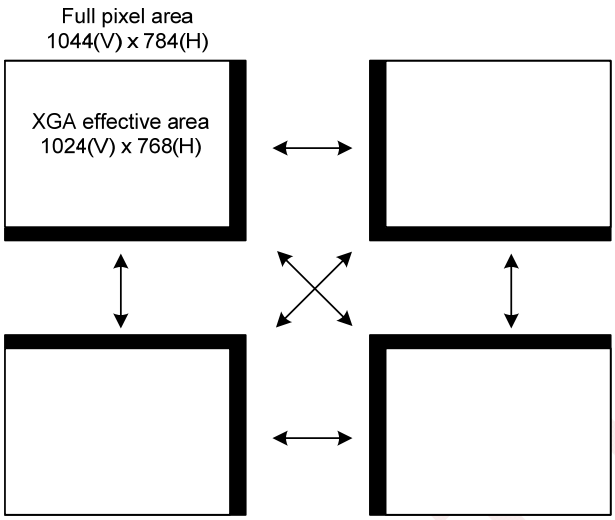
Simulated colors are expressed making use of frame rate and image lag effect of human eyes. When two colors are switching alternately in high-speed, it looks an intermediate color for human eyes. Three simulated colors can be added to original colors by changing data in 4-frame cycle making use of this property (2 bit FRC).

FRC simulated color image when noticing arbitral one pixel is shown below.



## 11. Orbit Function

The image data start position can be changed. This enables reducing of the noticeability of local drops in luminance.




◆Register Settings

| Address | Register name | Number of bits | Function |
|---|---|---|---|
| 0x02h | ORBIT_H[4:0] | 5 | Horizontal orbit adjustment<br>-10 to 0 to +10,<br>Default: 0 |
| 0x03h | ORBIT_V[4:0] | 5 | Vertical orbit adjustment<br>-10 to 0 to +10,<br>Default: 0 |

### 11.1. Horizontal Display Position Shift

The display start position is changed by the register ORBIT_H. The variable range is ± 10 pixels.

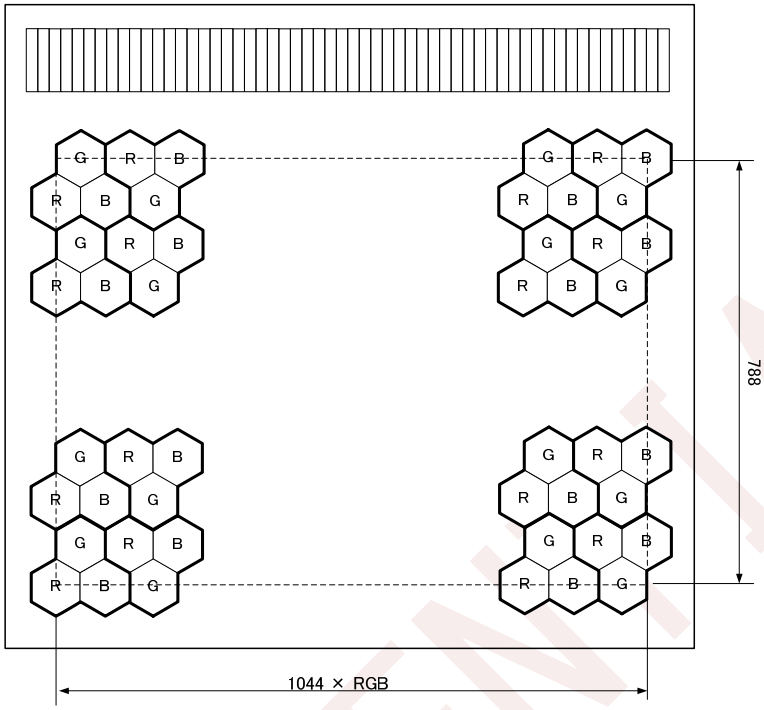
| ORBIT_H setting value | -10 | … | -1 | 0 (Default) | 1 | … | 10 |
|---|---|---|---|---|---|---|---|
| Number of pixels shifted | Leftward 10-pixel | … | Leftward 1-pixel | Center | Rightward 1-pixel | … | Rightward 10-pixel |

### 11.2. Vertical Display Position Shift

The display start position is changed by the register ORBIT_V. The variable range is ± 10 pixels.

| ORBIT_V setting value | -10 | … | -1 | 0 (Default) | 1 | … | 10 |
|---|---|---|---|---|---|---|---|
| Number of pixels shifted | Upward 10-pixels | … | Upward 1-pixel | Center | Downward 1-pixel | … | Downward 10-pixel |

## Pixel Array



## Optical Characteristics

### 1. Optical Characteristics

| Item | | Symbol | Measurement Method | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Luminance | Mode 0 | L0 | 1 | 170 | 200 | 230 | Cd/m$^2$ |
| | Mode 3 | L3 | 1 | 255 | 300 | 345 | Cd/m$^2$ |
| Contrast | | CR | 1 | 10,000 | — | — | |
| Chromaticity | W (L0 & L3) | x | 1 | 0.298 | 0.310 | 0.322 | CIE |
| | | y | 1 | 0.298 | 0.310 | 0.322 | CIE |
| | R | x | 1 | 0.635 | 0.655 | 0.675 | CIE |
| | | y | 1 | 0.310 | 0.330 | 0.350 | CIE |
| | G | x | 1 | 0.255 | 0.275 | 0.295 | CIE |
| | | y | 1 | 0.625 | 0.645 | 0.665 | CIE |
| | B | x | 1 | 0.127 | 0.147 | 0.167 | CIE |
| | | y | 1 | 0.045 | 0.065 | 0.085 | CIE |

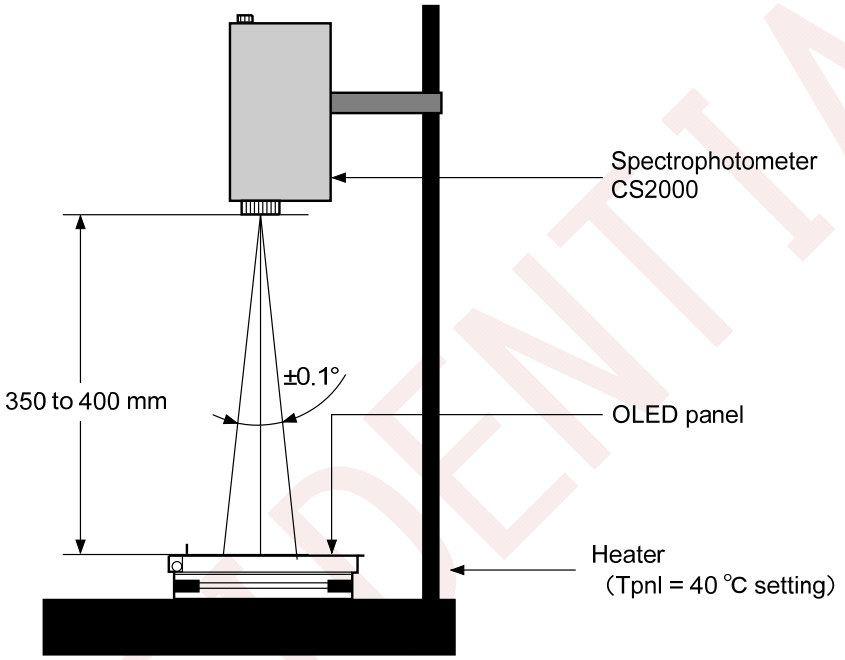
Drive conditions:
OTPDG_REGDIS=0、OTPCALDAC_REGDIS=0,
LUMINANCE=0 (Mode 0), 3 (Mode 3)

## 2. Measurement System・Measurement Method 1

The luminance and chromaticity are measured in Measurement System A shown below.

Measurement temperature: Tpnl = 40°C
Measurement point: One point on the screen center
All white display: All RGB signal data is set to High.
All black display: All RGB signal data is set to Low.

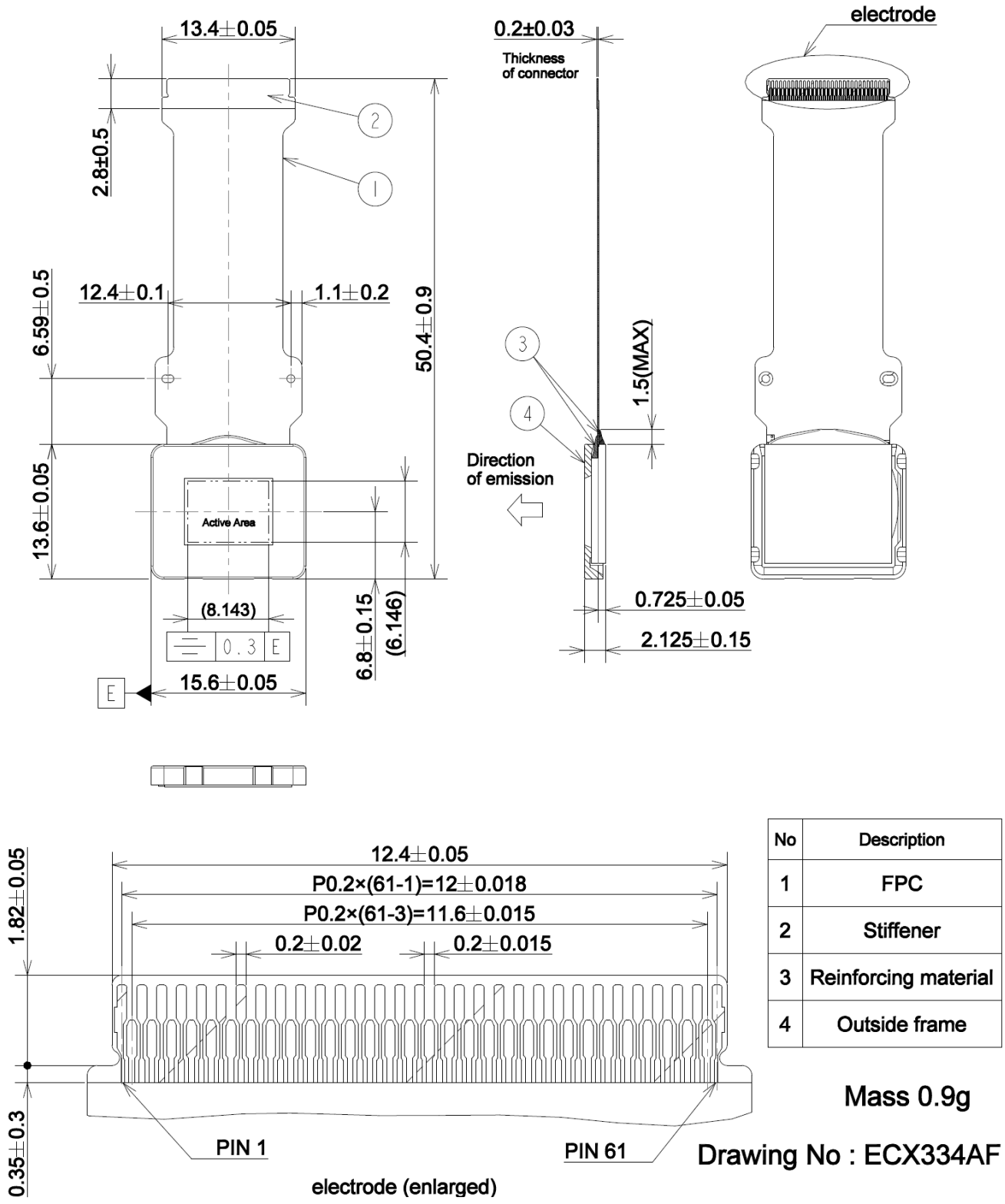
Luminance and chromaticity: Measure the luminance and chromaticity in all white display in Measurement System A.
Contrast: Measure the luminance in all white display (@ Mode3: 300cd/$m^2$) and all black display in Measurement System A, and substitute them into the formula below.
Contrast = Luminance in all white display/Luminance in all black display




System A

## Package Outline

(Unit: mm)




| No | Description |
|---|---|
| 1 | FPC |
| 2 | Stiffener |
| 3 | Reinforcing material |
| 4 | Outside frame |

Mass 0.9g

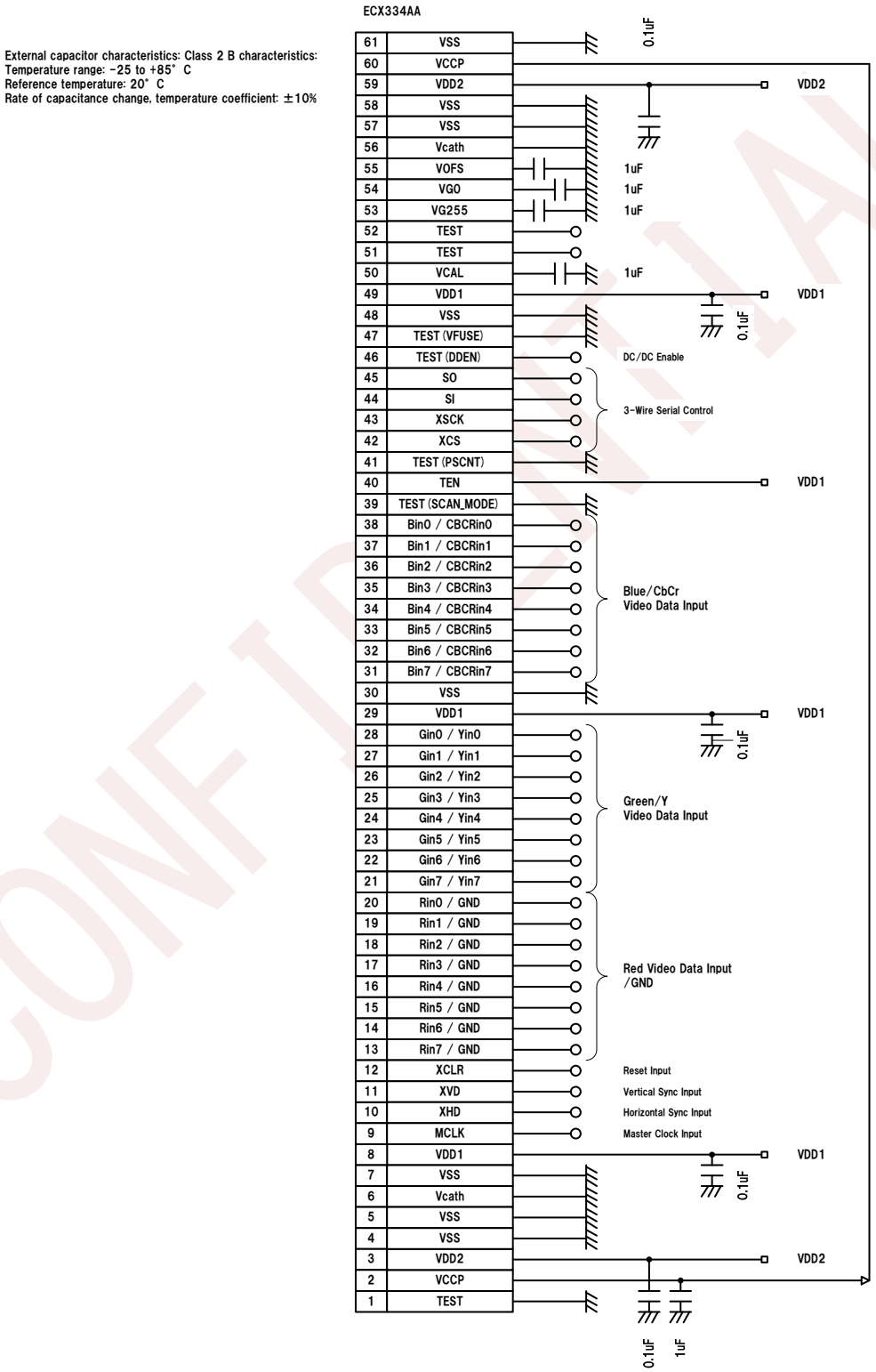
Drawing No : ECX334AF

## Recommended Items

### 1. Peripheral Circuits

The recommended peripheral circuits for the panel pins are shown below.

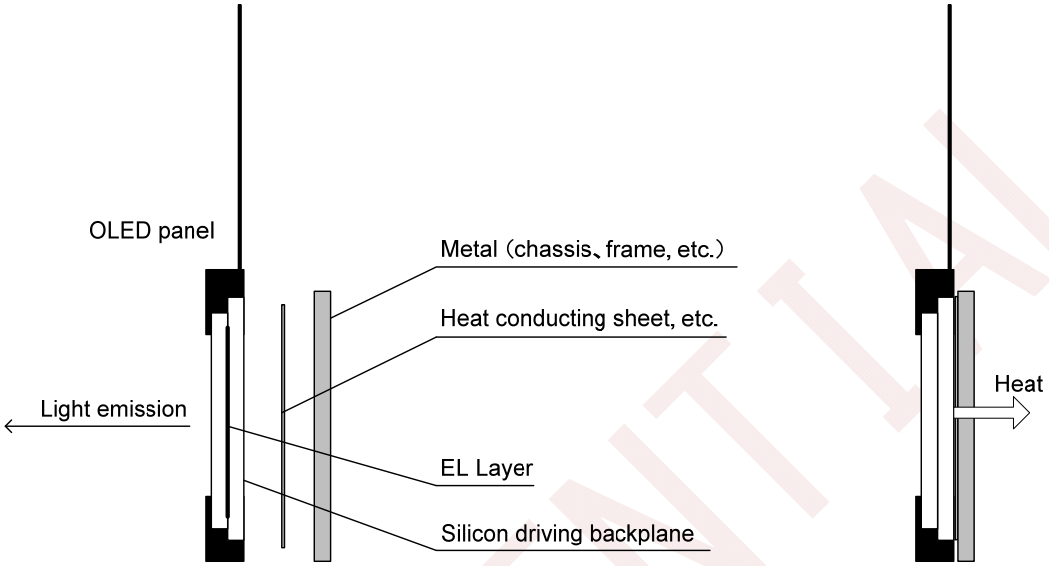
Regarding power supply capacitor connections, mount an approximately 2.2 µF to 10 µF capacitor for each power supply. Insufficient capacitance may affect the picture quality.

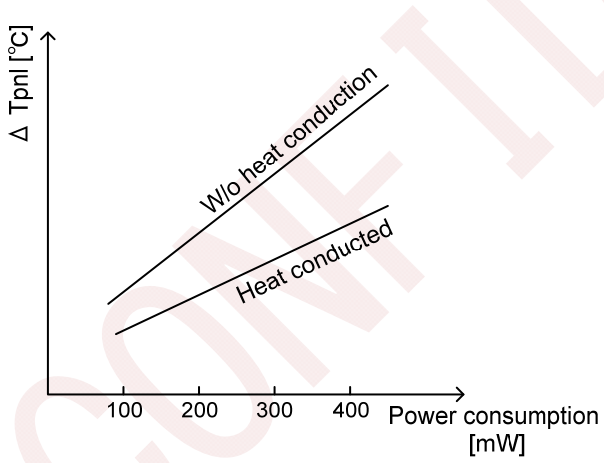


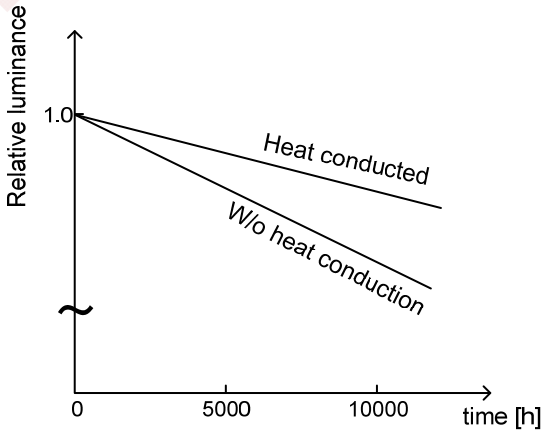
## 2. Suppression of the Panel Temperature

Organic EL panel temperatures rise due to power consumption (heat generation) by the EL emissive layer and the silicon drive board. A rise in the panel temperature may affect the drop in luminance over time.

The rise in panel temperature can be suppressed by establishing a thermal connection between the rear surface (silicon board surface) of the panel and metal (chassis, frame, etc.) in the panel mount area.



## Notes on Handling

1. Static charge prevention

   Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

   (1) Use non-chargeable gloves, use bare hands.
   (2) Use a wrist strap when handling.
   (3) Do not touch any electrodes of the panel.
   (4) Wear non-chargeable clothes and conductive shoes.
   (5) Install grounded conductive mats on the working floor and working table.
   (6) Keep the panel away from any charged materials.

2. Protection from dust and dirt

   (1) Operate in a clean environment.
   (2) Do not touch the panel surface. The surface is easily scratched.
   When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
   (3) Use ionized air to blow dust off the panel surface.

3. Others

   (1) Do not hold the flexible board or twist or bend it because the flexible board connection block is easily affected by twisting.
   (2) The minimum fold radius of the flexible board is 1 mm.
   (3) Do not drop the panel.
   (4) Do not twist or bend the panel.
   (5) Keep the panel away from heat sources.
   (6) Do not dampen the panel with water or other solvents.
   (7) Do not store or use the panel (module) at high temperatures or high humidity,
   as this may affect the characteristics.
   (8) When disposing of this panel, handle it as industrial waste and comply with related regulations.
   (9) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as this may affect the performance.
   (10) This panel is delivered packed in a degassed aluminum laminated bag.
   When storing this panel after unsealing the bag, put it into the aluminum laminated bag again and seal it with tape with the opening folded after inserting desiccants.

## Note

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