SeeYA 0.32inch Micro-OLED（800×600RGB）

Preliminary Specification

Model Name：SY032WEM01

Revision

Version	Date	Description
V0.0	2022.06.27	Initial release

Contents

1. General Description

This display is a 0.32inch diagonal, 800× 600 dots active-matrix color OLED panel module based on single-crystal silicon transistors. This panel integrates panel driver and logic driver, and realizes small size, light weight, low power consumption and high resolution.
Applications: View finders, Head mounted displays, etc.

- 800 x 600 Real RGB Resolution
- AP Operated Resolution

  -- 800 x 600,768 x 576,320 x 240,
- Frame rate: 800 x 600 up to 120hz
- Normal operation supports full color mode: 16.7M colors (24-bit 8(R):8(G):8(B))
- Interface

  -- RGB interface(R:8bit,G:8bit,B:8bit)

  -- MIPI D-PHY with 2 lanes

  --I2C interface
- Vertical/Horizontal scan direction control
- Orbit supported
- Wide range Brightness adjustment
- Normal/Rolling/Dimming mode
- Temperature compensation
- Over temperature protect
- 3 Power input: ELVDD(5~6.5v), ELVSS(-3~-5.5v), VDDI(1.62~1.98v)

2. General Feature

Item	Specification
Resolution	800(H) x 600 (V)
Number of dots	1.44M (800x600x3)
Pixel Size	8.1μm x 8.1μm
Pixel Arrangement	Hexagon, delta arrangement
Active Area	6.48mm x 4.86mm / 0.32" diagonal
Luminance	2000
Contrast Ratio	100,000:1
Uniformity	> 85%
Power Consumption	220mW
Gray Levels	256
Interface	I2C+RGB and MIPI
Frame Rate	15~120HZ
Weight	TBD
Operating Temperature	-20°C to +70°C
Storage Temperature	-40°C to +80°C

3. Optical Specification

Tpanel=30℃	Parameter	Min.	Typ.	Max.	Unit
Brightness			2000		cd/m2
CR	white to Black Contrast Ratio		100,000:1		
Uniformity	End to end large-area uniformity	85			%
CIE Red	CIE-x		0.64		
	CIE-y		0.33		
CIE Green	CIE-x		0.24		
	CIE-y		0.68		
CIE Blue	CIE-x		0.15		
	CIE-y		0.06		
CIE White	CIE-x		0.313		
	CIE-y		0.329		
DCI-P3			90		
Frame rate		15		120	HZ
Power consumption(3000nits, D-PHY 2lanes,60Hz)			220		mW

Note1: If there is no specified, the specification of optical is specified at 30 degrees Celsius.

Note2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. Brightness is measured as peak luminance at full white pattern (Gray level=255 with 8bits color depth);

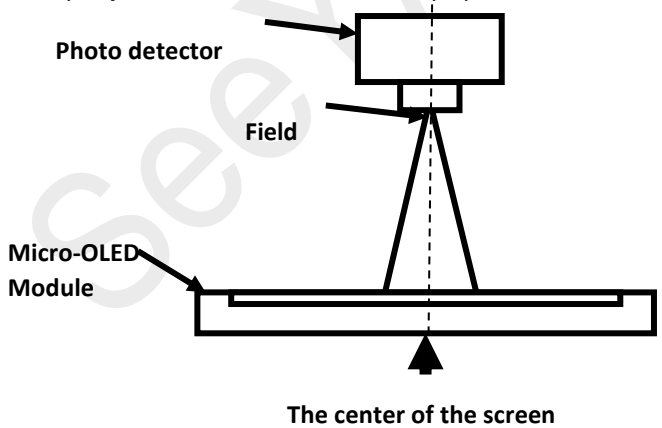


Fig.1

Note3: Definition of Uniformity at gray level255(8bits color depth) and 100%duty emission.

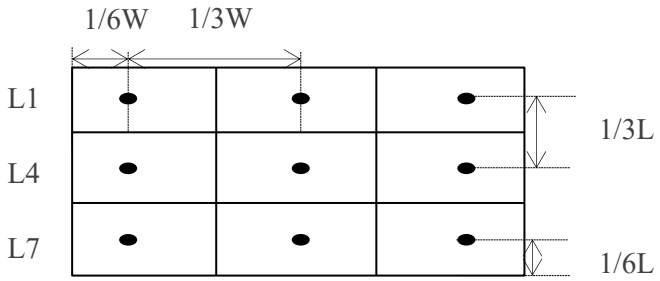
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

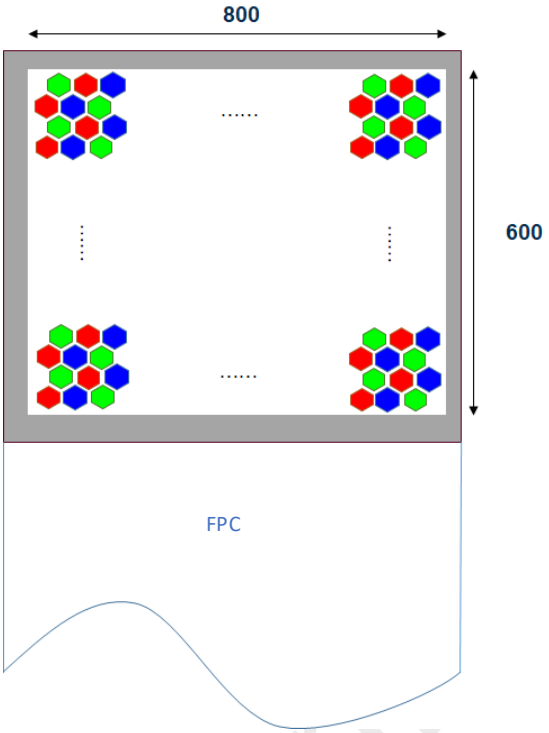
L-------Active area length; W----- Active area width

Lmax: The measured maximum luminance of all measurement position.

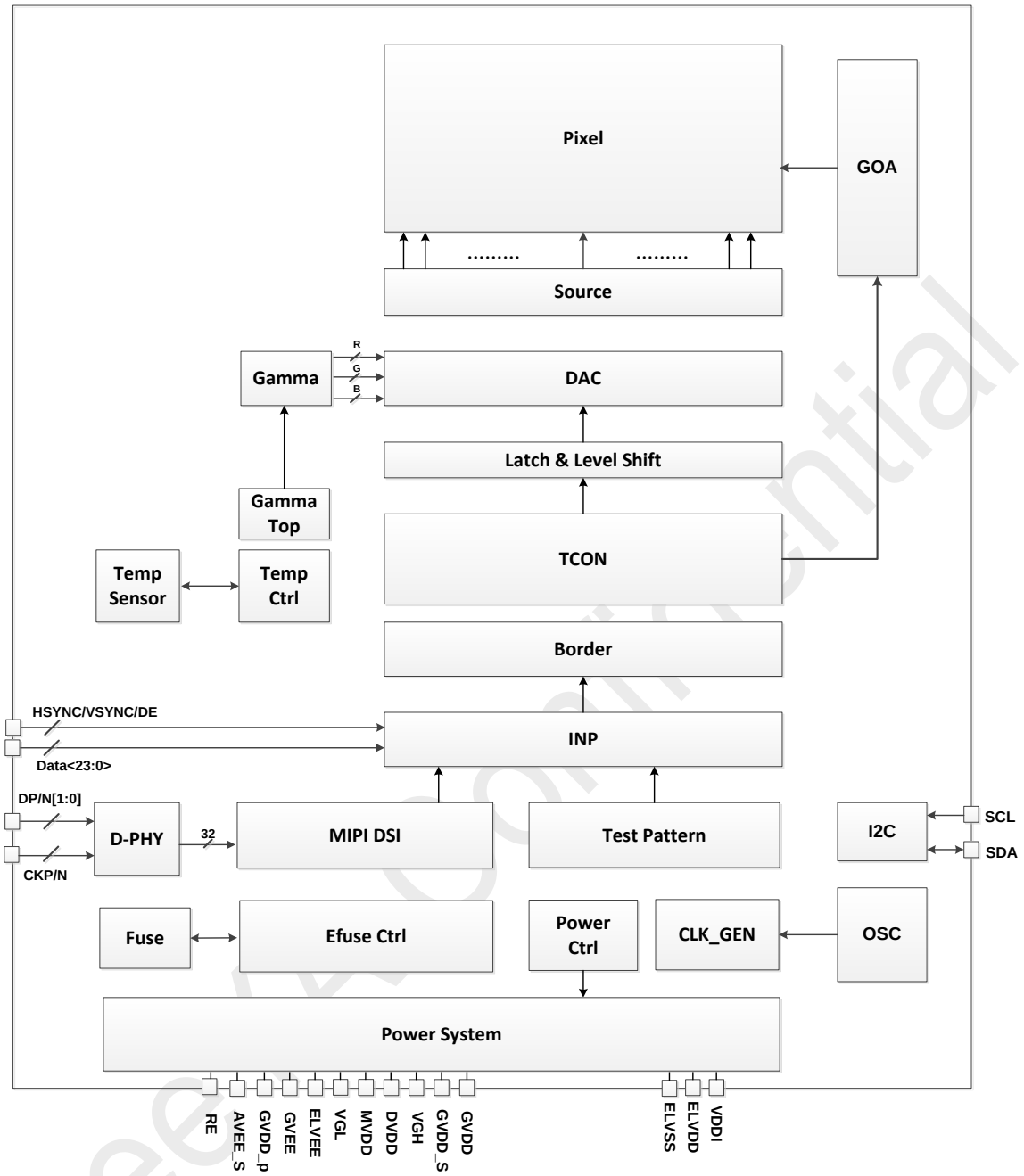
Lmin: The measured minimum luminance of all measurement position.



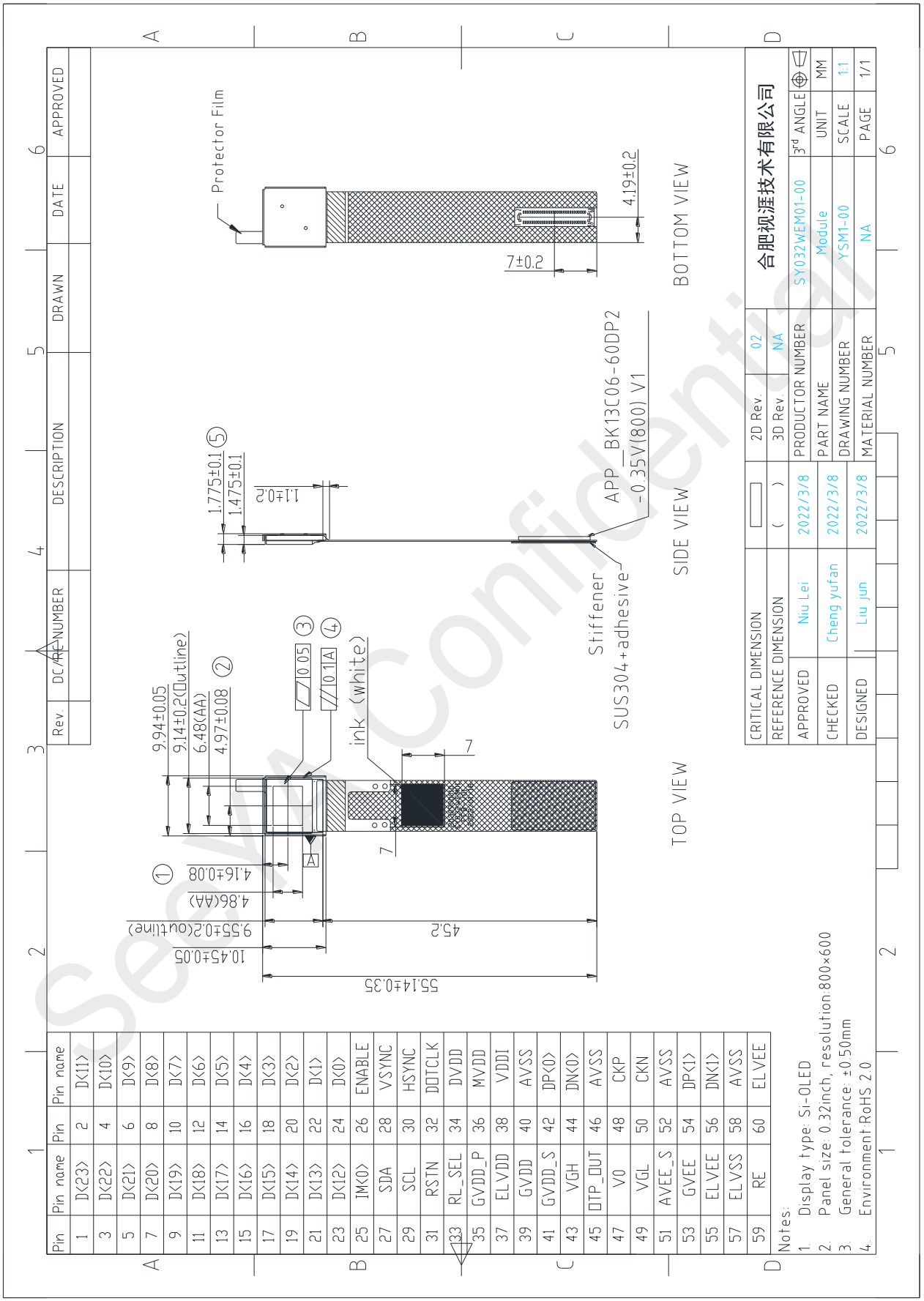
4. Pixel Array



5. System Block



6. Module Diagram



Pin	Pin name	Pin	Pin name
1	D<23>	2	D<11>
3	D<22>	4	D<10>
5	D<21>	6	D<9>
7	D<20>	8	D<8>
9	D<19>	10	D<7>
11	D<18>	12	D<6>
13	D<17>	14	D<5>
15	D<16>	16	D<4>
17	D<15>	18	D<3>
19	D<14>	20	D<2>
21	D<13>	22	D<1>
23	D<12>	24	D<0>
25	IM<0>	26	ENABLE
27	SDA	28	VSYNC
29	SCL	30	HSYNC
31	RSTN	32	DDTCLK
33	RL_SEL	34	DVDD
35	GVDD_P	36	MVDD
37	ELVDD	38	VDDI
39	GVDD	40	AVSS
41	GVDD_S	42	DP<0>
43	VGH	44	DN<0>
45	OTP_OUT	46	AVSS
47	V0	48	CKP
49	VGL	50	CKN
51	AVEE_S	52	AVSS
53	GVEE	54	DP<1>
55	ELVEE	56	DN<1>
57	ELVSS	58	AVSS
59	RE	60	ELVEE

7. Pin Description

Pin Description

Pin No.	Symbol	Type	Description
1	D<23>	Input	RGB data pin,default R7;
2	D<11>	Input	RGB data pin,default G3;
3	D<22>	Input	RGB data pin,default R6;
4	D<10>	Input	RGB data pin,default G2;
5	D<21>	Input	RGB data pin,default R5;
6	D<9>	Input	RGB data pin,default G1;
7	D<20>	Input	RGB data pin,default R4;
8	D<8>	Input	RGB data pin,default G0;
9	D<19>	Input	RGB data pin,default R3;
10	D<7>	Input	RGB data pin,default B7;
11	D<18>	Input	RGB data pin,default R2;
12	D<6>	Input	RGB data pin,default B6;
13	D<17>	Input	RGB data pin,default R1;
14	D<5>	Input	RGB data pin,default B5;
15	D<16>	Input	RGB data pin,default R0;
16	D<4>	Input	RGB data pin,default B4;
17	D<15>	Input	RGB data pin,default G7;
18	D<3>	Input	RGB data pin,default B3;
19	D<14>	Input	RGB data pin,default G6;
20	D<2>	Input	RGB data pin,default B2;
21	D<13>	Input	RGB data pin,default G5;
22	D<1>	Input	RGB data pin,default B1;
23	D<12>	Input	RGB data pin,default G4;
24	D<0>	Input	RGB data pin,default B0;
25	IM<0>	Input	Use to select the interface type IM<0> / Command / Display Data 0V / I2C / MIPI or RGB 1.8V / MIPI / MIPI
26	ENABLE	Input	Data enable input;
27	SDA	Input/Output	IM<0>=0, Data input/output for I2C; IM<0>=1, use as LSW<0>;
28	VSYNC	Input	Vertical sync input;
29	SCL	Input	IM<0>=0, Serial clock for I2C; IM<0>=1, use as LSW<1>;
30	HSYNC	Input	Horizontal sync input;
31	RSTN	Power	This signal will reset the device and must be applied to properly Initialize the chip. Signal is active low.
32	DOTCLK	Input	Pixel clock input;
33	RL_SEL	Input	Use to select I2C slave address. (digital test pad in/out pad)
34	DVDD	Output	Regulator output for logic digital system positive power. Connect a capacitor for stabilization.
35	GVDD_P	Output	Regulator output for GAMMA analog system positive power. Connect a capacitor(2.2uF) for stabilization.
36	MVDD	Output	Regulator output for MIPI analog system positive power. Connect a capacitor(2.2uF) for stabilization.
37	ELVDD	Power	Power supply for OLED cell. Connect a capacitor(4.7uF) for stabilization.
38	VDDI	Power	Power supply for D-PHY, DSI and digital part. Connect a capacitor(4.7uF) for stabilization.
39	GVDD	Output	Regulator output for GAMMA analog system positive power. Connect a capacitor(1uF) for stabilization.
40	AVSS	Power	System GND for internal digital/analog system.

41	GVDD_S	Output	Regulator output for source analog system positive power. Connect a capacitor(2.2uF) for stabilization.
42	DP<0>	Input/Output	This pin is DSI-D0+ differential clock signal if MIPI Port interface is used. DP0/N0 is differential small amplitude signals. If not used, keep it open.
43	VGH	Output	Regulator for GOA. Connect a capacitor(1uF) for stabilization.
44	DN<0>	Input/Output	This pin is DSI-D0- differential clock signal if MIPI Port interface is used. DP0/N0 is differential small amplitude signals. If not used, keep it open.
45	OTP_OUT	Output	Test pin for debug signal.
46	AVSS	Power	System GND for internal digital/analog system.
47	V0	Power	Regulator for source. Connect a capacitor(1uF) for stabilization.
48	CKP	Input	This pin is DSI-CLK+ differential clock signal if MIPI Port interface is used. DP1/N1 is differential small amplitude signals. If not used, keep it open.
49	VGL	Output	Regulator for GOA. Connect a capacitor(1uF) for stabilization. Connect a Schottky diode to GND.
50	CKN	Input	This pin is DSI CLK- differential clock signal if MIPI Port interface is used. CLKP/N is differential small amplitude signals. If not used, keep it open.
51	AVEE_S	Output	Regulator for source. Connect a capacitor(2.2uF) for stabilization. Connect a Schottky diode to GND.
52	AVSS	Power	System GND for internal digital/analog system.
53	GVEE	Output	Regulator for gamma. Connect a capacitor(1uF)for stabilization. Connect a Schottky diode to GND.
54	DP<1>	Input/Output	This pin is DSI-D1+ differential clock signal if MIPI Port interface is used. DP1/N1 is differential small amplitude signals. If not used, keep it open.
55	ELVEE	Power	Power supply for OLED cell. Connect all ELVEE together.
56	DN<1>	Input/Output	This pin is DSI D1- differential clock signal if MIPI Port interface is used. DP1/N1 is differential small amplitude signals. If not used, keep it open.
57	ELVSS	Power	Power supply for OLED cell. Connect a capacitor(4.7uF) for stabilization.Connect a Schottky diode to GND.
58	AVSS	Power	System GND for internal digital/analog system.
59	RE	Output	OLED Reset Power supply. Connect a capacitor(2.2uF) for stabilization.
60	ELVEE	Power	Power supply for OLED cell. Connect a capacitor(2.2uF) for stabilization. Connect a Schottky diode to GND. Connect all ELVEE together.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When this Micro-OLED product is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use this Micro-OLED product within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, this Micro-OLED product will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage (1)	VDDI	-0.3~2.2	V
Power Supply Voltage (2)	ELVDD	-0.3~7	V
	ELVSS	-5.5~0.3	V
MIPI Differential Input	CLKP, CLKN, DATAP0, DATAN0, DATAP1, DATAN1,	1.32	V
Input Voltage of Interface	Vin	-0.3 ~ VDDI+0.3	V
Output Voltage of Interface	Vo	-0.3 ~ VDDI+0.3	V
Operating temperature	Topr	-20~70	°C
Storage temperature	Tstg	-40~80	°C

8.2 DC Characteristic

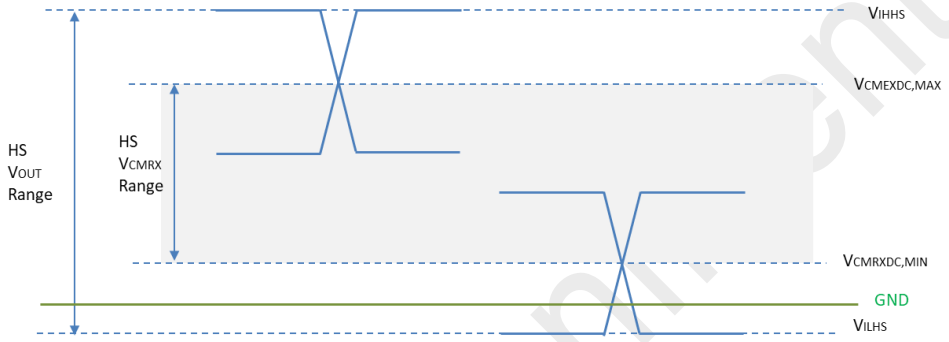
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage						
Digital I/O Input Level @Logic HighR7	VIH	VDDI=1.62V ~ 1.98V	0.7*VDDI	-	VDDI	V
Digital I/O Input Level @Logic Low	VIL	VDDI=1.62V ~ 1.98V	0	-	0.3*VDDI	V
Digital I/O Output Level @Logic High	VOH	Iout = -1mA	0.8*VDDI	-	VDDI	V
Digital I/O Output Level @Logic Low	VOL	Iout = +1mA	0	-	0.2*VDDI	V
Digital I/O Input leakage @Logic High	IIHD	Vin = VDDI			1	uA
Digital I/O Input leakage @Logic Low	IILD	Vin = 0	-1			uA
MIPI I/O Power Supply	MVDD	-	-	1.2	-	V
MIPI Input leakage @Logic High	IIHMD	Vin = MVDD			1	uA
MIPI Input leakage @Logic Low	IILMD	Vin = 0	-1			uA

8.3 DSI DC/AC Characteristic

8.1.1 Receiver characteristic

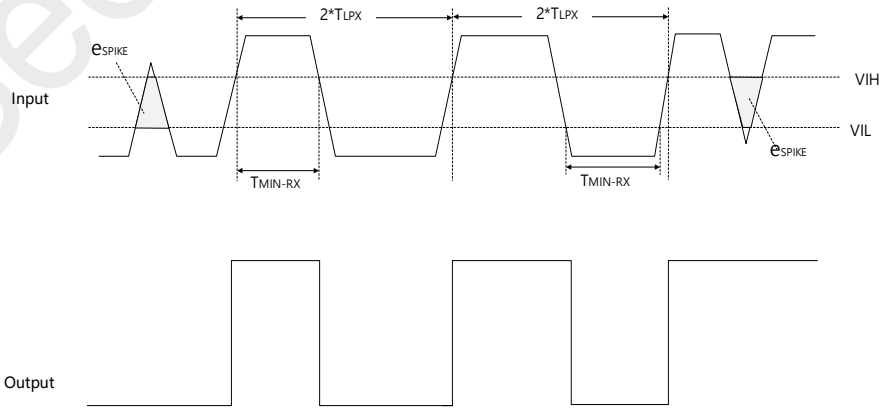
High speed receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	-	330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IDTH}	Differential input high threshold	-	-	70	mV
V_{IDTL}	Differential input low threshold	-70	-	-	mV
V_{IHHS}	Single-ended input high voltage	-	-	460	mV
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV
C_{CM}	Common-mode termination	-	-	60	pF



Low power receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
V_{IH}	Logic 1 input voltage	980	-	-	mV
V_{IL}	Logic 0 input voltage, not in ULP state	-	-	550	mV
V_{IL_ULPS}	Logic 0 input voltage, ULP state	-	-	300	mV
V_{HYST}	Input hysteresis	25	-	-	mV
e_{SPIKE}	Input pulse rejection	-	-	300	V·ps
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns



8.1.2 Transmitter Characteristics

High-Speed Transmitter Characteristics

Parameter	Description	Min	Typ.	Max	Unit
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	-	-	360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
t_R and t_F (note1,2)	20%-80%rise time and fall time	-	-	0.3	UI
		-	-	0.35	UI

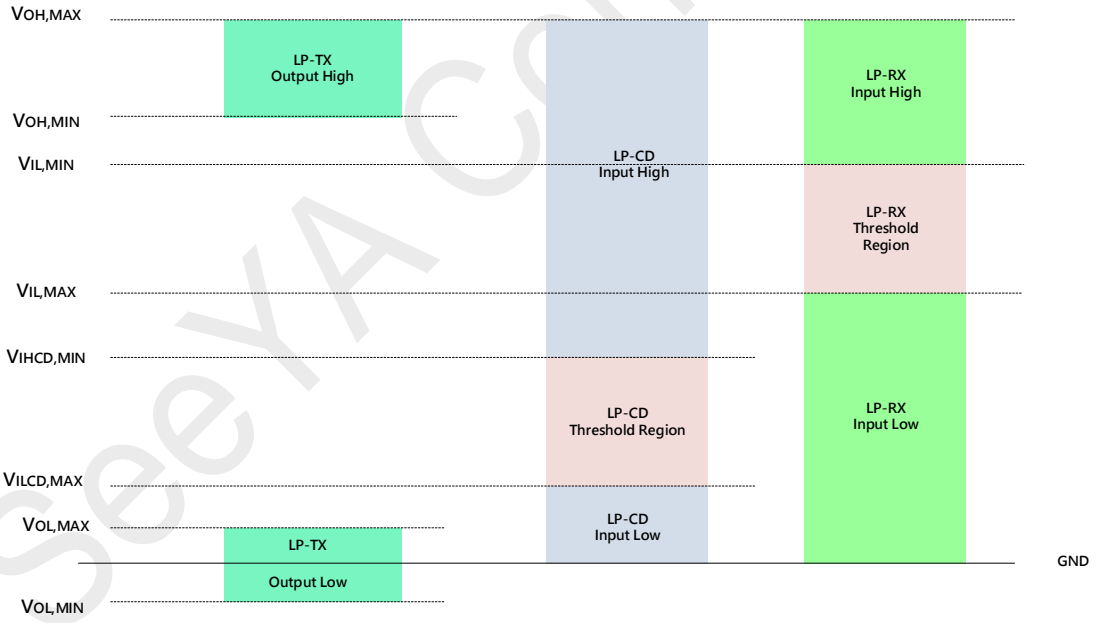
Note:

Applicable when supporting maximum HS bitrates ≤ 1Gbps (UI≥1ns)

Applicable when supporting maximum HS bitrates > 1Gbps(UI<1ns) but ≤ 1.5Gbps(UI≥0.667ns)

Low-Power Transmitter Characteristics

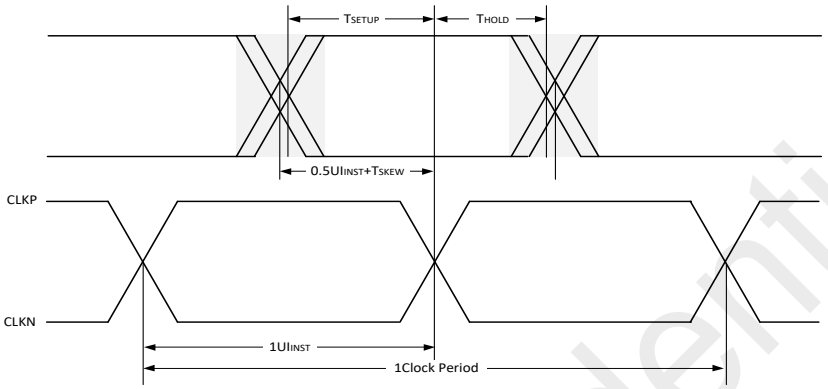
Parameter	Description	Min	Typ.	Max	Unit
V_{OH}	The output high level	1.1	1.2	1.3	V
V_{OL}	The output low level	-50	-	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω
V_{IHCD}	Logic1 contention threshold	450	-	-	mV
V_{ILCD}	Logic0 contention threshold	-	-	200	mV



8.4 Timing Characteristics

8.4.1 High Speed Mode Characteristics

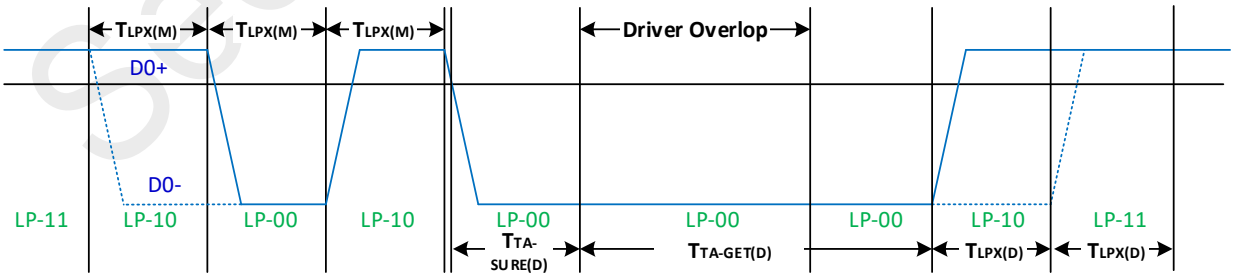
Parameter	Symbol	Min	Typ.	Max	Unit
UI instantaneous	U_{IINST}	1	-	3	ns
T Data to Clock Skew	T_{SKEW}	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	T_{SETUP}	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	T_{HOLD}	0.15	-	-	UIHS



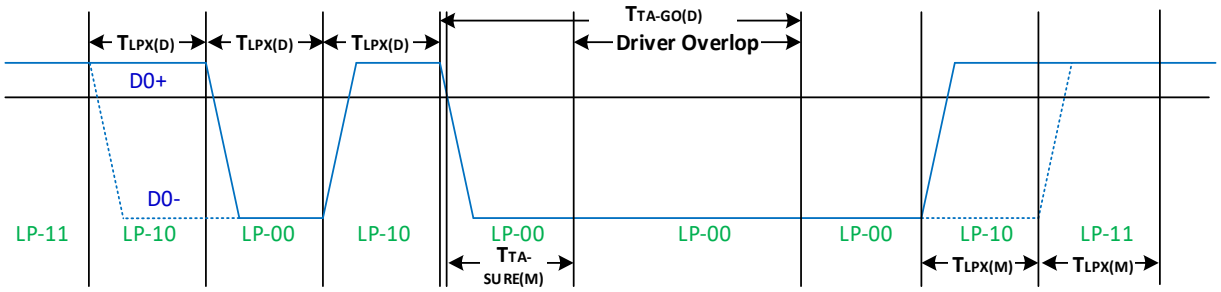
8.4.2 Low Power Mode Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	TLPX	-	2*TLPX	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround	5* TLPX			
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround	4* TLPX			

- Bus Turnaround from MPU to display module

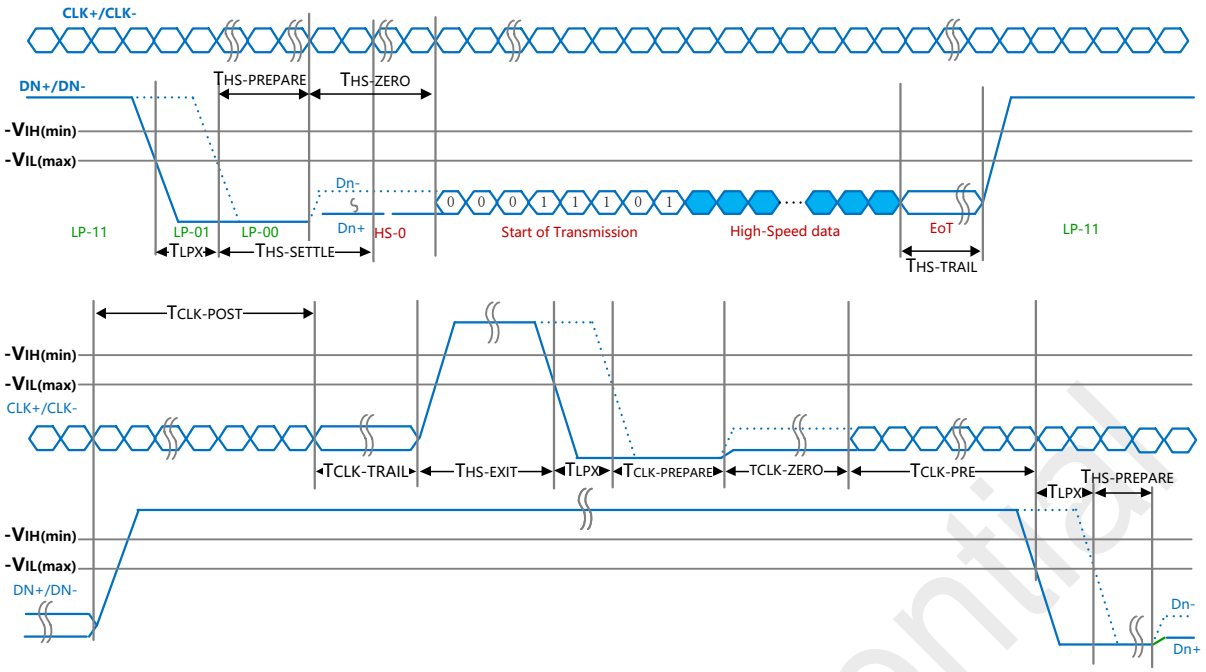


- Bus Turnaround from MPU to display module

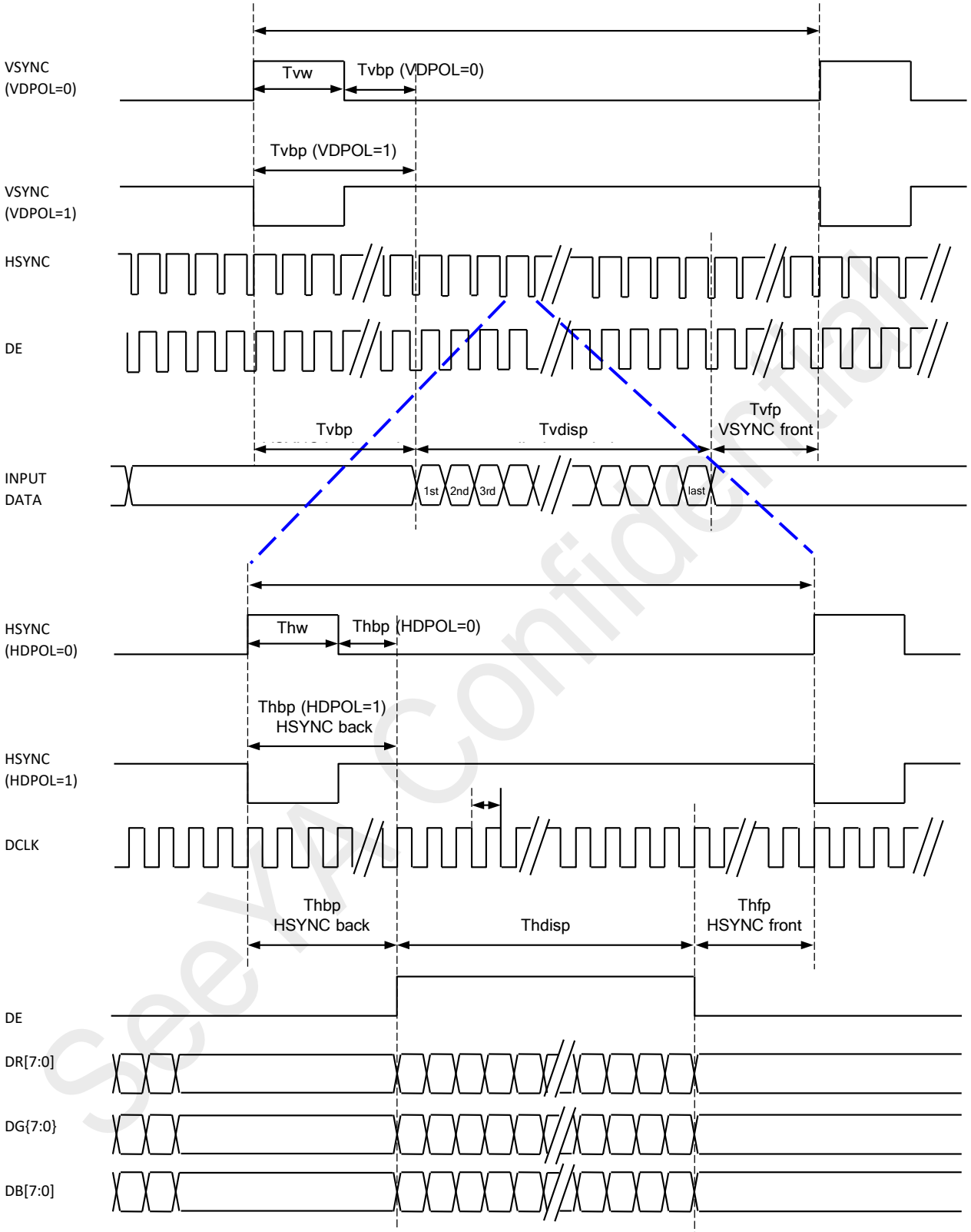


8.4.3 High Speed Mode Operation Timing Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL	60ns+52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE	95	-	300	ns
$T_{CLK-TERM\_EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst t	60	-	-	ns
$T_{CLK-PREPARE}$+$T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst	100	-	-	ns
T_{D-TERM_EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX	-	-	35ns+ 4*UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns+4*UI	-	85ns+ 6*UI	ns
$T_{HS-PREPARE}$+$T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	145ns+10*UI	-	-	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns+6*UI	-	145ns +10*UI	ns

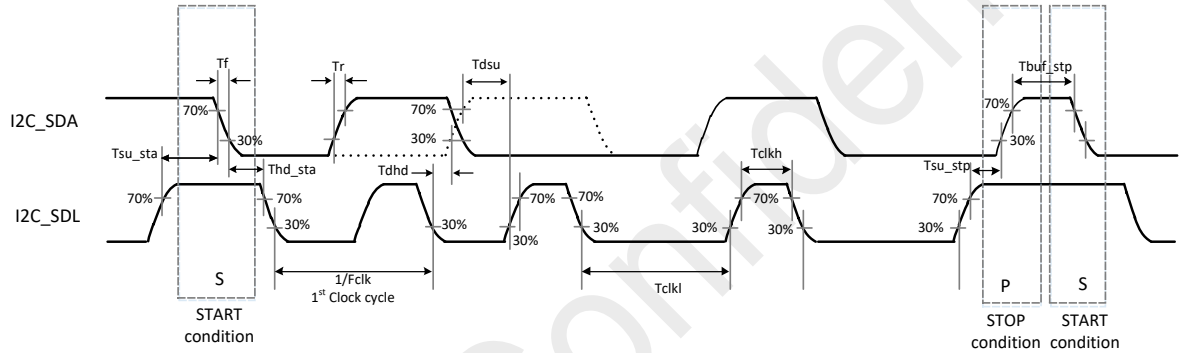


8.4.4 RGB Interface Timing



8.4.5 I2C-Bus Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
I2C Clock Frequency	F_{clk}	-	-	400	kHz	
I2C Clock Low	T_{clkl}	1300	-	-	ns	
I2C Clock High	T_{clkh}	600	-	-	ns	
I2C Data Rising Time	T_{dr}	-	-	300	ns	
I2C Data Falling Time	T_{df}	-	-	300	ns	
I2C Data Setup Time	T_{dsu}	100	-	-	ns	
I2C Data Hold Time	T_{dhd}	-	-	TBD	ns	
I2C Setup Time (Start Condition)	T_{su_sta}	600	-	-	ns	
I2C Hold Time (Start Condition)	T_{hd_sta}	600	-	-	ns	
I2C Setup Time (Stop Condition)	T_{su_stp}	600	-	-	ns	
I2C Bus Free Time (Stop Condition)	T_{buf_stp}	1300	-	-	ns	



8.5 Input Video Timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical cycle	VP	-	-	628	-	Line
Vertical low pulse width	VS	-	-	4	-	Line
Vertical front porch	VFP	-	-	1	-	Line
Vertical back porch	VBP	-	-	23	-	Line
Vertical active area	VDISP	-	-	600	-	Line
Vertical refresh rate	VRR	-	-	60	-	Hz

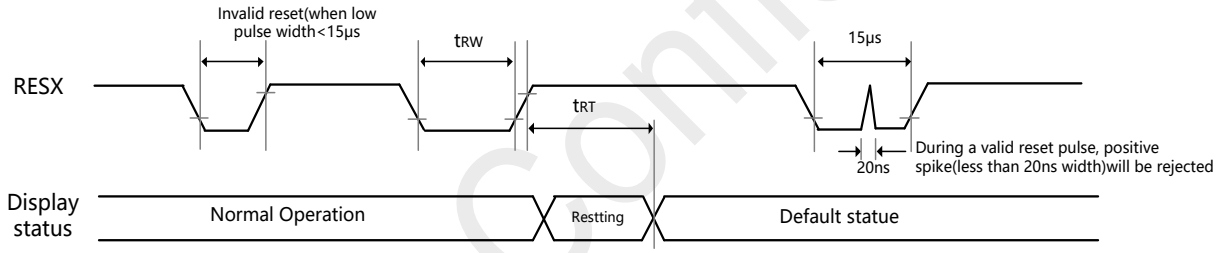
Vertical video timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
HS cycle	HP	-	-	1056	-	DCK
HS low pulse width	HS	-	-	128	-	DCK
Horizontal front porch	HFP	-	-	40	-	DCK
Horizontal back porch	HBP	-	-	88	-	DCK
Horizontal active area	HDISP	-	-	800	-	DCK

Horizontal video timing

8.6 Reset Timing Characteristics

When Reset happens in Sleep-out mode, this Micro-OLED product will enter blanking sequence with the maximum time 120 msec. Then this Micro-OLED product will remain in blanking state and return \ default state. During reset complete time (tRT), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.

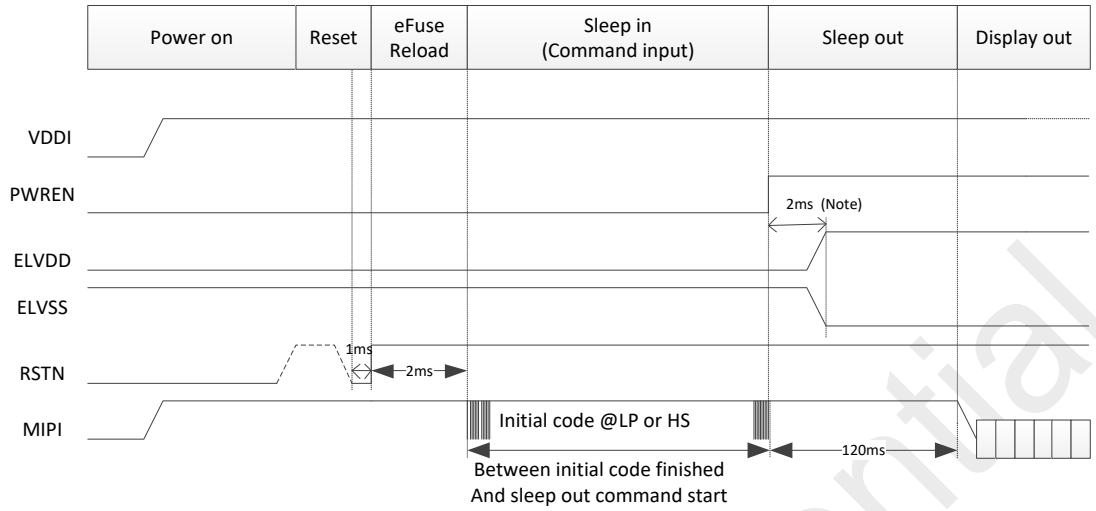


Reset time @VDDI=1.62V to 1.98V, Ta=-40°C to 85°C

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RESX	t_{RW}	Reset low pulse width	15			us	
	t_{RT}	Reset Complete time			2	ms	When reset applied at sleep-in mode
					120	ms	When reset applied at sleep-out mode

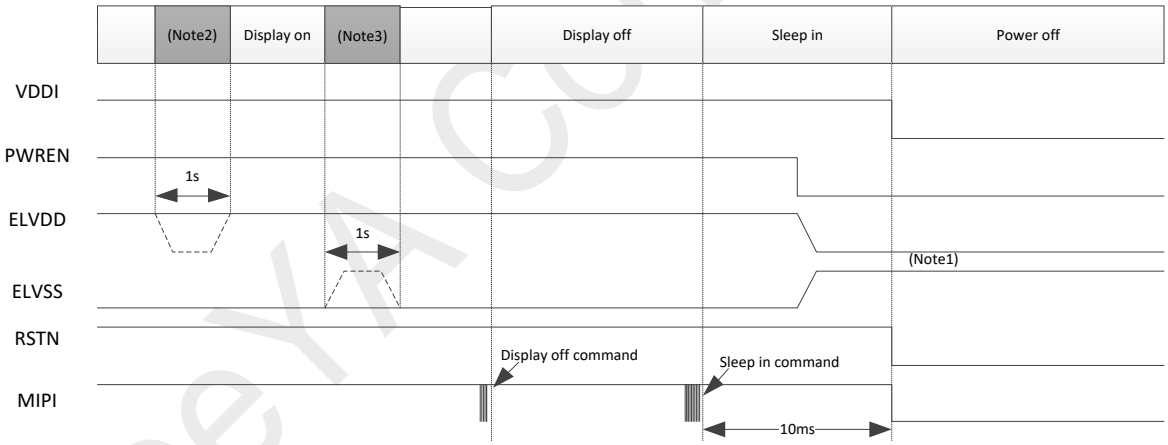
9. Power Sequence

Power on sequence



Note: ELVDD/ELVSS power on timing is depend on power IC, we suggest customer to select power IC that power on timing is ≤ 2ms.

Power off sequence



Note:

1.ELVDD/ELVSS power off timing is depend on power IC.

2.When IC is in display on status, ELVDD abnormal drop occurs. If ELVDD can recover less than 1 second, then IC will return to normal display.

3.When IC is in display on status, ELVSS abnormal drop occurs. If ELVSS can recover less than 1 second, then IC will return to normal display.

10. Interface

This Micro-OLED product supports MIPI interface,RGB interface and inter-integrated circuit interface (I2C).

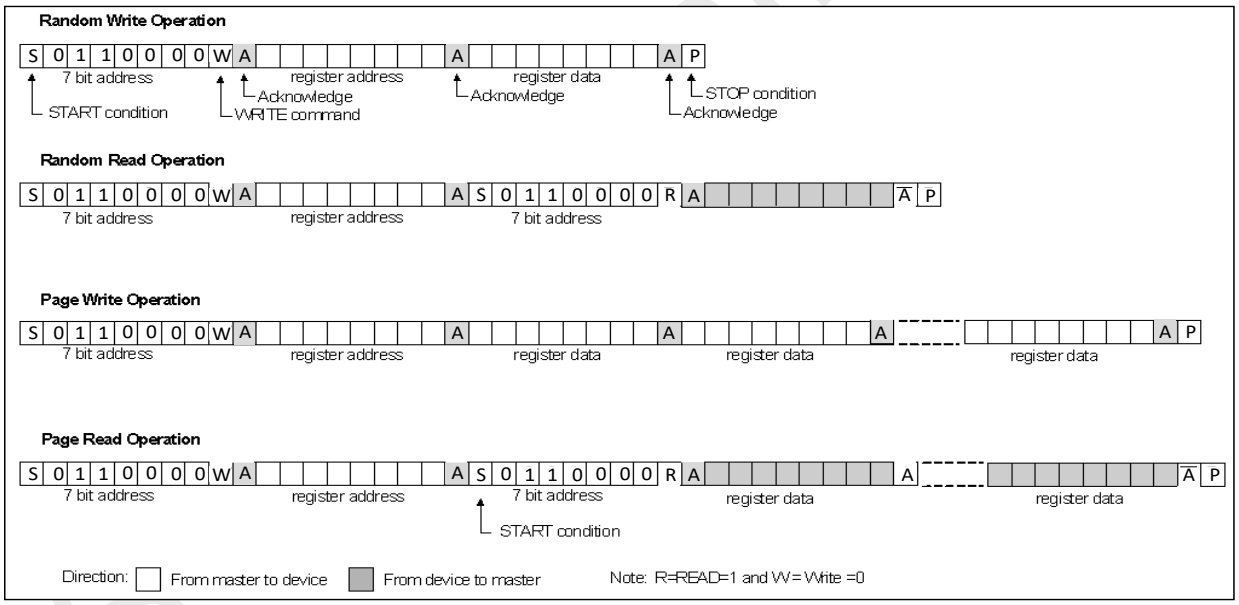
IM<0>	Command Execute	Image Write
0V	I2C	MIPI or RGB
1.8V	MIPI	MIPI

10.1 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte maybe sent. The master generates all clock pulses, including the ninth acknowledge clock pulse.

I2C-Bus Protocol

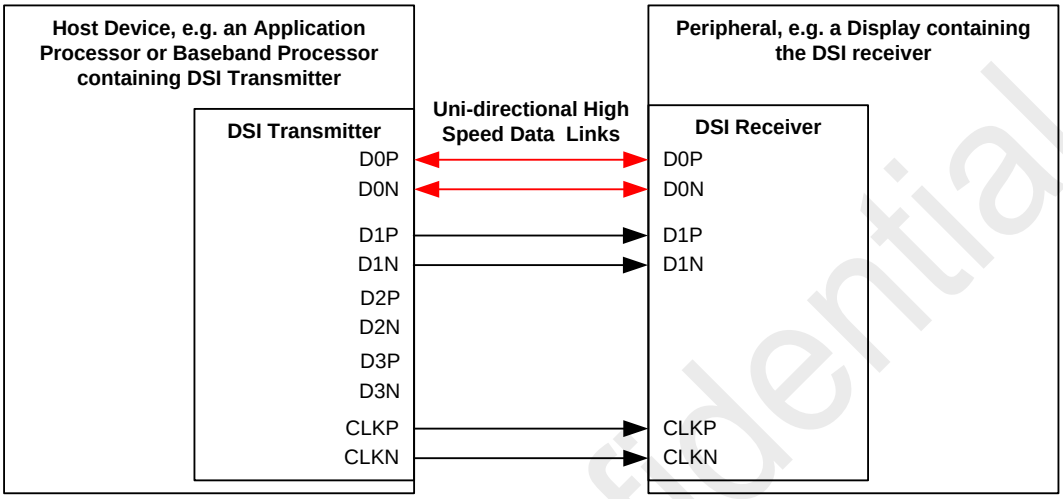
Before any data is transmitted on the I2C-bus, the device, which should respond is addressed first. The address of SY032 is 0x60 or 0x62. The slave addressing is always carried out with the first byte transmitted after the START procedure.



10.2 MIPI Interface

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.



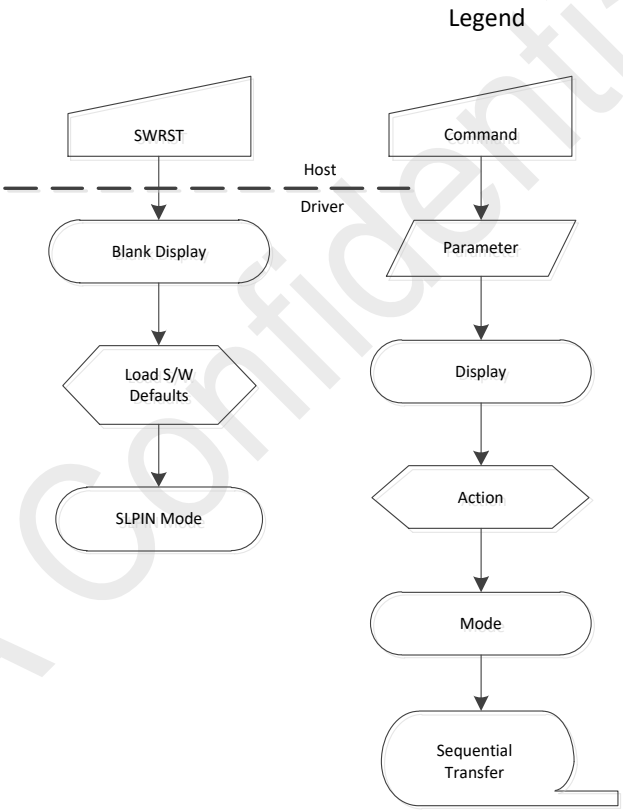
DSI transmitter and receiver interface

11. User Command

Command list

Operation	Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
SWRESET	01	01	W	No Parameter								01
RDDPM	0A	01	R		Idle Mode On/Off		Sleep In/Out	1	Display On/Off			08
RDDMADCTL	0B	01	R					RGB/BGR		Flip Horizontal	Flip Vertical	03
RDDIM	0D	01	R			Inversion On/Off						00
SLPIN	10	01	W	No Parameter								NA
SLPOUT	11	01	W	No Parameter								NA
INVOFF	20	01	W	No Parameter								NA
INVON	21	01	W	No Parameter								NA
DISPOFF	28	01	W	No Parameter								NA
DISPON	29	01	W	No Parameter								NA
TEOFF	34	01	W	No Parameter								NA
TEON	35	01	W								Mode	NA
MADCTL	36	01	W					RGB/BGR		Flip Horizontal	Flip Vertical	NA
IDMOFF	38	01	W	No Parameter								NA
IDMON	39	01	W	No Parameter								NA
STESL	44	01	W	TE_SCAN_LINE[15:8]								NA
		02	W	TE_SCAN_LINE[7:0]								NA
RDDDBS	A1	01	R	DDB1[7:0]								00
		02	R	DDB2[7:0]								72
		03	R	DDB3[7:0]								02
		04	R	DDB4[7:0]								FF
		05	R	DDB5[7:0]								FF
PAGESEL	FF	01	R/W	PAGE_SEL[7:0]								FF

SWRESET: Software Reset (01h)

01H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	0	0	0	0	0	1	01
Parameter	W	No Parameter								
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default value in each command description).									
Restriction	The host processor must wait 10 milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time. SWRESET should not be sent when the display module is not in SLPIN mode.									
Default	WRITE ONLY, N/A									
Flow Chart										

RDDPM: Read Display Power Mode (0Ah)

0AH	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	**R**	0	0	0	0	1	0	0	1	0A
Parameter	**R**	-	D6	D5	D4	D3	D2	-	-	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Not Defined	Set to '0'
D6	Idle Mode On/Off	-
D5	Partial Mode On/Off	Set to '0'
D4	Sleep In/Out	-
D3	Display Normal Mode On/Off	Set to '1'
D2	Display On/Off	-
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D7 '0'
Bit D6 – Idle Mode On/Off ,'0' = Idle Mode Off. '1' = Idle Mode On.
Bit D5 '0'
Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode.
Bit D3 '1'
Bit D2 – Display On/Off '0' = Display is Off. '1' = Display is On.
Bit D1 '0'
Bit D0 '0'

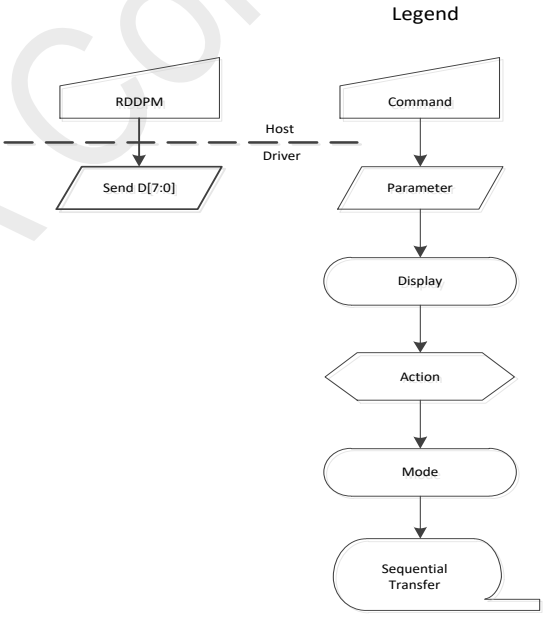
Restriction

N/A

Default

SW Reset/HW Reset : 0Ah= 0x08

Flow Chart



RDDMADCTL: Read Display MADCTL (0Bh)

0BH	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	R	0	0	0	0	1	0	1	1	0B
Parameter	R	-	-	-	-	D3	-	D1	D0	03

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D3	RGB/BGR Order	1=BGR, 0=RGB
D1	Flip Horizontal	1=Normal display 0=Flip Horizontal
D0	Flip Vertical	0=Normal display 1=Flip Vertical

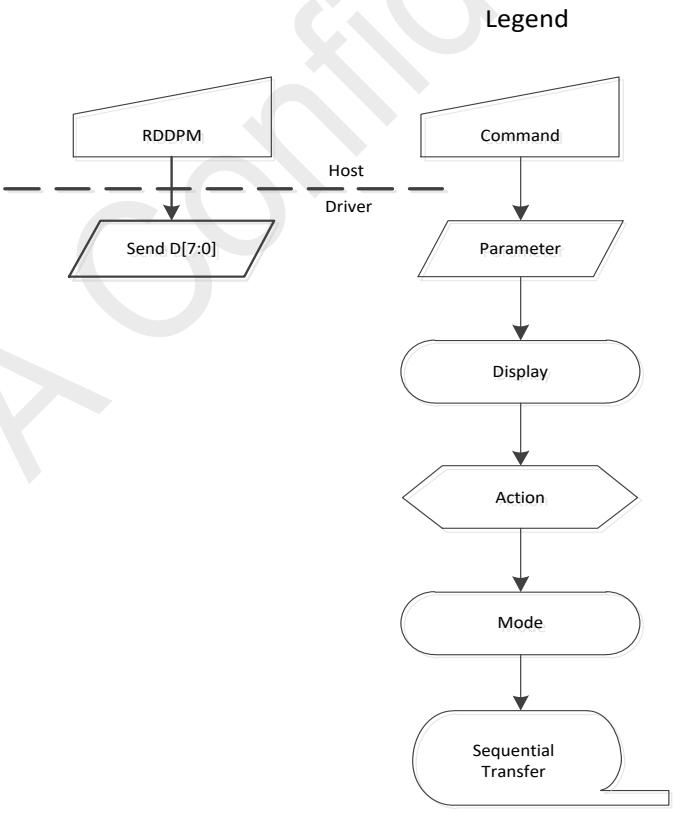
Restriction

N/A

Default

SW Reset/HW Reset : 0Bh= 0x03

Flow Chart



RDDIM: Read Display Image Mode (0Dh)

0DH	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	R	0	0	0	0	1	1	0	1	0D
Parameter	R	-	-	D5	-	-	-	-	-	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D5	Inversion On/Off	1=Inversion is On 0=Inversion is Off

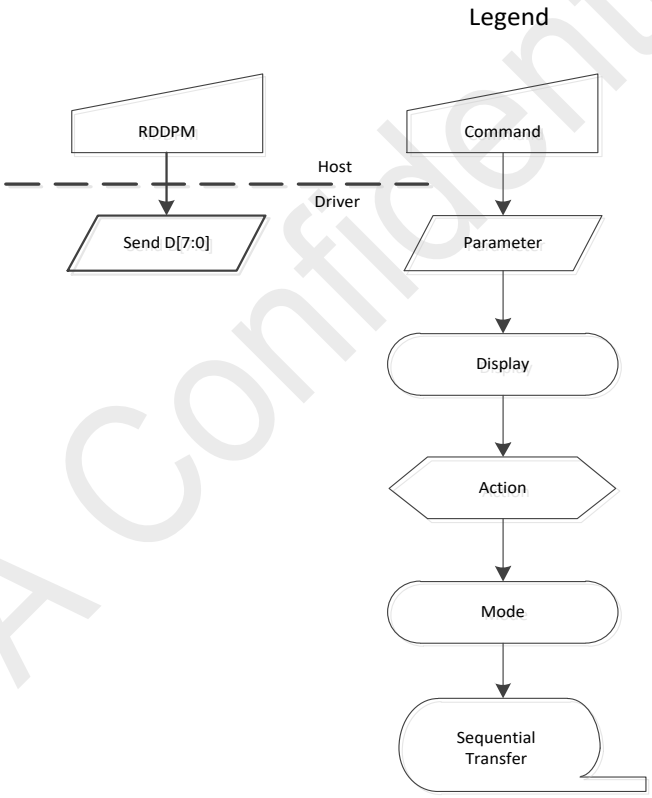
Restriction

N/A

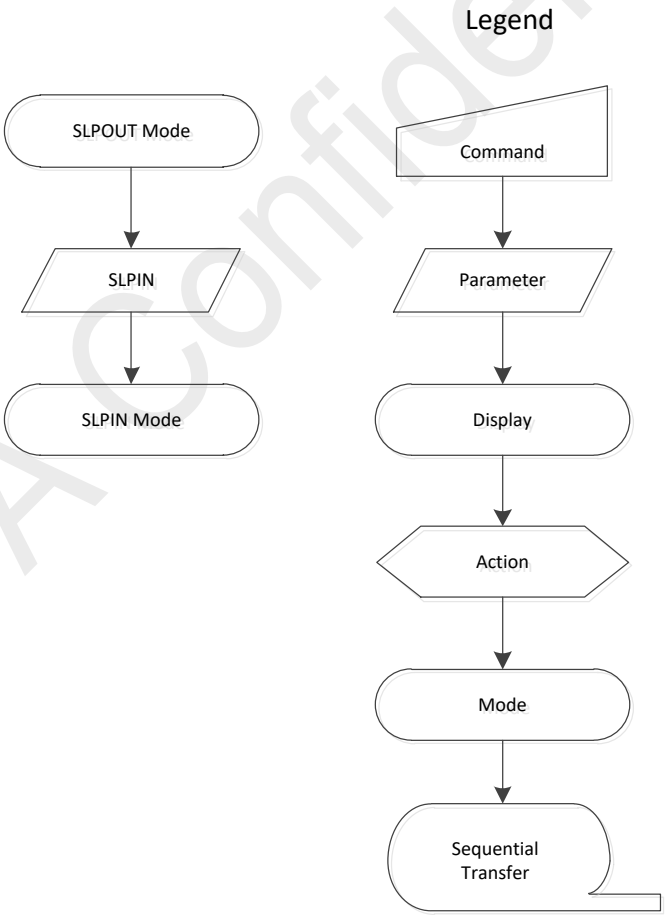
Default

SW Reset/HW Reset : 0Dh= 0x00

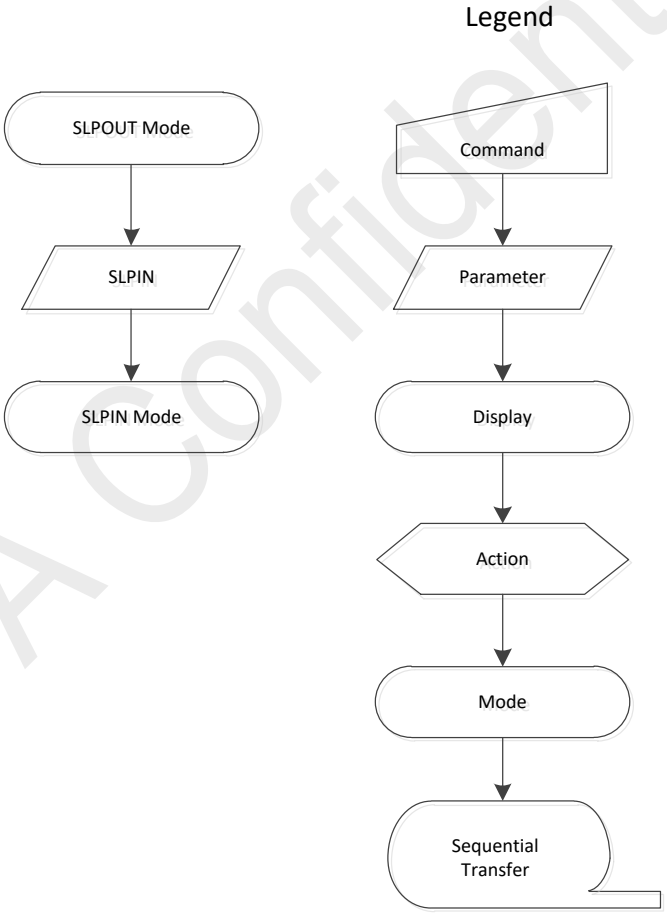
Flow Chart



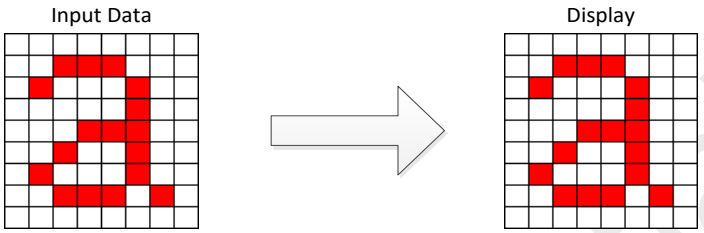
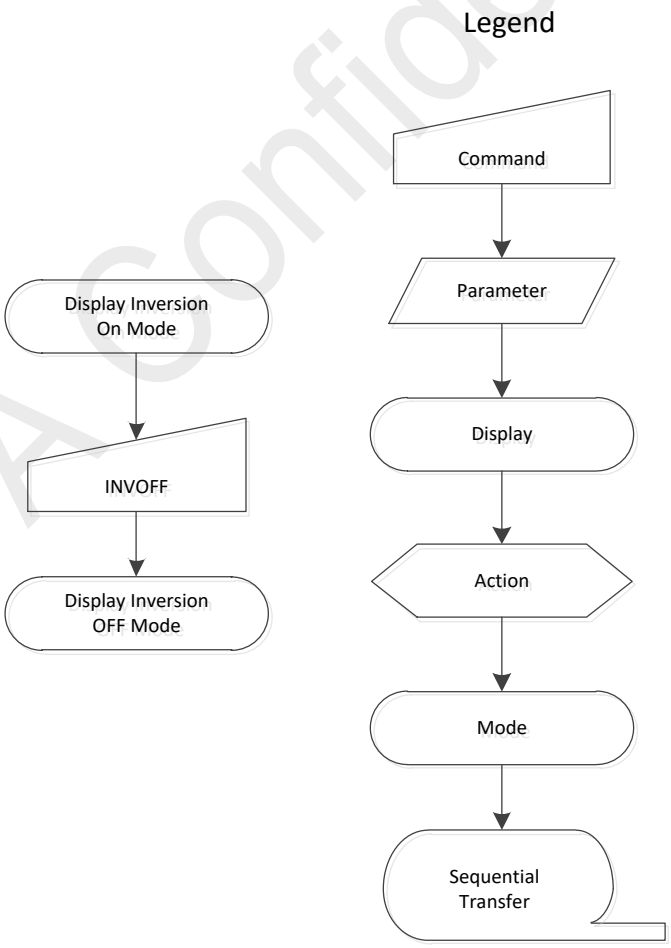
SLPIN: Enter Sleep In Mode (10h)

10H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	0	1	0	0	0	0	10
Parameter	W	No Parameter								
Description	This command causes the display module to enter the minimum power consumption mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports. In this mode the DC/DC converter is stopped, and panel scanning is stopped.									
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 80msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.									
Default	WRITE ONLY, N/A									
Flow Chart	It takes 10msec to get into Sleep In mode after SLPIN command issued. 									

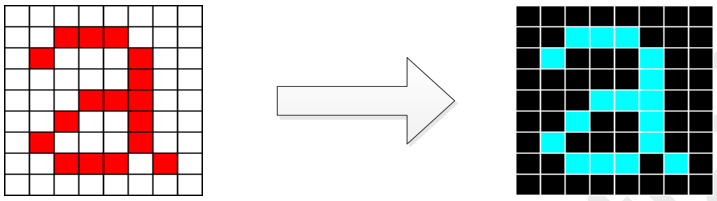
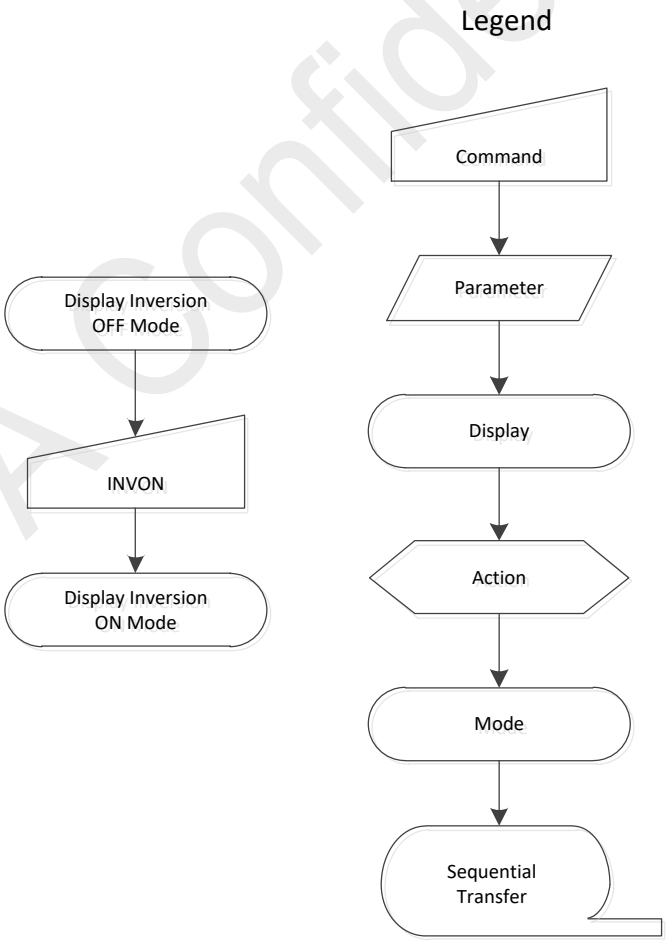
SLPOUT: Exit Sleep in Mode (11h)

11H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	0	1	0	0	0	1	11
Parameter	W	No Parameter								
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, and panel scanning is started.									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 10msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.									
Default	WRITE ONLY, N/A									
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued. 									

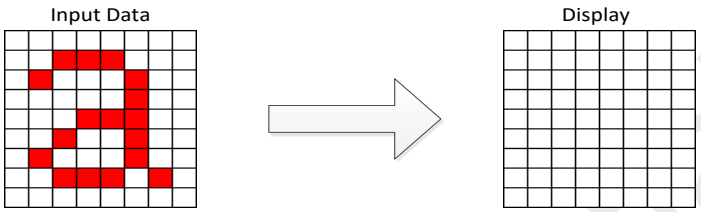
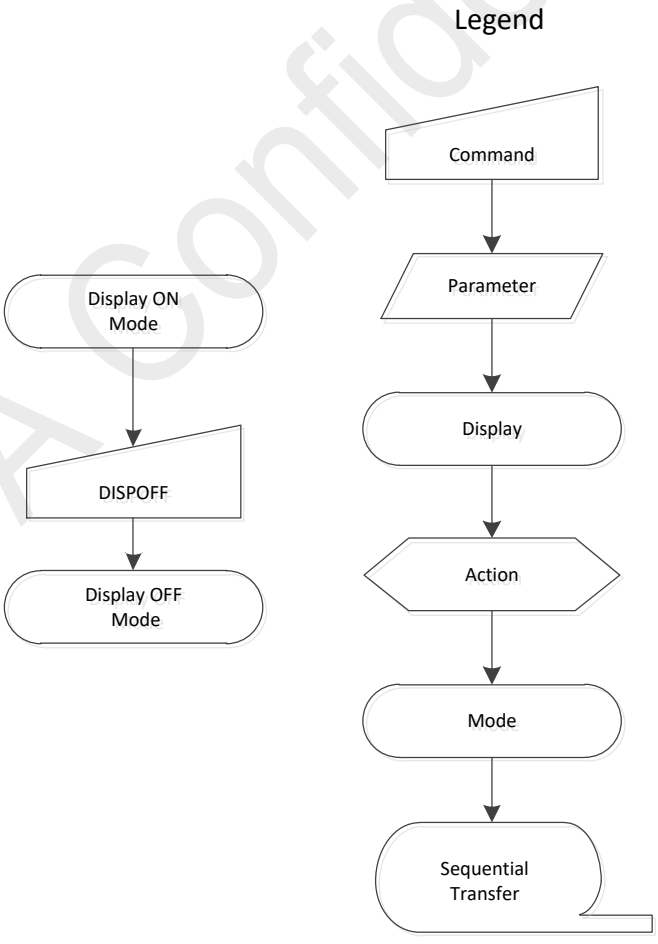
INVOFF: Display Inversion Off (20h)

20H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	0	0	0	0	0	20
Parameter	W	No Parameter								
Description	Displayed image colors are not inverted. (Example) 									
Restriction	This command has no effect when module is already in inversion off mode.									
Default	WRITE ONLY, N/A									
Flow Chart										

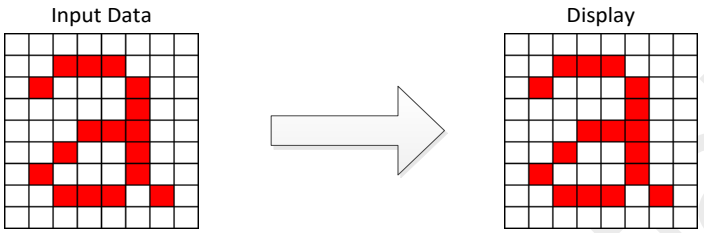
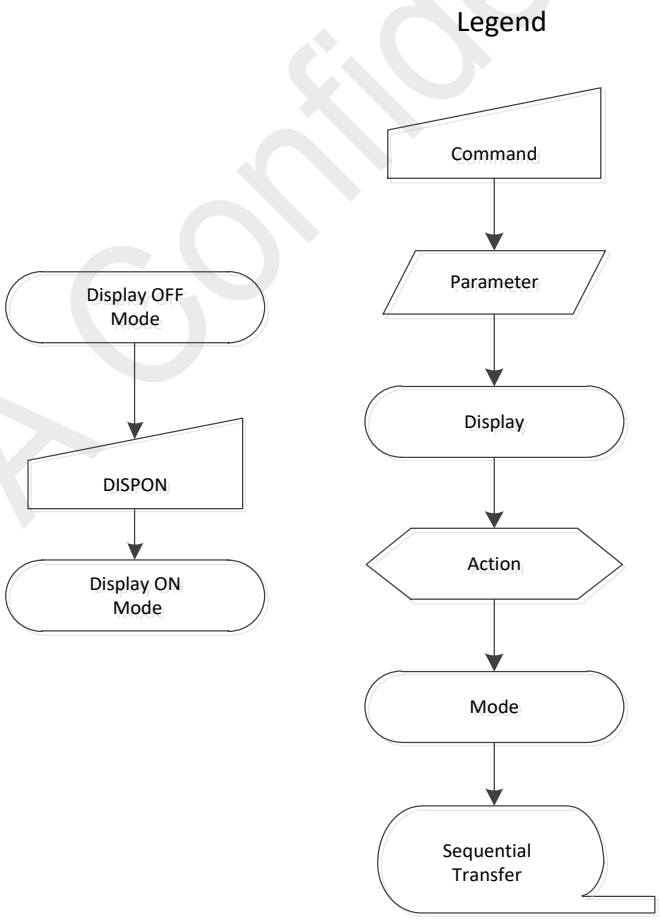
INVON: Display Inversion On (21h)

21H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	0	0	0	0	1	21
Parameter	W	No Parameter								
Description	Displayed image colors are inverted. (Example) Input Data → Display 									
Restriction	This command has no effect when module is already in inversion on mode.									
Default	WRITE ONLY, N/A									
Flow Chart										

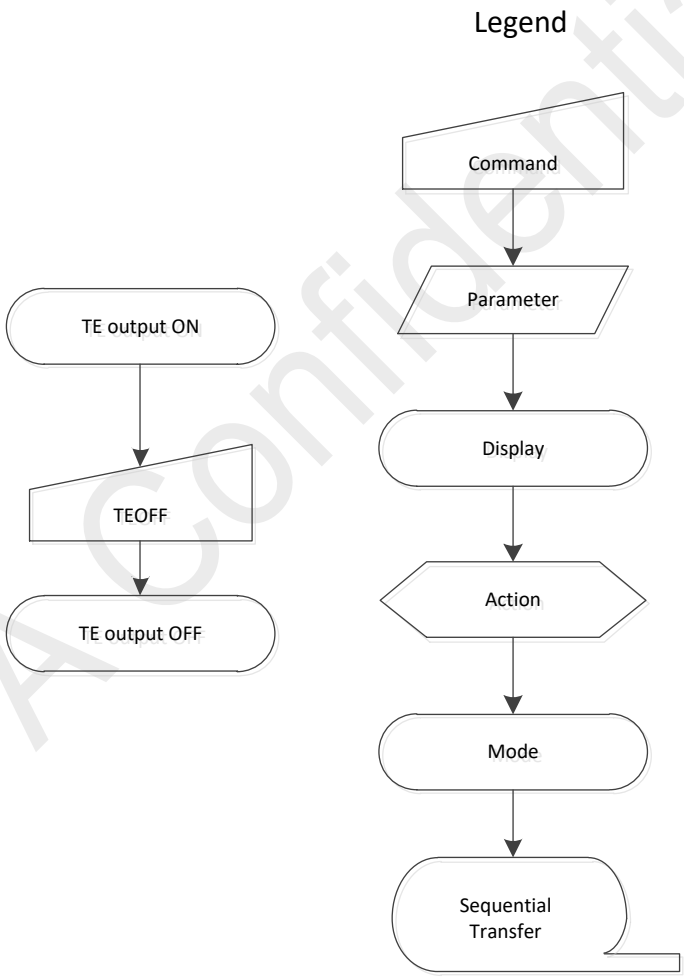
DISPOFF: Display Off (28h)

28H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	0	1	0	0	0	28
Parameter	W	No Parameter								
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the DISPLAY output is disabled and blank page inserted. (Example) 									
Restriction	This command has no effect when module is already in display off mode.									
Default	WRITE ONLY, N/A									
Flow Chart										

DISPON: Display On (29h)

29H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	0	1	0	0	1	29
Parameter	W	No Parameter								
Description	This command is used to recover from DISPLAY OFF mode. In this mode, the DISPLAY output is enabled (Example) 									
Restriction	This command has no effect when module is already in display on mode.									
Default	WRITE ONLY, N/A									
Flow Chart										

TEOFF: Tearing Effect Line OFF (34h)

34H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	1	0	1	0	0	34
Parameter	W	No Parameter								
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									
Default	WRITE ONLY, N/A									
Flow Chart										

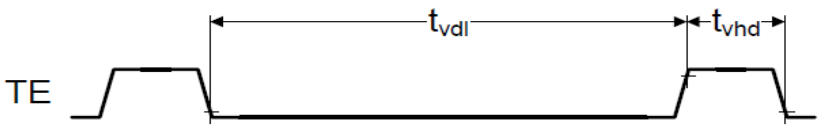
TEON: Tearing Effect Line ON (35h)

35H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	1	0	1	0	1	35
Parameter	W	-	-	-	-	-	-	-	Mode	

Description

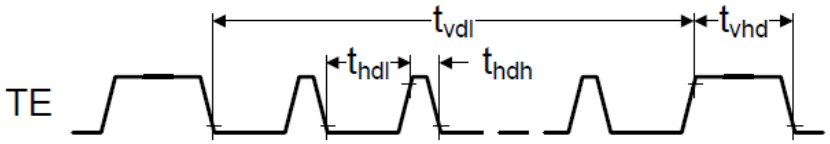
Mode: 0

The Tearing Effect Output line consists of V-Blanking information only.



Mode: 1

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.

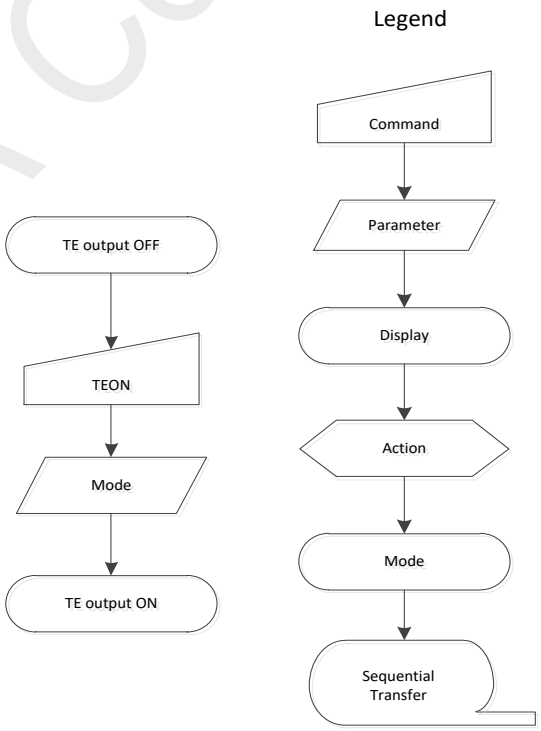


Tearing Effect output will be low if the display module is in Sleep-In mode.

This command turns on the display module's Tearing Effect output signal on the TE signal line.

Restriction	Tearing Effect output will active when IC is in display on status.
Default	WRITE ONLY, N/A

Flow Chart

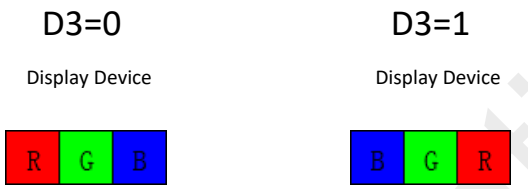


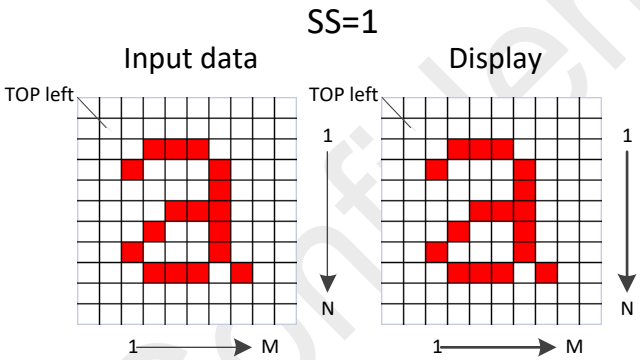
MADCTL: Set Address Mode (36h)

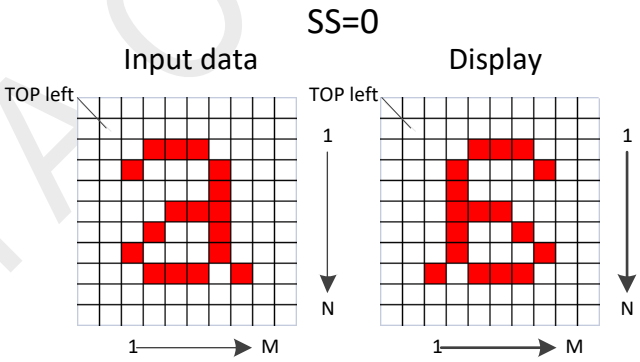
36H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	1	0	1	1	0	36
Parameter	W	-	-	-	-	D3	-	D1	D0	

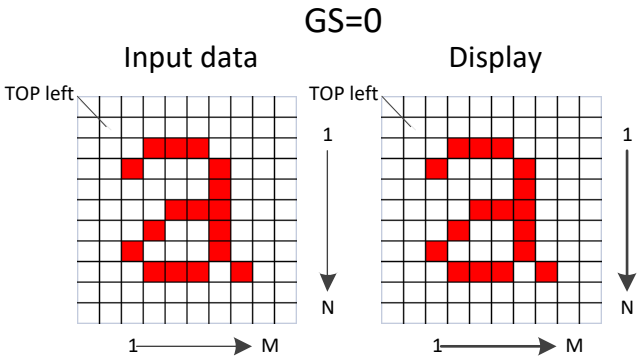
Description

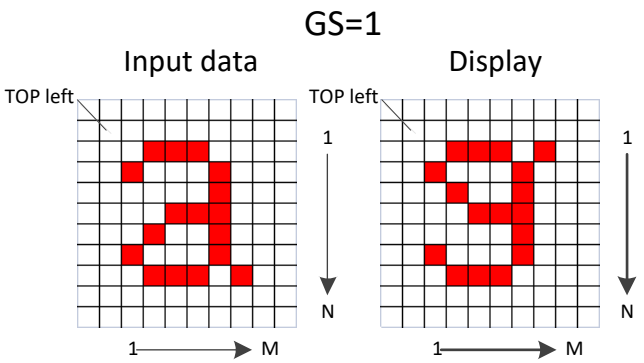
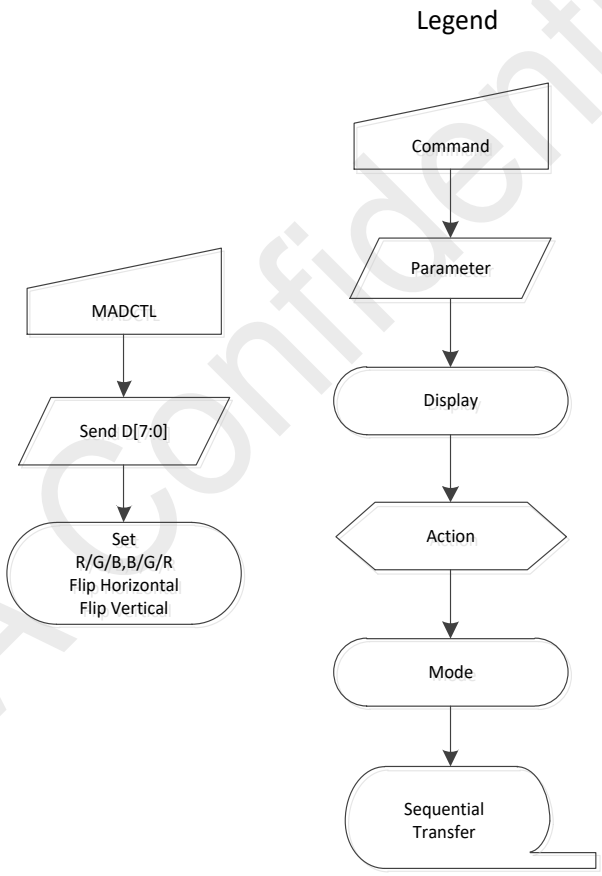
Bit	Description	Comment
D3	RGB/BGR Order	1=BGR, 0=RGB
D1	Flip Horizontal (SS)	1=Normal display 0=Flip Horizontal
D0	Flip Vertical (GS)	0=Normal display 1=Flip Vertical



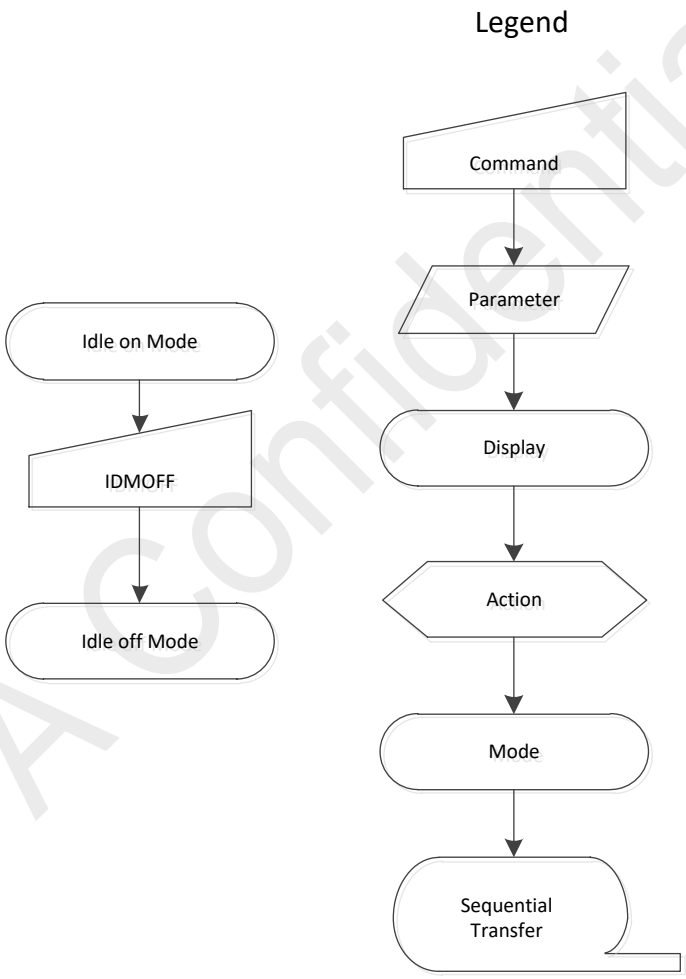






	
Restriction	N/A
Default	WRITE ONLY, N/A
Flow Chart	

IDMOFF: Idle Mode Off (38h)

38H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	1	1	0	0	0	38
Parameter	W	No Parameter								
Description	This command is used to recover from Idle mode on. In the idle off mode, the display module can display maximum 16.7M colors.									
Restriction	N/A									
Default	WRITE ONLY, N/A									
Flow Chart										

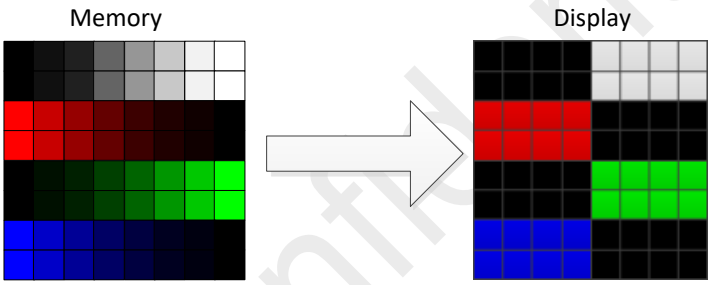
IDMON: Idle Mode On (39h)

39H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	0	1	1	1	0	0	1	39
Parameter	W	No Parameter								

Description

This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B, 8 color depth data are displayed.

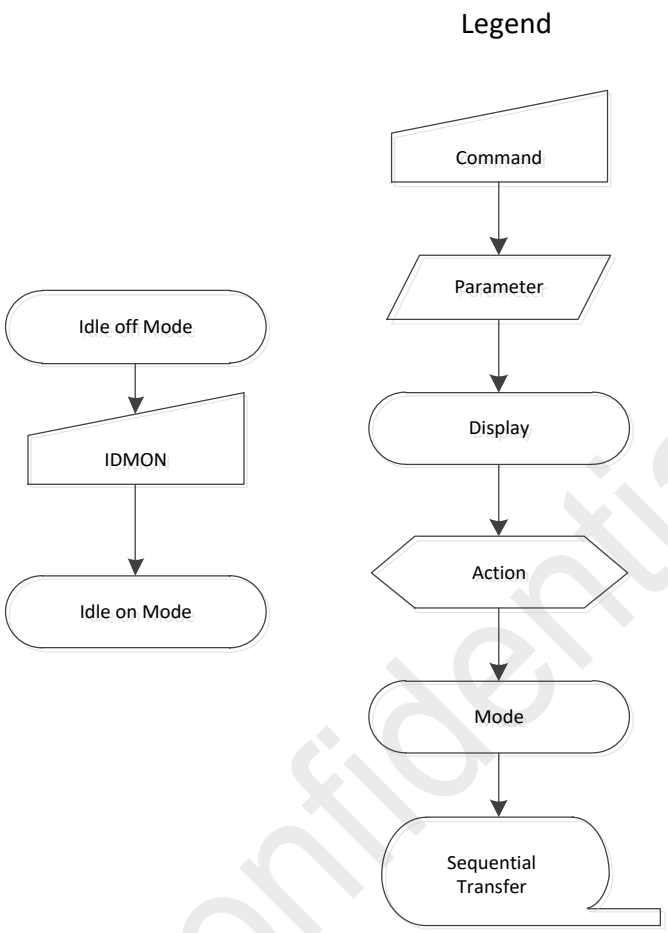
(Example)



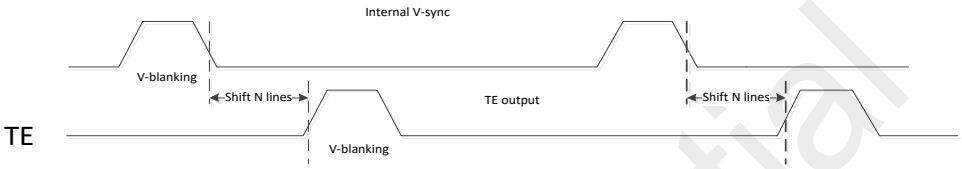
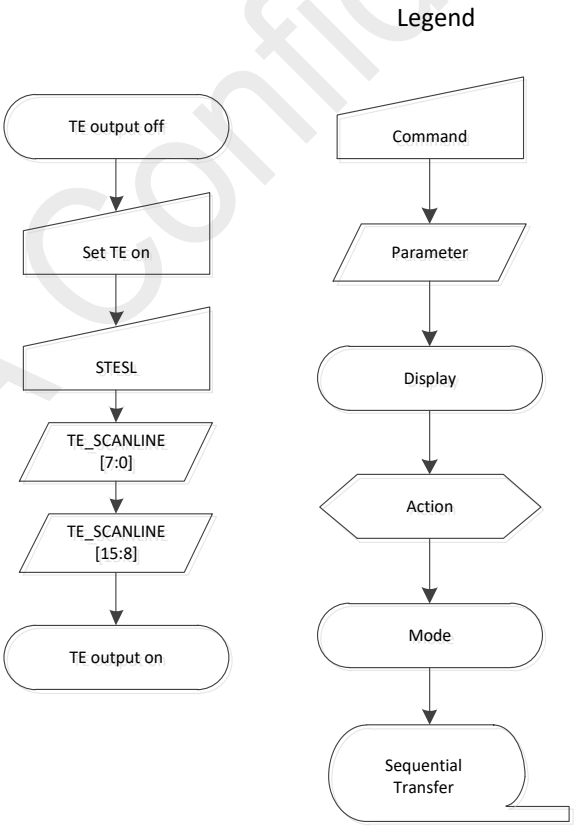
	R7-R0	G7-G0	B7-B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magent	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X=do not care

Restriction	N/A
Default	WRITE ONLY, N/A

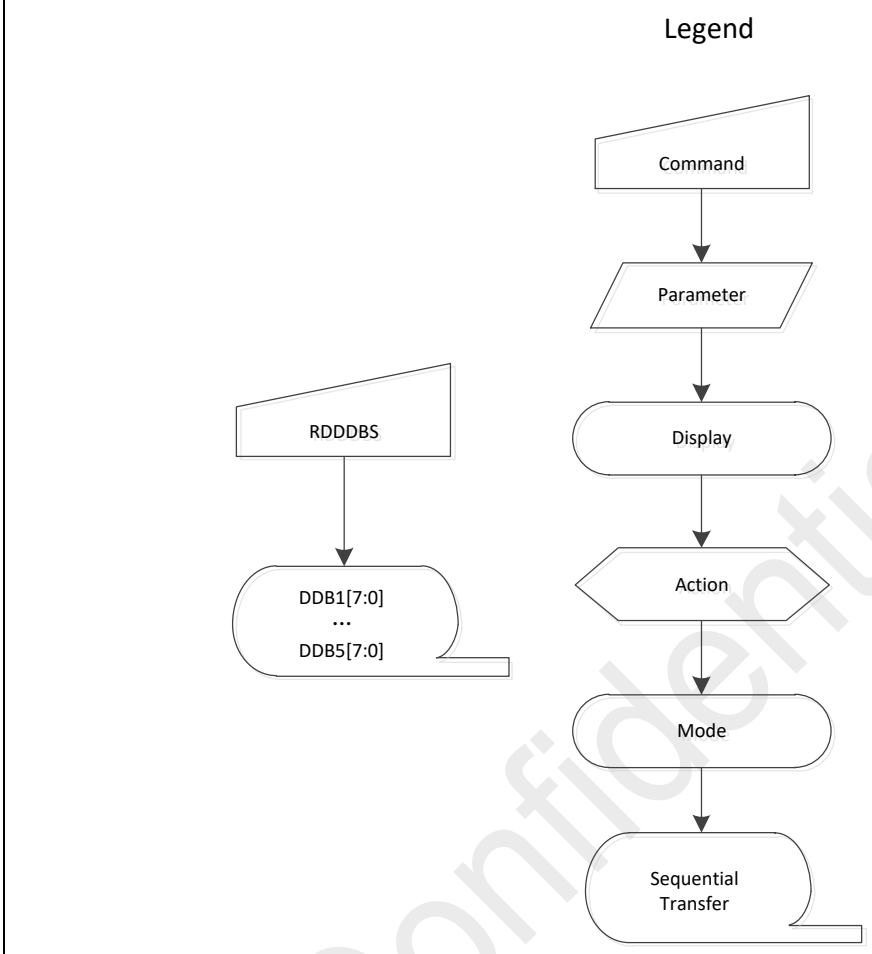
Flow Chart	

STESL: Set Tear Scanline (44h)

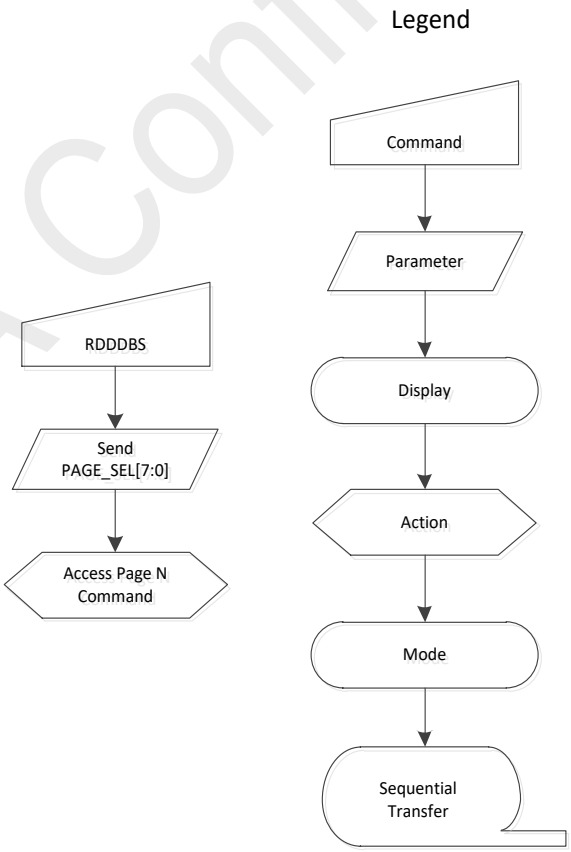
44H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	W	0	1	0	0	0	1	0	0	44
1st Parameter	W	TE_SCANLINE[15:8]								
2nd Parameter	W	TE_SCANLINE [7:0]								
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal line when the display line reaches TE_SCANLINE N. 									
Restriction	Tearing Effect output will be low if the display module is in Sleep-In mode.									
Default	WRITE ONLY, N/A									
Flow Chart										

RDDDBS: Read DDB Start (A1h)

A1H	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Address	R	1	0	0	1	0	0	0	1	A1
1st Parameter	R	DDB1[7:0]								00
2nd Parameter	R	DDB2[7:0]								72
3rd Parameter	R	DDB3[7:0]								02
4th Parameter	R	DDB4[7:0]								FF
5th Parameter	R	DDB5[7:0]								FF
Description	This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data. The format of returned data is as follows: Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 2: MS (most significant) byte of Supplier ID. Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example. Parameter 4: MS (most significant) byte of Supplier Elective Data Parameter 5: single-byte Escape or Exit Code (EEC). The code is interpreted as follows: - FFh – Exit code – there is no more data in the Descriptor Block - 00h – Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard) - Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in MIPI Alliance Standard for Device Descriptor Block (DDB). DDBs may contain many more data fields providing information about the peripheral.									
Restriction	N/A									
Default	Power On Sequence / SW Reset/HW Reset : A1h= 0x00, 0x72, 0x02, 0xFF, 0xFF									

Flow Chart	

PAGESEL: Page Select (FFh)

<table>
<tr><th>FFH</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Address</td><td>R/W</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FF</td></tr>
<tr><td>Parameter</td><td>R/W</td><td colspan="8">PAGE_SEL[7:0]</td><td>FF</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to select page
<table>
<tr><th>PAGE_SEL[7:0]</th><th>Function</th></tr>
<tr><td>00</td><td>select page 0 command</td></tr>
<tr><td>01</td><td>select page 1 command</td></tr>
<tr><td>02</td><td>select page 2 command</td></tr>
<tr><td>03</td><td>select page 3 command</td></tr>
<tr><td>04</td><td>select page 4 command</td></tr>
<tr><td>05</td><td>select page 5 command</td></tr>
<tr><td>07</td><td>select page 7 command</td></tr>
<tr><td>0C</td><td>select page C command</td></tr>
<tr><td>FF</td><td>select page FF command</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">N/A</td></tr>
<tr><td>Default</td><td colspan="10">Power On Sequence / SW Reset/HW Reset : FFh= 0xFF</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

12. Reliability

TBD

13. Handling Precautions

- Mounting Method

The MOLEDA panel of SeeYA module consists of one silicon backplane and one cover glass, which can easily get damaged. Since the module is constructed as to be fixed by utilizing fitting holes in the printed circuit board. Extreme care should be used when handling the MOLED.

- Caution of MOLED Handling and Cleaning

When cleaning the display surface, use soft solvent as recommended isopropyl alcohol and wipe gently, don't wipe the display surface with dry or hard materials that will damage the polarizer surface, don't use the following solvent, Water, Ketone, Aromatics

- Caution of Against Static Charge

For MOLED module, use C-MOS drivers, therefore we recommend that you, connect any unused input terminal to VCI or VSS, do not input and signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects MOLED. Against static charge, you should make sure that the product is safe or not by experiment in advance.

- Packing

The packing principle is that MOLED module should keep its packing condition at the time of delivery. For safety & avoiding the module damage, Carton box must stack the below 4 boxes.

When storing the MOLED after unpacking, note the followings. MOLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.

To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

- Caution for Operation

If you do not follow normal POWER ON, OFF sequence or abnormal operating, then MOLED module can be damaged electro-optically and does not recover. Do not change software without SeeYA confirmation.

Response time may extremely delay at a temperature lower than operating range, MOLED does not normally operate at a high temperature. But this may recover at a proper temperature.

When you set optimal operating voltage to MOLED module, you can see the optimal contrast of MOLED. So, add voltage controllable function at SET Module.

MOLED module may not display normally when twisting power or pressing power is added. Therefore, you should secure MOLED module maximum thickness at set assembly not to have any pressure affect MOLED module.

Electro-chemical reaction may occur when there is humidity on pad, therefore, you should use MOLED Module below maximum operating humidity.

MOLED Module Power VDD should be designed to protect surge current at SET Module. You should not damage connector and cable for MOLED module assembly by force folding or by applying extreme power.

MOLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage MOLED module by surrounding elements.

To satisfy EMI standards, you should plan your design after considering emitting energy. We can't guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area. Image-sticking may occur if MOLED displays same image for a long time, so you need to make a change for MOLED.

- Storage

Place in a dark place where neither exposure to direct sunlight or any fluorescent light is permitted and keep at room temperature & room humidity. Store with no contact with polarizer surface. It is recommended to store them as they have been contained in the inner container when we delivered them.

- Safety Precautions

Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMOLED module, dust adhesion, or scratches on the display part. In the event that the contents of AMOLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary. Do not use the AMOLED module for the special purpose besides display units. Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken. For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

- Precautions before use

You should discuss the following case with SeeYA:

- in case of any questions about contents of this "Specification for Approval".
- in case of occurring new problems not mentioned at this "Specification for Approval".
- in case of your request about income inspection specification change.
- in case of occurring new problem at your driving test.

*If SeeYA has to change the conditions specified in the specification, previously shall be held and decided.

14. Packing

TBD