Tentative

SONY

0.6 cm (Type 0.23) Active Matrix Color OLED Panel Module

ECX336BF

1. Overview / Application

ECX336 BF is a 0.6 cm (0.23inch) diagonal, 640(RGB) × 400 dots active matrix color OLED (Organic Light Emitting Display) panel module based on single crystal silicon transistors. The module integrates panel driver and logic driver, and achieves smaller size, light in weight and high resolution.

(Potential applications: Head mounted displays, View finders, Small monitors etc.)

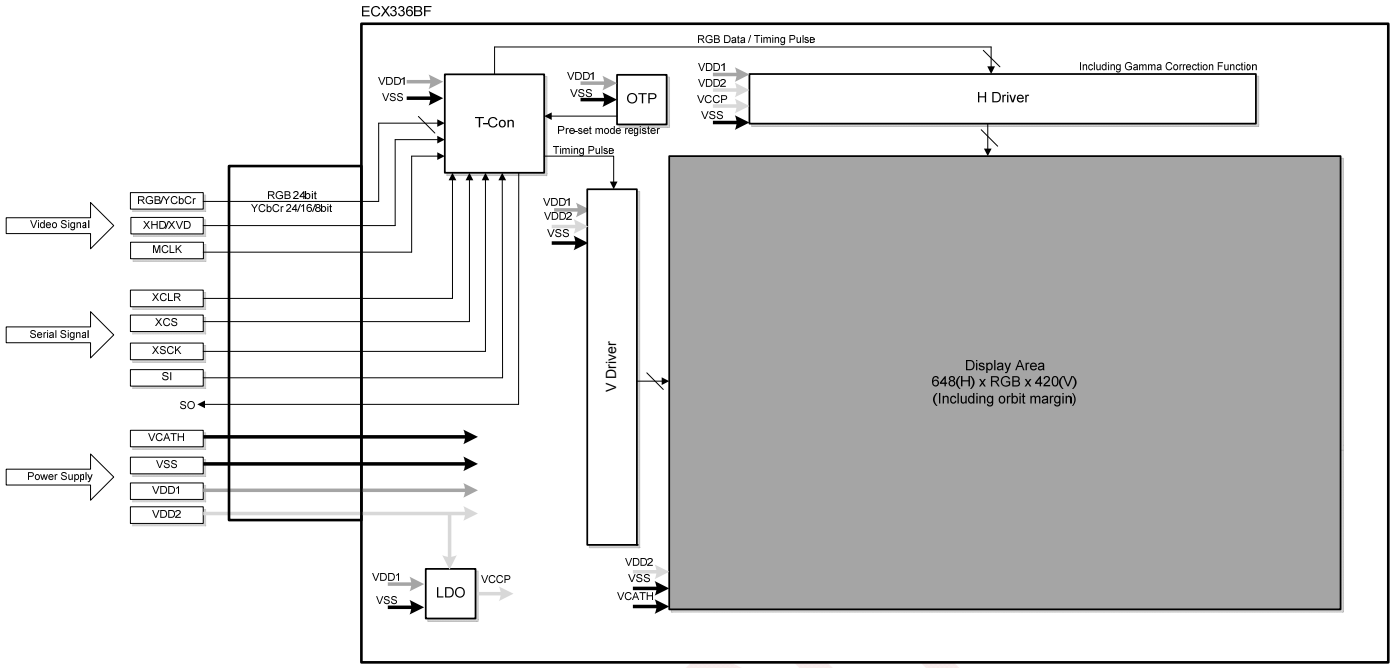
2. Features

- Small-size, high resolution 0.23 nHD+ display dots 640 (RGB) × 400 = 0.77M dots
- Ultra high contrast
- Wide color gamut
- Fast response
- Thin and light in weight
- Power-saving (PS) mode
- Scan direction selection, up or down and right or left.
- Orbit supported
- Input interface that supports parallel RGB 24-bit, YCbCr 24-bit and YCbCr 16-bit input

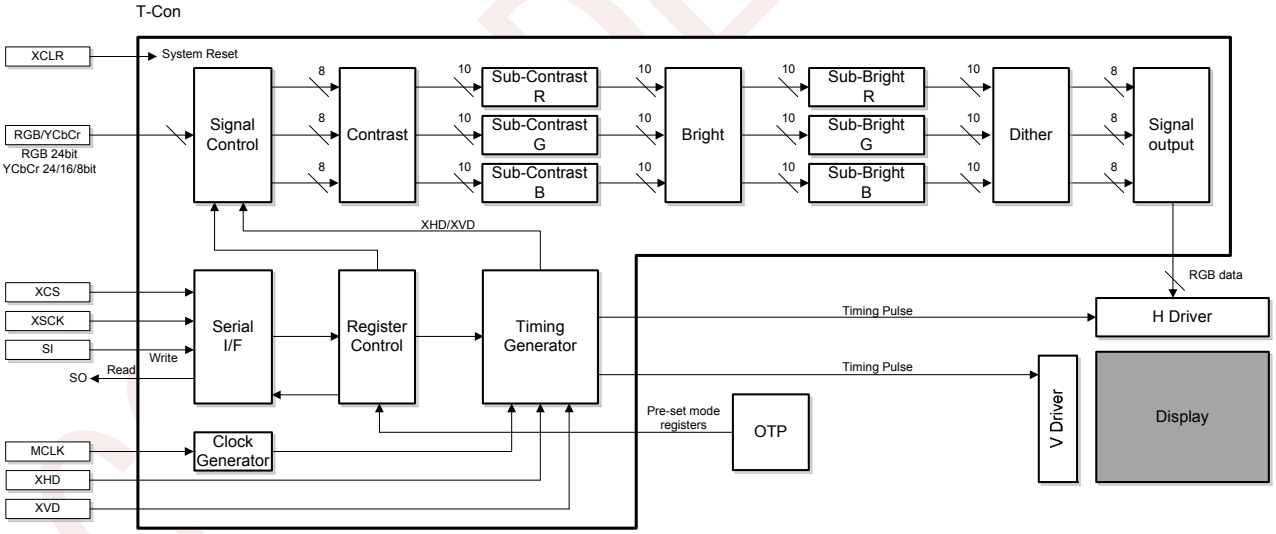
3. Module Structure

Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

4. System Block Diagram

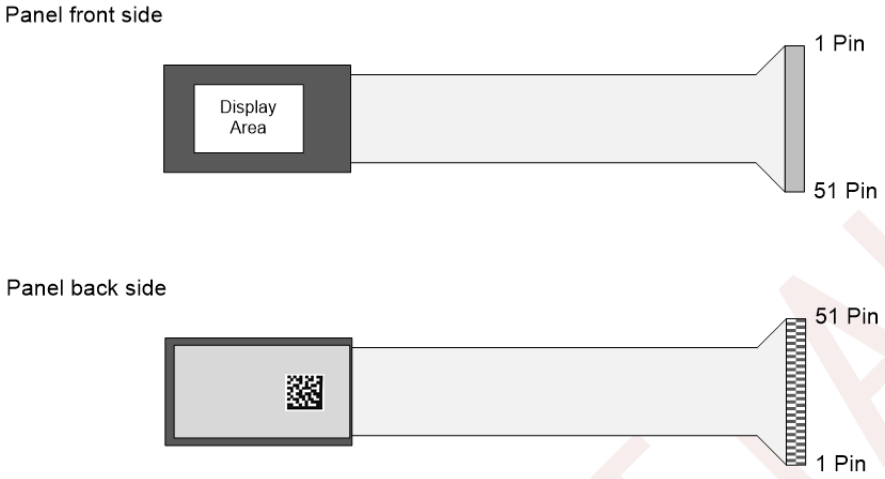


Details of T-Con Block



5. Pin Description

5.1. Pin Assignment



5.2. Pin Description

Pin No.	Symbol	Type	Pin Description	Equivalent circuit
1	VCATH	Power Supply	EL cathode power supply	
2	VCCP	Power supply	VCCP power supply	
3	VCAL	Output	Temperature sensor output voltage	*6
4	VG255	Output	Gamma top reference voltage (255)	*6
5	VG0	Output	Gamma bottom reference voltage (0)	*6
6	VOFS	Output	Gamma offset voltage	*6
7	VREF	Output	Gamma reference voltage	*6
8	VDD2	Power supply	10V power supply	
9	VSS	Power supply	GND	
10	VDD1	Power supply	1.8V power supply	
11	MCLK	Input	Master clock	*1
12	XHD	Input	Horizontal sync signal (negative polarity)	*1
13	XVD	Input	Vertical sync signal (negative polarity)	*1
14	VSS	Power supply	GND	
15	XCLR	Input	System reset (negative polarity)	*2
16	DATA7	Input	Video signal input (refer to 5.3.)	*1
17	DATA6	Input	Video signal input (refer to 5.3.)	*1
18	DATA5	Input	Video signal input (refer to 5.3.)	*1
19	DATA4	Input	Video signal input (refer to 5.3.)	*1
20	DATA3	Input	Video signal input (refer to 5.3.)	*1

Pin No.	Symbol	Type	Pin Description	Equivalent circuit
21	DATA2	Input	Video signal input (refer to 5.3.)	*1
22	DATA1	Input	Video signal input (refer to 5.3.)	*1
23	DATA0	Input	Video signal input (refer to 5.3.)	*1
24	DATA15	Input	Video signal input (refer to 5.3.)	*1
25	DATA14	Input	Video signal input (refer to 5.3.)	*1
26	DATA13	Input	Video signal input (refer to 5.3.)	*1
27	DATA12	Input	Video signal input (refer to 5.3.)	*1
28	DATA11	Input	Video signal input (refer to 5.3.)	*1
29	DATA10	Input	Video signal input (refer to 5.3.)	*1
30	DATA9	Input	Video signal input (refer to 5.3.)	*1
31	DATA8	Input	Video signal input (refer to 5.3.)	*1
32	DATA23	Input	Video signal input (refer to 5.3.)	*1
33	DATA22	Input	Video signal input (refer to 5.3.)	*1
34	DATA21	Input	Video signal input (refer to 5.3.)	*1
35	DATA20	Input	Video signal input (refer to 5.3.)	*1
36	DATA19	Input	Video signal input (refer to 5.3.)	*1
37	DATA18	Input	Video signal input (refer to 5.3.)	*1
38	DATA17	Input	Video signal input (refer to 5.3.)	*1
39	DATA16	Input	Video signal input (refer to 5.3.)	*1
40	TEST	Input	Test pin (connect to GND)	*3
41	XSCK	Input	Serial communication Serial clock (negative polarity)	*2
42	XCS	Input	Serial communication Chip select (negative polarity)	*2
43	SI	Input	Serial communication Data input	*2
44	SO	Output	Serial communication Data output	*7
45	TEST	Output	Test pin (no connect)	*4
46	TEST	Input	Test pin (connect to GND)	*5
47	VSS	Power supply	GND	
48	VDD1	Power supply	1.8V power supply	
49	VSS	Power supply	GND	
50	VDD2	Power supply	10V power supply	
51	VCCP	Power supply	VCCP power supply	*6

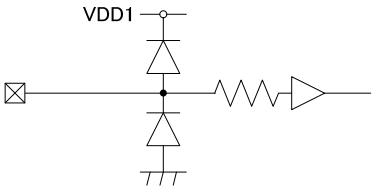
5.3. Pin description (video signal input pin)

Input interface supports parallel RGB 24 bit, YCbCr 24 bit, 16 bit inputs.

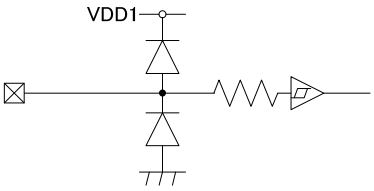
Pin No.	Symbol	RGB 24bit	YCbCr / YPbPr 24bit	YCbCr / YPbPr 16bit
16	DATA7	Digital G signal G[7]	Luma signal Y[7]	Luma signal Y[7]
17	DATA6	Digital G signal G[6]	Luma signal Y[6]	Luma signal Y[6]
18	DATA5	Digital G signal G[5]	Luma signal Y[5]	Luma signal Y[5]
19	DATA4	Digital G signal G[4]	Luma signal Y[4]	Luma signal Y[4]
20	DATA3	Digital G signal G[3]	Luma signal Y[3]	Luma signal Y[3]
21	DATA2	Digital G signal G[2]	Luma signal Y[2]	Luma signal Y[2]
22	DATA1	Digital G signal G[1]	Luma signal Y[1]	Luma signal Y[1]
23	DATA0	Digital G signal G[0]	Luma signal Y[0]	Luma signal Y[0]
24	DATA15	Digital R signal R[7]	Chrominance signal Cr[7]	Chrominance signal CbCr[7]
25	DATA14	Digital R signal R[6]	Chrominance signal Cr[6]	Chrominance signal CbCr[6]
26	DATA13	Digital R signal R[5]	Chrominance signal Cr[5]	Chrominance signal CbCr[5]
27	DATA12	Digital R signal R[4]	Chrominance signal Cr[4]	Chrominance signal CbCr[4]
28	DATA11	Digital R signal R[3]	Chrominance signal Cr[3]	Chrominance signal CbCr[3]
29	DATA10	Digital R signal R[2]	Chrominance signal Cr[2]	Chrominance signal CbCr[2]
30	DATA9	Digital R signal R[1]	Chrominance signal Cr[1]	Chrominance signal CbCr[1]
31	DATA8	Digital R signal R[0]	Chrominance signal Cr[0]	Chrominance signal CbCr[0]
32	DATA23	Digital B signal B[7]	Chrominance signal Cb[7]	GND
33	DATA22	Digital B signal B[6]	Chrominance signal Cb[6]	GND
34	DATA21	Digital B signal B[5]	Chrominance signal Cb[5]	GND
35	DATA20	Digital B signal B[4]	Chrominance signal Cb[4]	GND
36	DATA19	Digital B signal B[3]	Chrominance signal Cb[3]	GND
37	DATA18	Digital B signal B[2]	Chrominance signal Cb[2]	GND
38	DATA17	Digital B signal B[1]	Chrominance signal Cb[1]	GND
39	DATA16	Digital B signal B[0]	Chrominance signal Cb[0]	GND

5.4. Equivalent Circuits

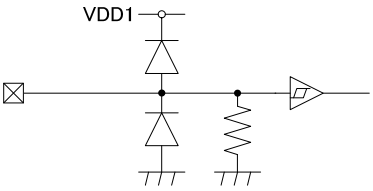
※1 Pin No.11, 12, 13 & 16–39



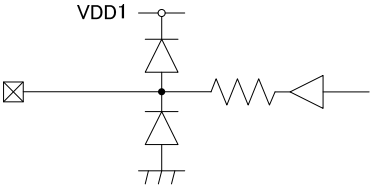
※2(Schmitt) Pin No. 15, 41, 42 & 43



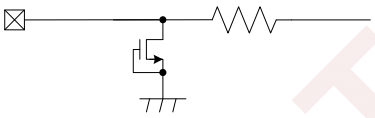
※3(Schmitt) Pin No. 40



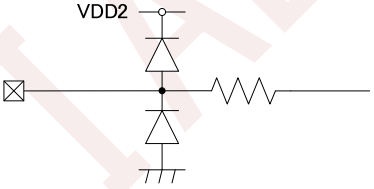
※4 Pin No. 45



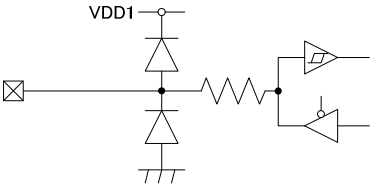
※5 Pin No. 46



※6 Pin No. 3, 4, 5, 6, 7 & 51



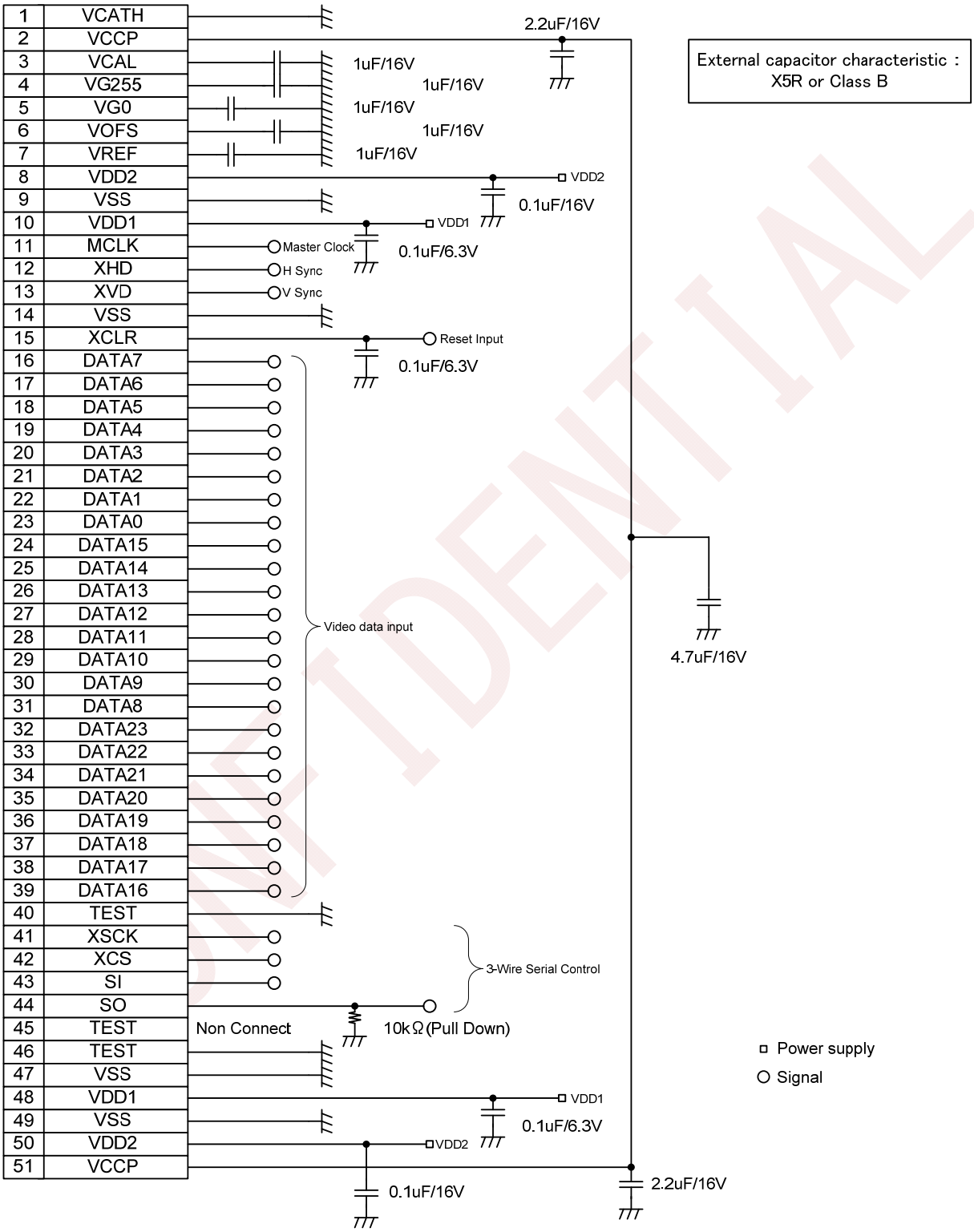
※7 Pin No. 44



5.5. Reference Peripheral circuits

Regarding power supply capacitor connections, mount an approximately 2.2 µF to 10 µF capacitor for each power supply. Insufficient capacitance may affect the picture quality.

Pin No. 2 and No.51 should be connected each other as close as possible.



※Above circuit is just one of typical example for reference to drive the module. Sony does NOT take any liability if the circuit example causes any problem because the circuit is only for reference.

6. Absolute Maximum Ratings

Item	Symbol	Min.	Maximum Ratings	Unit
1.8V power supply	VDD1	-0.3	2.0	V
10V power supply	VDD2	-0.3	12.0	V
EL cathode voltage	Vcath	-0.3	0.3	V
Logic input voltage	Vi	-0.3	VDD1+ 0.3	V
Storage temperature	Tpnl	-30	+80	°C

7. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
1.8V power supply	VDD1	1.62	1.8	1.98	V
10V power supply	VDD2	9.7	10.0	10.3	V
EL cathode voltage	Vcath	-0.3	0	0.3	V
Operating temperature range	Tpnl	-20		70	°C

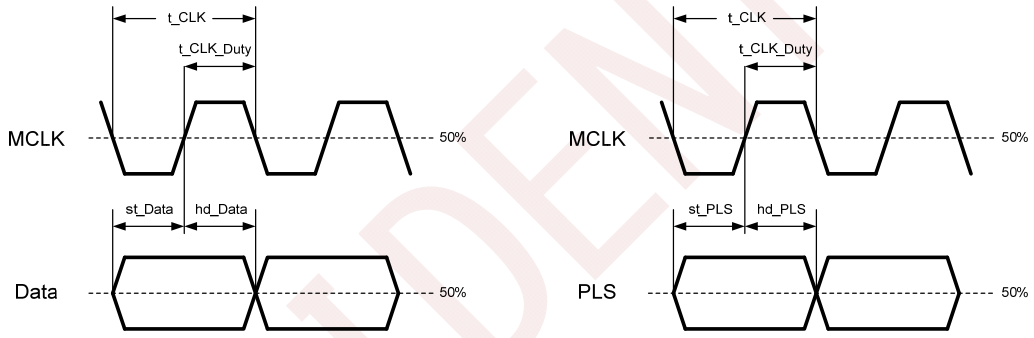
8. Electrical Characteristics

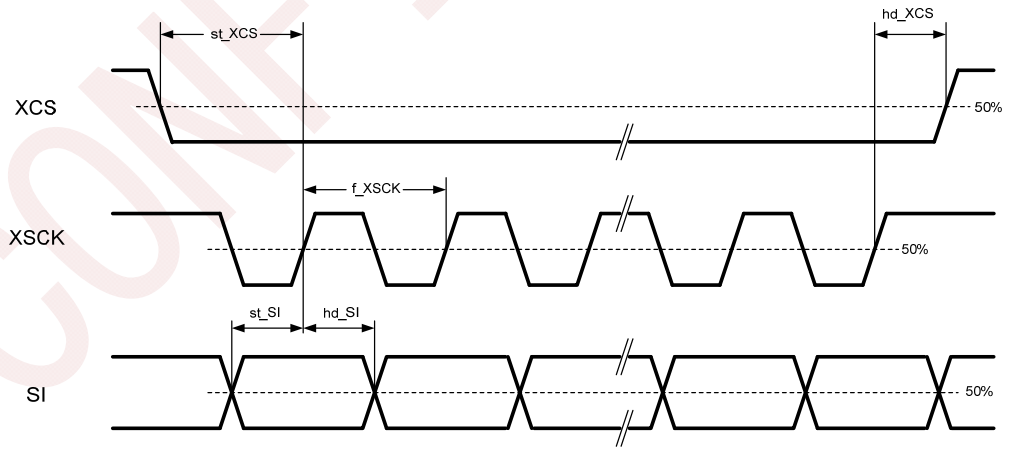
8.1. DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	VIH		0.7VDD1		VDD1	V
Low level input voltage	VIL		0		0.3VDD1	V
High level input voltage	Vt+	Schmitt input	0.7VDD1		VDD1	V
Low level input voltage	Vt-	Schmitt input	0		0.3VDD1	V
Vt+ - Vt-	Vhys	Schmitt input		0.50		V
Logic high level output voltage	VOH		VDD1-0.4			V
Logic low level output voltage	VOL				0.4	V

8.2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse cycle	t_CLK		36.6※	37.0		ns
Clock duty	t_CLK_Duty	All mode (54 MHz) common	40	50	60	%
Data setup time	st_Data	Vi = 1.62 to 1.98 V	2.5			ns
Data hold time	hd_Data	Vi = 1.62 to 1.98 V	1.8			ns
Control pulse setup time	st_PLS	Vi = 1.62 to 1.98 V	2.5			ns
Control pulse hold time	hd_PLS	Vi = 1.62 to 1.98 V	1.8			ns
XSCK frequency	f_SCLK			0.8	2.5	MHz
XCS setup time	st_XCS		0.4			µs
XCS hold time	hd_XCS		0.2			µs
SI setup time	st_SI		0.2			µs
SI hold time	hd_SI		0.2			µs





8.3. Power Consumption

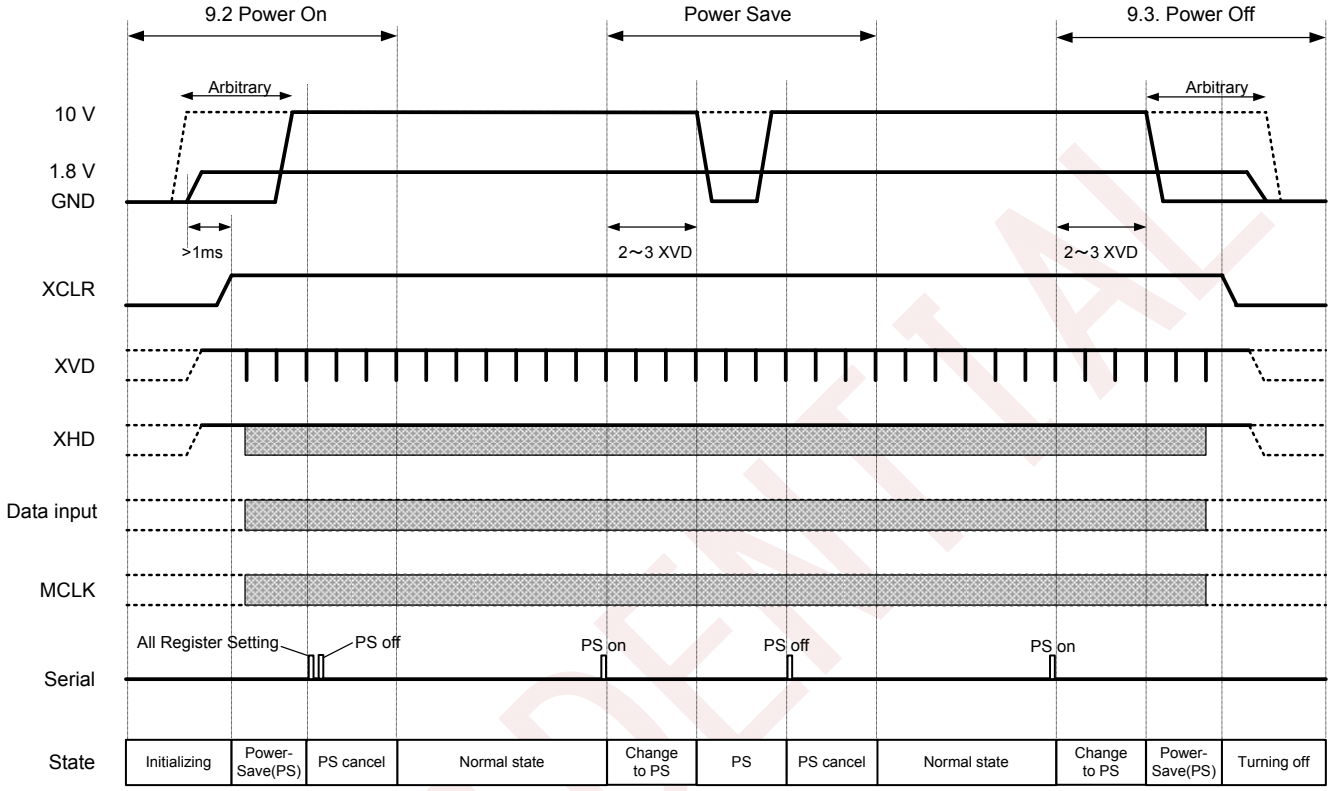
Item	Symbol	Conditions	Typical						Unit
			2000	1500	800	500	300	Standby	cd/m^2
VDD1 power consumption	PDD1	VDD1 = 1.8V VDD2 = 10.0V Tpnl = 40°C (*)	7					0.10	mW
VDD2 power consumption	PDD2		185	155	113	95	83	0.02	mW
Total	PTTL		195	162	120	102	90	0.12	mW

*: All white raster display, Clock frequency = 27MHz, Frame rate = 60Hz

9. Power Supply Sequence

Power supply sequence shown in below should be followed to avoid panel breakdown caused by excessive current flow into the internal circuit.

9.1. Sequence Diagram



9.2. Power On Sequence

1. Set XCLR to low and turn on 1.8V power supply to initialize.
2. 1ms after completion of 1.8 V power supply rising, set XCLR to high, then the panel changes to the power-saving mode.
3. After XCLR set to high, turn on 10V power supply.
4. Implement all the register settings and perform PS register off by serial communication to cancel power-saving mode.

Then the panel changes to the normal state.

*Complete turning on of 10V power supply before power saving mode off setting, while the order of turning on of 1.8V and 10V power supply is not restricted.

9.3. Power Off Sequence

1. Perform PS register on by serial communication to enter power-saving mode.
2. After completion of changing to power-saving mode, set XCLR to low and turn off 1.8V and 10V power supplies.

*Turning off of 1.8V power supplies should be done after completion of setting XCLR to low, while the order of turning off of 1.8V and 10V power supply is not restricted.

10. Description of Functions

10.1. Serial Communication

10.1.1 Register Map

Address	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Initial
+0x00	RGB_YCB	YCB_DEC	0	1	DWN	RGT	MCLKPOL	PS0	0E
+0x01	VCAL_MON	FORMAT_SEL_DATA[1:0]		YCB_P	FORMAT_SEL_V[1:0]		FORMAT_SEL_H[1:0]		00
+0x02	0	CALSEL[1:0]		ORBIT_H[4:0]					00
+0x03	0	0	0	ORBIT_V[4:0]					00
+0x04	0	0	1	1	1	1	1	1	3F
+0x05	0	0	0	0	DITHERON	LUMINANCE[2:0]			00
+0x06	0	0	0	0	0	0	0	0	00
+0x07	0	1	0	0	0	0	0	0	40
+0x08	0	0	0	0	0	OTPCALDAC_REGDIS	0	OTPDG_REGDIS	00
+0x09	CAP_EN	0	CAP_REFRESH[5:0]						00
+0x0A	120MODE	1	0	0	0	0	0	0	40
+0x0B	0	0	0	0	0	0	0	0	00
+0x0C	0	0	0	0	0	0	0	0	00
+0x0D	0	0	0	0	0	0	0	0	00
+0x0E	0	0	0	0	0	0	0	0	00
+0x0F	0	1	0	1	0	1	1	0	56
+0x10	0	0	0	0	0	0	0	0	00
+0x11	0	0	0	0	0	0	0	0	00
+0x12	0	0	0	0	0	0	0	0	00
+0x13	0	0	0	0	0	0	0	0	00
+0x14	0	0	0	0	0	0	0	0	00
+0x15	0	0	0	0	0	0	0	0	00
+0x16	0	0	0	0	0	0	0	0	00
+0x17	0	0	0	0	0	0	0	0	00
+0x18	0	0	0	0	0	0	0	0	00
+0x19	0	0	0	1	0	0	0	0	00
+0x1A	0	0	0	0	0	0	0	0	00
+0x1B	0	0	0	0	0	0	0	0	00
+0x1C	0	0	0	0	0	0	0	0	00
+0x1D	0	0	0	0	0	0	0	0	00
+0x1E	0	0	0	0	0	0	0	0	00
+0x1F	0	0	0	0	0	0	0	0	00
+0x20	0	0	0	0	0	0	0	CONT[8]	01
+0x21	CONT[7:0]								00
+0x22	0	RCONT[6:0]							40
+0x23	0	GCONT[6:0]							40
+0x24	0	BCONT[6:0]							40
+0x25	BRT[7:0]								80
+0x26	0	RBRT[6:0]							40
+0x27	0	GBRT[6:0]							40
+0x28	0	BBRT[6:0]							40
+0x29	0	0	0	0	1	0	1	0	10
+0x2A	CALDAC[7:0]								80
+0x2B	0	1	0	1	1	0	1	0	40
+0x2C	0	0	0	0	0	1	0	0	04
+0x2D	H_ACT_U[7:0]								7A
+0x2E	0	0	0	0	0	H_ACT_D[10:8]			02
+0x2F	H_ACT_D[7:0]								FA
+0x30	V_ACT_U[7:0]								26
+0x31	0	0	0	0	0	0	V_ACT_D[9:8]		01
+0x32	V_ACT_D[7:0]								B6
+0x33	0	0	0	0	0	0	0	0	00

+0x34	0	0	0	0	0	0	1	1	03
+0x35	0	1	0	1	1	0	1	0	5A
+0x36	0	0	0	0	0	0	DE_U[9:8]		00
+0x37	DE_U[7:0]								76
+0x38	0	0	0	0	0	0	DE_D[9:8]		02
+0x39	DE_D[7:0]								FE
+0x3A	0	0	0	0	0	0	1	0	02
+0x3B	0	0	0	0	1	1	0	1	0D
+0x3C	0	0	0	0	0	0	WSST1_U[9:8]		00
+0x3D	WSST1_U[7:0]								1B
+0x3E	0	0	0	0	0	0	WSST1_D[9:8]		00
+0x3F	WSST1_D[7:0]								1C
+0x40	0	0	0	0	0	0	WSST2_U[9:8]		01
+0x41	WSST2_U[7:0]								F3
+0x42	0	0	0	0	0	0	WSST2_D[9:8]		01
+0x43	WSST2_D[7:0]								F4
+0x44	1	0	0	0	0	0	0	0	80
+0x45	0	0	0	0	0	0	0	0	00
+0x46	0	0	0	0	0	0	0	WSEN1_U[8]	00
+0x47	WSEN1_U[7:0]								41
+0x48	WSEN1_W[7:0]								08
+0x49	0	0	0	0	0	0	WSEN2_U[9:8]		02
+0x4A	WSEN2_U[7:0]								FC
+0x4B	WSEN2_W[7:0]								08
+0x4C	WSEN3_U[7:0]								16
+0x4D	WSEN3_W[7:0]								08
+0x4E	0	0	0	0	0	0	0	DSEN_U[8]	00
+0x4F	DSEN_U[7:0]								4E
+0x50	0	0	0	0	0	0	DSEN_W[9:8]		02
+0x51	DSEN_W[7:0]								C2
+0x52	VCK_U[7:0]								01
+0x53	VCK_W[7:0]								2D
+0x54	SIGSELREF_U[7:0]								01
+0x55	SIGSELREF_W[7:0]								2B
+0x56	0	0	0	0	SIGSELOFS_U[3:0]				00
+0x57	SIGSELOFS_W[7:0]								2B
+0x58	SIGSEL_W[7:0]								23
+0x59	SELREF_U[7:0]								02
+0x5A	SELREF_W[7:0]								25
+0x5B	SELOFS_U[7:0]								02
+0x5C	SELOFS_W[7:0]								25
+0x5D	SEL_U[7:0]								02
+0x5E	SEL_W[7:0]								1D
+0x5F	0	0	0	0	0	0	0	0	00
+0x60	0	0	1	0	0	0	1	1	23
+0x61	0	0	0	0	0	0	1	0	02
+0x62	0	0	0	1	1	1	0	1	1D
+0x63	0	0	0	0	0	0	0	AZEN_U[8]	00
+0x64	AZEN_U[7:0]								1A
+0x65	0	0	0	0	0	0	AZEN_D[9:8]		03
+0x66	AZEN_D[7:0]								0A
+0x67	0	0	0	0	0	0	0	0	00
+0x68	0	0	0	0	0	0	0	0	00
+0x69	0	0	0	0	0	0	0	0	00
+0x6A	0	0	0	0	0	0	0	0	00
+0x6B	0	0	0	0	0	0	0	0	00
+0x6C	0	0	0	0	0	0	0	0	00
+0x6D	0	0	0	0	0	0	0	0	00

+0x6E	0	0	0	0	0	0	0	0	00
+0x6F	0	0	0	0	0	0	0	0	00
+0x70	0	0	0	0	0	0	0	0	00
+0x71	0	0	0	0	0	0	0	0	00
+0x72	0	0	0	0	0	0	0	0	00
+0x73	0	0	0	0	0	0	0	0	00
+0x74	0	0	0	0	0	0	0	0	00
+0x75	0	0	0	0	0	0	0	0	00
+0x76	0	0	0	0	0	0	0	0	00
+0x77	0	0	0	0	0	0	0	0	00
+0x78	0	0	0	0	0	0	0	0	00
+0x79	0	1	1	0	1	0	0	0	68
+0x7A	0	0	0	0	0	0	0	0	00
+0x7B	0	0	0	0	0	0	0	0	00
+0x7C	0	0	0	0	0	0	0	0	00
+0x7D	0	0	0	0	0	0	0	0	00
+0x7E	0	0	0	0	0	0	0	0	00
+0x7F	0	0	0	0	0	0	0	0	00
+0x80	0	0	0	0	0	0	0	RD_ON	00
+0x81	RD_ADDR[7:0]								00

10.1.2. Description of Registers

Register name	Bits	V sync	Function	Related Items
PS0	1		Power Save Mode 0: Power Save on 1: Power Save off	9.
MCLKPOL	1		MCLK polarity switching 0: Negative polarity 1: Positive polarity (default)	—
RGT	1		Selection of rightward / leftward scan	10.4.
DWN	1		Selection of upward / down ward scan	10.4.
YCB_DEC	1		Selection of YCbCr / YPbPr conversion	10.2.
RGB_YCB	1		Selection of RGB / YCbCr (YPbPr) format	10.2.
FORMAT_SEL_H	2		Selection of input format (number of horizontal active pixels)	10.3.
FORMAT_SEL_V	2		Selection of input format (number of vertical active pixels)	10.3.
YCB_P	1		Selection of YCbCr (YPbPr) input pattern	10.2.
FORMAT_SEL_DATA	2		Selection of YCbCr (YPbPr) input format	10.2.
VCAL_MON	1		Temperature sensing circuit monitoring on / off	10.5.
ORBIT_H	5	○	Horizontal orbit adjustment	10.10.1
CALSEL	2		VCAL output selection	10.5.
ORBIT_V	5	○	Vertical orbit adjustment	10.10.2.
LUMINANCE	3		Luminance and white chromaticity preset mode selection	10.8.
DITHERON	1		Dithering On/Off	10.9.
OTPDG_REGDIS	1		White chromaticity preset mode on / off	10.8.
OTPCALDAC_REGDIS	1		Luminance preset mode on / off	10.8.
CAP_REFRESH	6		Capture mode setting (normally fixed to 0)	-
CAP_EN	1		Capture mode on / off (normally fixed to 0:off)	-

Register name	Bits	V sync	Function	Related Items
120MODE	1		120Hz mode On / Off (Normally fixed to 0:off)	-
CONT	9		Contrast adjustment	10.7.1.
RCONT	7		R sub-contrast adjustment	10.7.1.
GCONT	7		G sub-contrast adjustment	10.7.1.
BCONT	7		B sub-contrast adjustment	10.7.1.
BRT	8		Brightness adjustment	10.7.2.
RBRT	7		R sub-brightness adjustment	10.7.2.
GBRT	7		G sub-brightness adjustment	10.7.2.
BBRT	7		B sub-brightness adjustment	10.7.2.
CALDAC	8		Manual luminance adjustment	10.6.
H_ACT_U	8		Timing setting register (setting value separately submitted)	10.3.
H_ACT_D	11		Timing setting register (setting value separately submitted)	10.3.
V_ACT_U	8		Timing setting register (setting value separately submitted)	10.3.
V_ACT_D	10		Timing setting register (setting value separately submitted)	10.3.
DE_U	10		Timing setting register (setting value separately submitted)	10.3.
DE_D	10		Timing setting register (setting value separately submitted)	10.3.
WSST1_U	10		Timing setting register (setting value separately submitted)	10.3.
WSST1_D	10		Timing setting register (setting value separately submitted)	10.3.
WSST2_U	10		Timing setting register (setting value separately submitted)	10.3.
WSST2_D	10		Timing setting register (setting value separately submitted)	10.3.
WSEN1_U	9		Timing setting register (setting value separately submitted)	10.3.
WSEN1_W	8		Timing setting register (setting value separately submitted)	10.3.
WSEN2_U	10		Timing setting register (setting value separately submitted)	10.3.
WSEN2_W	8		Timing setting register (setting value separately submitted)	10.3.
WSEN3_U	8		Timing setting register (setting value separately submitted)	10.3.
WSEN3_W	8		Timing setting register (setting value separately submitted)	10.3.
DESN_U	9		Timing setting register (setting value separately submitted)	10.3.
DSEN_W	10		Timing setting register (setting value separately submitted)	10.3.
VCK_U	8		Timing setting register (setting value separately submitted)	10.3.
VCK_W	8		Timing setting register (setting value separately submitted)	10.3.
SIGSELREF_U	8		Timing setting register (setting value separately submitted)	10.3.
SIGSELREF_W	8		Timing setting register (setting value separately submitted)	10.3.
SIGSELOFS_U	4		Timing setting register (setting value separately submitted)	10.3.
SIGSELOFS_W	8		Timing setting register (setting value separately submitted)	10.3.
SIGSEL_W	8		Timing setting register (setting value separately submitted)	10.3.
SELREF_U	8		Timing setting register (setting value separately submitted)	10.3.

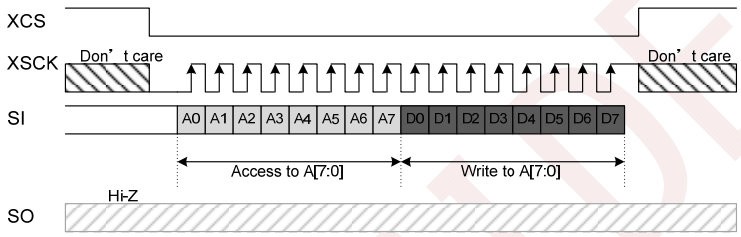
Register name	Bits	V sync	Function	Related Items
SELREF_W	8		Timing setting register (setting value separately submitted)	10.3.
SELOFS_U	8		Timing setting register (setting value separately submitted)	10.3.
SELOFS_W	8		Timing setting register (setting value separately submitted)	10.3.
SEL_U	8		Timing setting register (setting value separately submitted)	10.3.
SEL_W	8		Timing setting register (setting value separately submitted)	10.3.
AZEN_U	9		Timing setting register (setting value separately submitted)	10.3.
ZAEN_D	10		Timing setting register (setting value separately submitted)	10.3.
RD_ON	1		Register read on / off	10.1.4.
RD_ADDR	8		Register read address setting	10.1.4.

10.1.3. Serial I/F Write Access

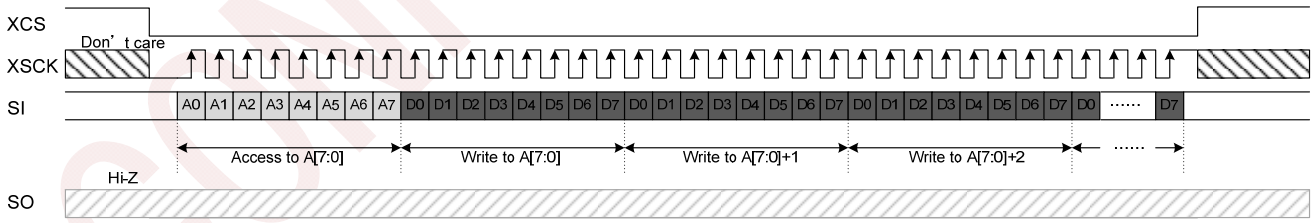
Serial communication of normal / burst transfer, LSB first is supported for write operation.

Input the address of the objective register from SI pin (#43), then input the data to the address.

The timing of write access is shown below.



Write Access Normal Transfer (LSB First)



Write Access Burst Transfer (LSB First)

10.1.4. Serial I/F Read Access

Serial communication of normal / burst transfer, LSB first is supported for read operation.

◆Register Settings

Address	Register name	Bits	Function
0x80h	RD_ON	1	Register read on / off 0: Off (default) 1: On

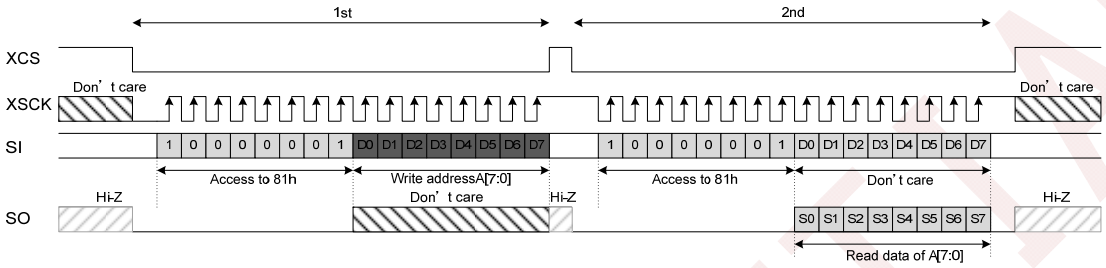
0x81h	RD_ADDR	8	Register read address setting

Set RD_ON to 1, and then perform 2 times serial communication.

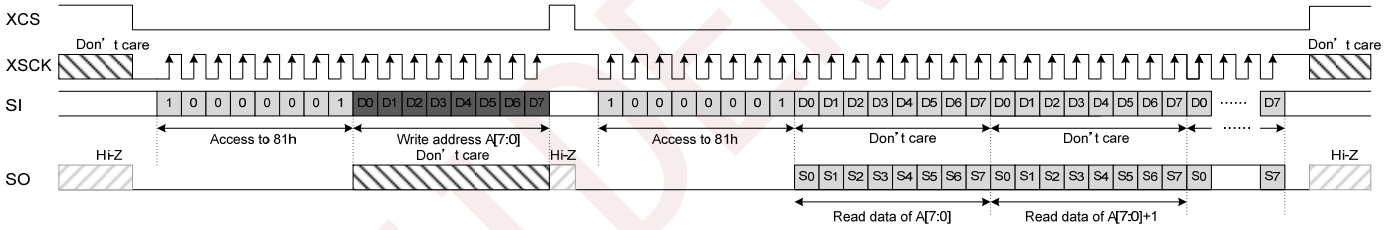
1st: Write the address of the objective register to RD_ADDR.

2nd: Read the data of the objective register from SO pin (#44) after accessing to the RD_ADDR.

The timing of read access is shown below.



Read Access Normal Transfer(LSB First)



Read Access Burst Transfer (LSB First)

10.2. Video Signal Transfer Format

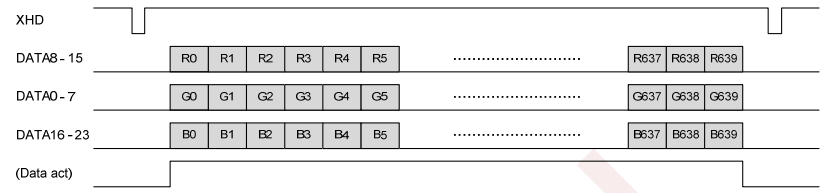
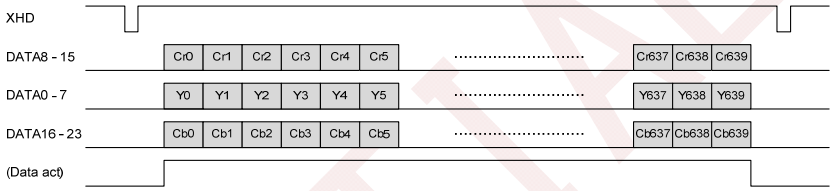
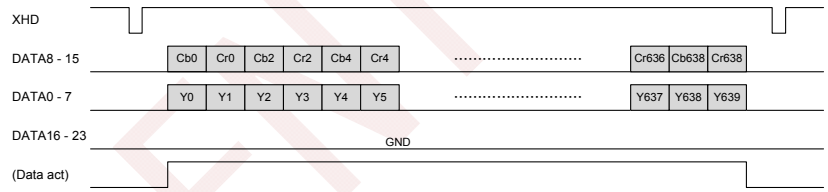
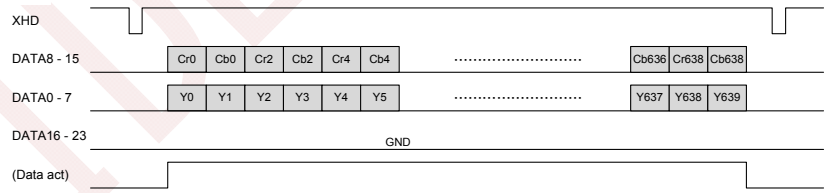
Set the registers appropriately for the video signal transfer format according to the table below.

◆Register Settings

Address	Register name	Bits	Function
0x00h	RGB_YCB	1	Selection of RGB / YCbCr (YPbPr) format 0: RGB (default) 1: YCbCr and YPbPr
0x00h	YCB_DEC	1	Selection of YCbCr / YPbPr conversion 0: YCbCr (BT. 601) (default) 1: YPbPr (BT. 709)
0x01h	FORMAT_SEL_DATA	2	Selection of YCbCr (YPbPr) input format 00: 24bit 4:4:4 input (default) 01: 16bit 4:2:2 input
0x01h	YCB_P	1	Selection of YCbCr (YPbPr) input pattern 0: Cb and Pb first (default) 1: Cr and Pr first

◆Register settings for each video signal transfer formats when YCB_DEC=0.

*Cb and Cr are replaced by Pb and Pr respectively when YCB_DEC=1.

Register settings			Video signal transfer format
RGB_YCB	FORMAT_SEL_DATA	YCB_P	
0	—	—	
1	00	—	
1	01	0	
		1	

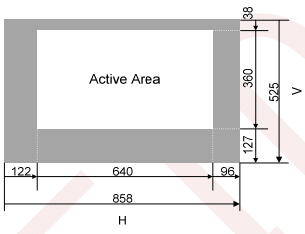
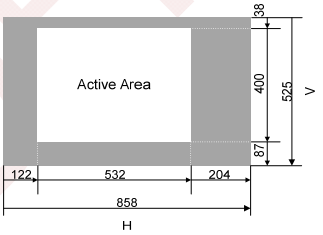
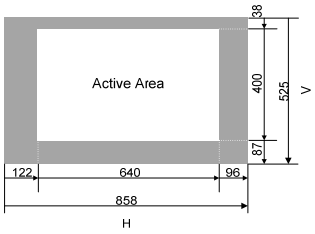
10.3. Input Signal Data Format

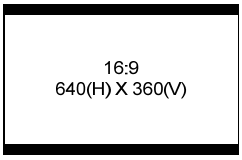
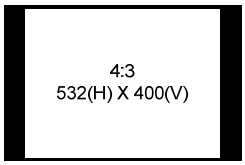
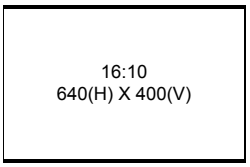
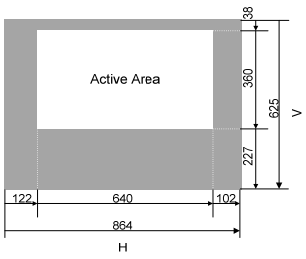
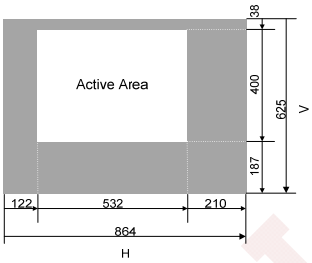
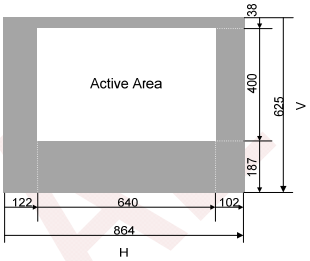
Set the panel timing registers appropriately for the input signal data format.

◆Register Settings

Address	Register name	Bits	Function
0x01h	FORMAT_SEL_H	2	Selection of input format (number of horizontal active pixels) 00: 640 (default) 10: 532
0x01h	FORMAT_SEL_V	2	Selection of input format (number of vertical active pixels) 00: 400 (default) 11: 360
0x2Dh | 0x66h	H_ACT_U | AZEN_D		Timing setting registers. Should be set appropriately for the input signal data format. Setting values are separately presented.

◆Panel Display Modes and Input Supported Formats

Panel Display Mode		①16:9 59.94Hz / 60Hz Frame Rate	②4:3 59.94Hz / 60Hz Frame Rate	③16:10 59.94Hz / 60Hz Frame Rate
		16:9 640(H) X 360(V)	4:3 532(H) X 400(V)	16:10 640(H) X 400(V)
Input Supported Format				
Active	H	640	532	640
	V	360	400	400
Total	H	858	858	858
	V	525	525	525
FP	H	96	204	96
	V	127	87	87
SYNC	H	64	64	64
	V	6	6	6
BP	H	58	58	58
	V	32	32	32
BP+SYNC	H	122	122	122
	V	38	38	38
fv	Hz	59.94 / 60	59.94 / 60	59.94 / 60
Th	µs	31.778 / 31.746	31.778 / 31.746	31.778 / 31.746
Clock	MHz	26.999 / 27.027	26.999 / 27.027	26.999 / 27.027

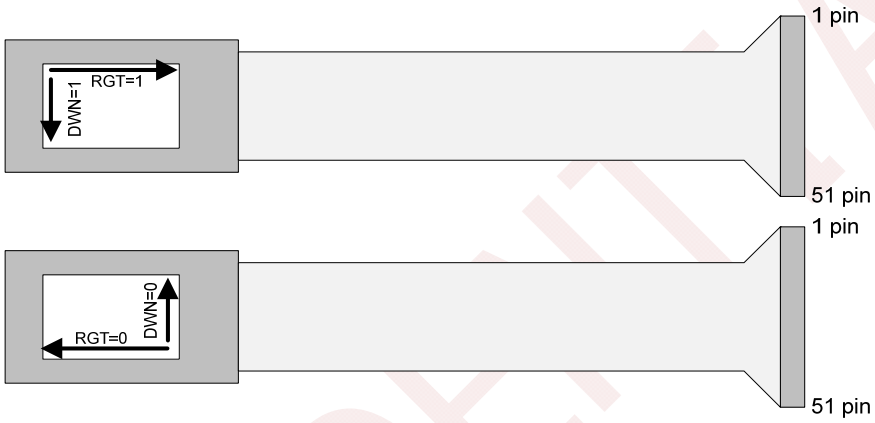
Panel Display Mode		④16:9 50Hz Frame Rate 	⑤4:3 50Hz Frame Rate 	⑥16:10 50Hz Frame Rate 
Input Supported Format				
Active	H	640	532	640
	V	360	400	400
Total	H	864	864	864
	V	625	625	625
FP	H	102	210	102
	V	227	187	187
SYNC	H	64	64	64
	V	6	6	6
BP	H	58	58	58
	V	32	32	32
BP+SYNC	H	122	122	122
	V	38	38	38
fv	Hz	50	50	50
Th	µs	32.000	32.000	32.000
Clock	MHz	27.000	27.000	27.000

10.4. Up/down and/or Right/left Inversion Function

Up/down and/or right/left inverse display of the panel are set by the registers RGT and DWN, respectively.

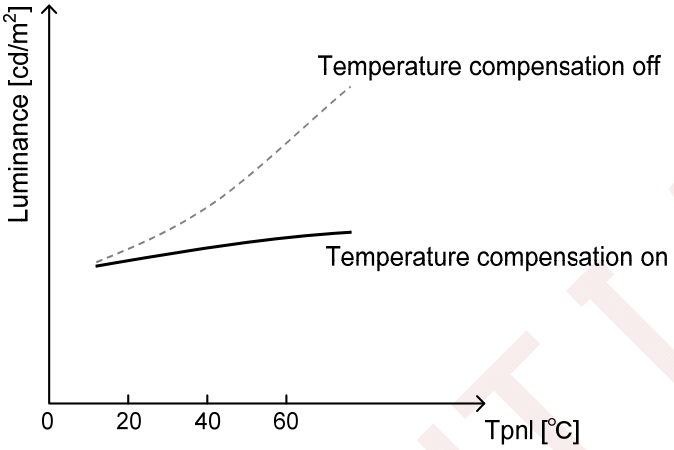
◆Register Settings

Address	Register name	Bits	Function
0x00h	RGT	1	Selection of rightward / leftward scan 0: Leftward scan 1: Rightward scan
0x00h	DWN	1	Selection of upward / downward scan 0: Upward scan 1: Downward scan



10.5. Luminance Temperature Compensation Function

In general, luminance of OLED depends on display panel temperature as show in below. This module integrates luminance compensation function against panel temperature variation. This function allows to sustain relatively constant luminance even if panel temperature changing as shown in below.



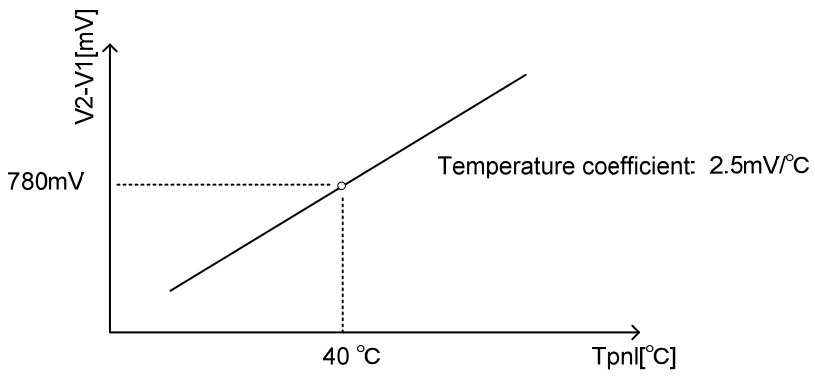
◆Register Settings

Address	Register name	Bits	Function
0x01h	VCAL_MON	1	Temperature sensor monitoring 0: Invalid (Default) 1: Valid
0x02h	CALSEL[1:0]	2	VCAL output selection 01: V1 output 10: V2 output

◆Method of Checking the Panel Temperature

The temperature sensor output voltage can be output from VCAL pin (#3).

Set the register VCAL_MON to 1: valid, set the register CALSEL as noted above, and read the V1 and V2 outputs. The temperature can be calculated by subtracting V1 from V2.



10.6. Luminance Adjustment Function

This function adjusts the VG255 voltage according to the register CALDAC setting to adjust the luminance.

◆Register Settings

Address	Register name	Bits	Function
0×2Ah	CALDAC[7:0]	8	Luminance adjustment setting value: 1 to 255 (in decimal notation) Default :128

10.7. White Balance Adjustment Function

10.7.1. Contrast/Sub-contrast

This function sets the contrast (gain) of the input signal. RGB simultaneous adjustment and R, G and B separate adjustment can be set.

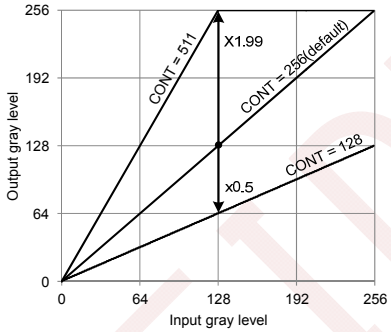
◆ Register Settings

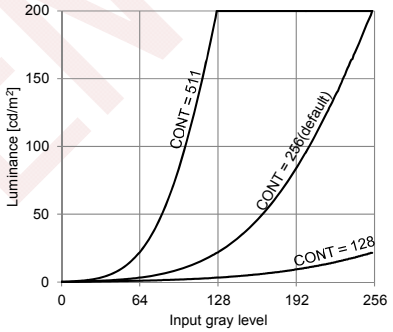
Address	Register name	Number of bits	Function
0x20h, 0x21h	CONT	9	To RGB input signal, × 0 ... × 1 (Default) ... × 1.99
0x22h	RCONT	7	Sets R relative to CONT to × 0.75 ... × 1 (Default) ... × 1.24
0x23h	GCONT	7	Sets G relative to CONT to × 0.75 ... × 1 (Default) ... × 1.24
0x24h	BCONT	7	Sets B relative to CONT to ×0.75 ... × 1 (Default) ... ×1.24

◆Contrast Adjustment (RGB Simultaneous Adjustment)

R, G and B output signal are adjusted simultaneously corresponding to the input signal using the register “CONT”. Setting value is 0 to 511 (decimal notation). Output gray level can be adjusted based on table in below.

CONT setting value	0	…	128	…	256 (Default)	…	384	…	511
Gain (to input)	× 0	…	× 0.5	…	× 1	…	× 1.5	…	× 1.99

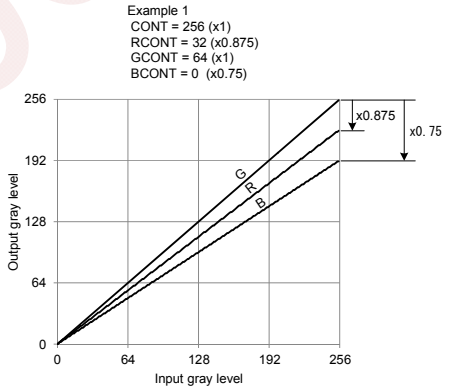


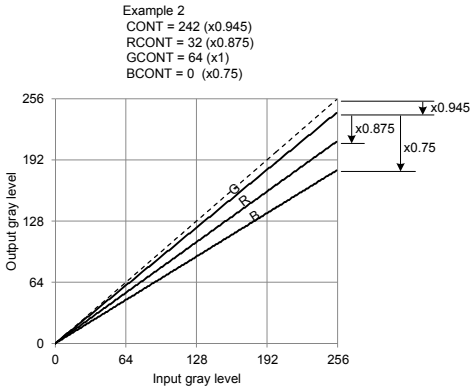


◆Sub Contrast Adjustment (RGB independent adjustment)

R, G and B output signal are adjusted separately using RCONT, GCONT and BCONT registers respectively, besides the register “CONT” The R, G and B output signal depends on both “RCONT, GCONT, BCONT” and “CONT”, as shown in examples in below. Gain for output and input is determined with multiple of “RCONT or GCONT or BCONT” and “CONT”. The “RCONT, GCONT, BCONT” setting range is 0 to 255 (decimal notation).

R/G/BCONT setting value	0	…	32	…	64 (Default)	…	96	…	127
Gain (to CONT)	× 0.75	…	× 0.875	…	× 1	…	× 1.125	…	× 1.24





10.7.2. Bright/Sub Bright

This sets the brightness level of the input signal. RGB simultaneous adjustment and R, G and B separate adjustment can be set.

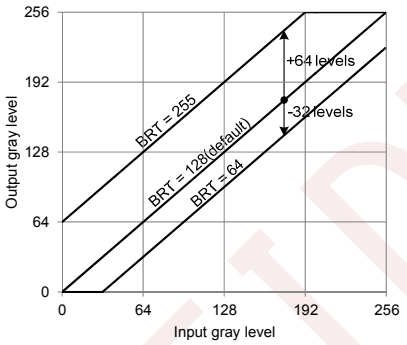
◆Register Settings

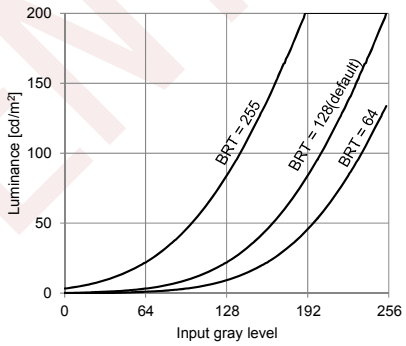
Address	Register name	Number of bits	Function
0x25h	BRT	8	To RGB input signal, -64 ... 0 (Default) ... +63 gradations
0x26h	RBRT	7	Sets R relative to BRT to-32 ... 0 (Default) ... +31 gradations
0x27h	GBRT	7	Sets G relative to BRT to-32 ... 0 (Default) ... +31 gradations
0x28h	BBRT	7	Sets B relative to BRT to-32 ... 0 (Default) ... +31 gradations

◆Brightness Adjustment (RGB simultaneous Adjustment)

R, G and B of input signal can be adjusted simultaneously using register BRT. The setting value is 0 to 255 (decimal notation).

BRT setting value	0	…	64	…	128(Default)	…	192	…	255
Output gradations (to input)	-64	…	-32	…	0	…	+32	…	+63



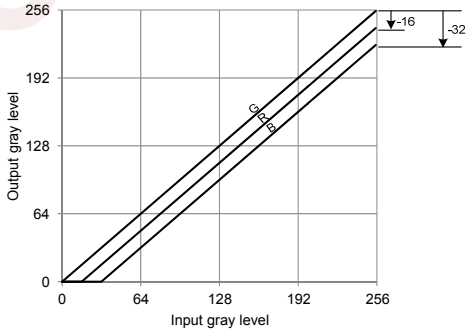


◆Sub Brightness Adjustment (RGB independent adjustment)

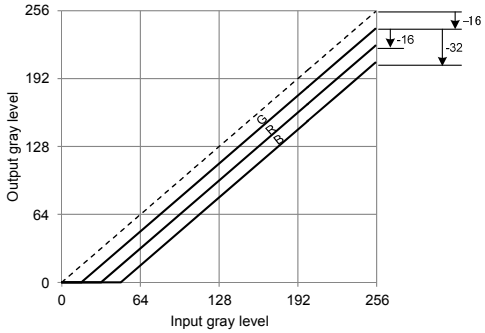
R, G and B output signal are adjusted separately using registers “RBRT, GBRT and BBRT” respectively, besides the register “BRT” The R, G and B output signal depends on both “RBRT, GBRT, BBRT” and “BRT”, as shown in example in below. Offset between output and input is determined with sum of “RBRT or GBRT or BBRT” and “BRT”. The “RBRT, GBRT, BBRT” setting range is 0 to 255 (decimal notation).

R/G/BBRT setting value	0	…	32	…	64(Default)	…	96	…	127
Output gradations (to BRT)	-32	…	-16	…	0	…	+16	…	+31

Example 3
BRT = 128 (0)
RBRT = 32 (-16 levels)
GBRT = 64 (0)
BBRT = 0 (-32 levels)



Example 4
BRT = 96 (-16 levels)
RBRT = 32 (-16 levels)
GBRT = 64 (0)
BBRT = 0 (-32 levels)



10.8. Luminance and White Balance Preset Mode

This product has 5 luminance and white balance preset modes.

By selecting the mode according to the register LUMINNACE, the luminance and the white chromaticity are adjusted to preset value.

◆Register Settings

Address	Register name	Bits	Function
0x08h	OTPCALDAC_REGDIS	1	Luminance adjustment 0: Preset mode valid (default) 1: Preset mode invalid (CALDAC adjustment)
0x08h	OTPDG_REGDIS	1	White chromaticity adjustment 0: Preset mode valid (default) 1: Preset mode invalid (CONT/BRT adjustment)
0x05h	LUMINANCE[2:0]	3	Luminance and white chromaticity preset mode selection 1: 300cd/m^2, (0.31,0.32) 2: 500cd/m^2, (0.31,0.32) 0: 800cd/m^2, (0.31,0.32) 3: 1500cd/m^2, (0.31,0.32) 4: 2000cd/m^2, (0.31,0.32)

10.9. Dithering Function

This function expresses quasi-gradations between original gradations based on FRC (Frame Rate Control) technology This function can compensate the loss of the number of gray level due to gray level sacrifice for contrast and brightness adjustment. In terms of the gray level sacrifice, please refer “10.7 White Balance Adjustment Function” and “10.8 Luminance and White Balance Preset Mode”.

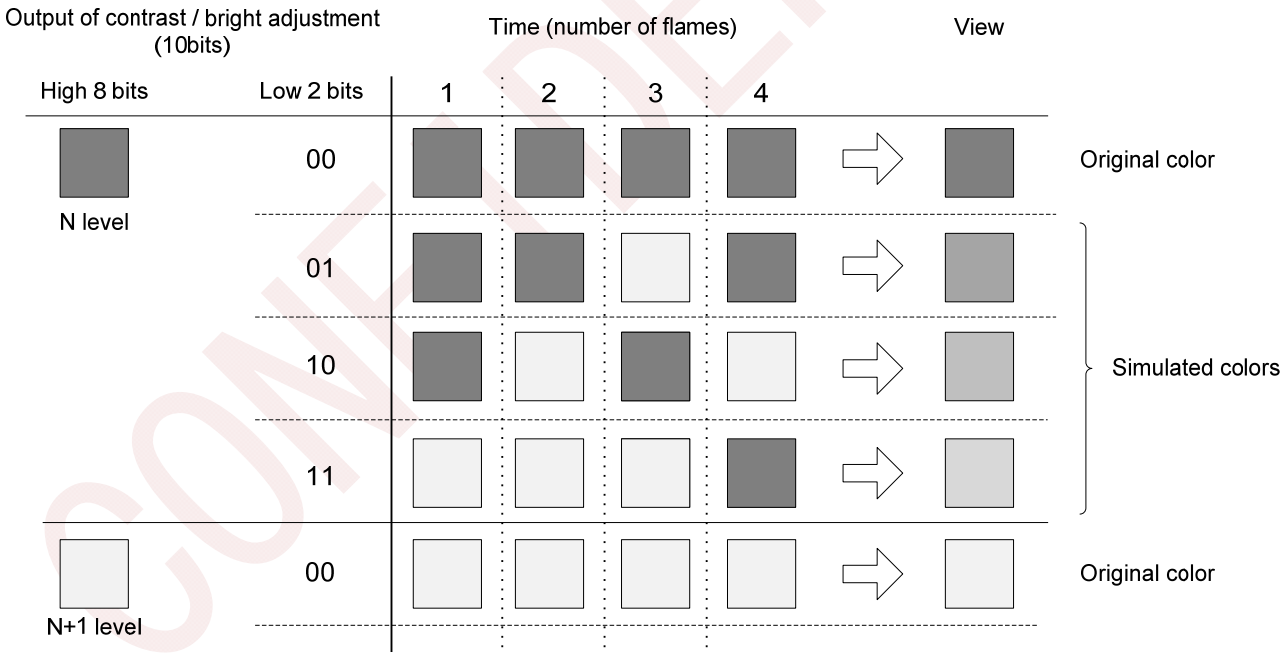
◆Register Settings

Address	Register name	Bits	Function
0x05h	DITHERON	1	Dithering processing on / off 0: Off (default) 1: On

10.9.1. FRC (Frame Rate Control)

This function based on FRC technology. FRC can create quasi-gray levels between tangible gray levels based on time-resolution operation. Human eyes can percept brightness as average of time-wise in case displaying different brightness image under enough fast frame rate, as shown in below figure. The figure in below is case of 2bit FRC. When two gray levels are switching alternately in high-speed, human eyes can effectively percept average brightness of those two brightness levels as quasi-gray level. The quasi-gray level can be added besides original colors by changing data in 4-frame cycle making use of this property (2 bit FRC).

Quasi-gray level creation of 2bit FRC is shown in below, with assumption of one pixel.

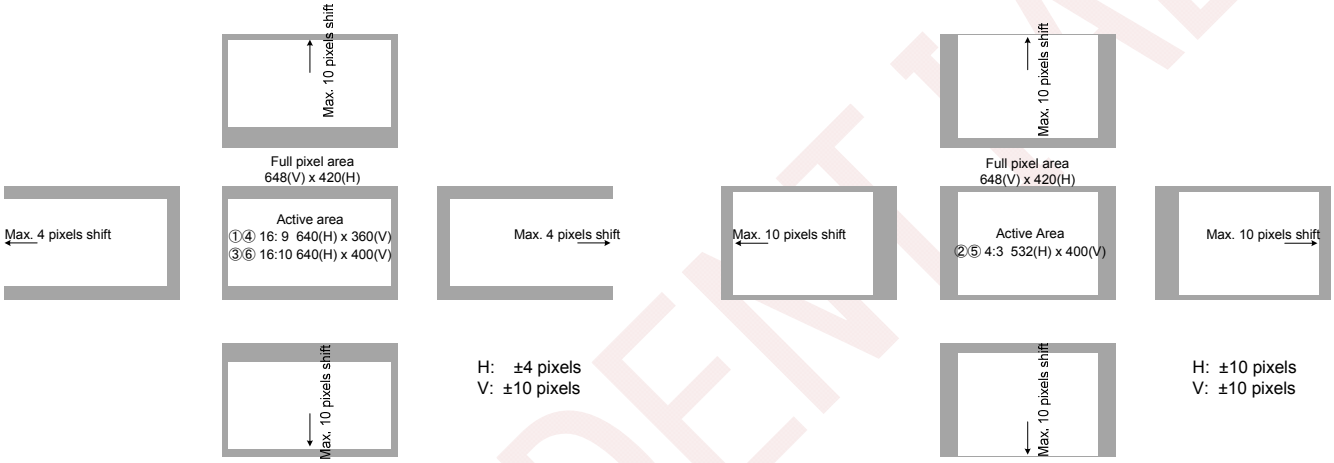


10.10. Orbit Function

The image data start position can be changed. This enables reducing of the noticeability of local drops in luminance.

◆Register Settings

Address	Register name	Bits	Function
0x02h	ORBIT_H[4:0]	5	Horizontal orbit adjustment -10 to 0 to +10, (-4 to 0 to +4 when horizontal active 640 pixels) Default: 0
0x03h	ORBIT_V[4:0]	5	Vertical orbit adjustment -10 to 0 to +10, Default: 0



10.10.1. Horizontal Display Position Shift

The display start position is changed by the register ORBIT_H. The variable range is ± 10 pixels (±4 pixels when horizontal active is 640 pixels).

ORBIT_H setting value	-10	…	-1	0 (Default)	1	…	10
Number of pixels shifted	Leftward 10-pixel	…	Leftward 1-pixel	Center	Rightward 1-pixel	…	Rightward 10-pixel

10.10.2. Vertical Display Position Shift

The display start position is changed by the register ORBIT_V. The variable range is ± 10 pixels.

ORBIT_V setting value	-10	…	-1	0 (Default)	1	…	10
Number of pixels shifted	Upward 10-pixels	…	Upward 1-pixel	Center	Downward 1-pixel	…	Downward 10-pixel

11. Optical Characteristics

11.1. Optical Characteristics

Item		Symbol	Measurement Method	Min.	Typ.	Max.	Unit
Luminance	Mode 1	L1	1	240	300	360	cd/m^2
	Mode 2	L2	1	425	500	575	cd/m^2
	Mode 0	L0	1	680	800	920	cd/m^2
	Mode 3	L3	1	1275	1500	1725	cd/m^2
	Mode 4	L4	1	1600	2000	2400	cd/m^2
Contrast		CR	1	10,000	—	—	
Chromaticity	W (L0,L2 & L3)	x	1	0.298	0.310	0.322	CIE
		y	1	0.308	0.320	0.332	CIE
	W (L1 & L4)	x	1	0.290	0.310	0.330	CIE
		y	1	0.300	0.320	0.340	CIE
	R	x	1	0.630	0.650	0.670	CIE
		y	1	0.310	0.330	0.350	CIE
	G	x	1	0.240	0.260	0.280	CIE
		y	1	0.520	0.540	0.560	CIE
	B	x	1	0.130	0.150	0.170	CIE
		y	1	0.050	0.070	0.090	CIE

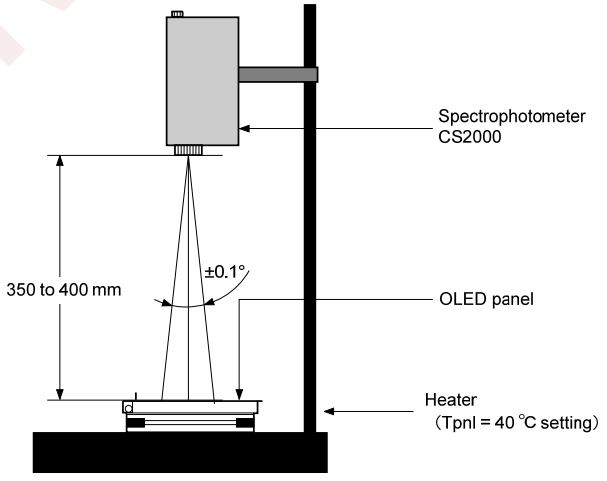
Drive conditions:
OTPDG_REGDIS=0、OTPCALDAC_REGDIS=0,
LUMINANCE=1(Mode1), 2 (Mode 2), 0 (Mode 0), 3 (Mode 3) , 4(Mode4)

11.2. Measurement System・Measurement Method 1

The luminance and chromaticity are measured in Measurement System A shown below.

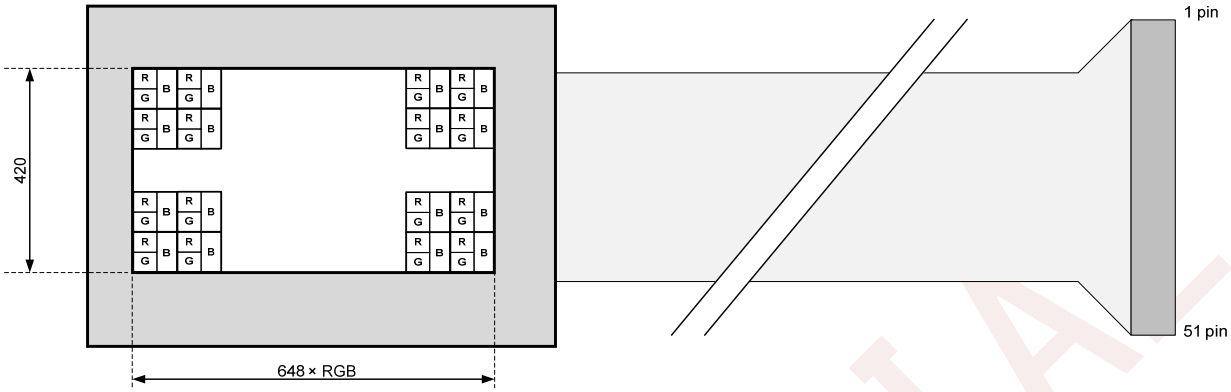
Measurement temperature: Tpnl = 40°C
Measurement point: One point on the screen center
All white display: All RGB signal data is set to High.
All black display: All RGB signal data is set to Low.

Luminance and chromaticity: Measure the luminance and chromaticity in all white display in Measurement System A.
Contrast: Measure the luminance in all white display (@ Mode0: 800cd/m^2) and all black display in Measurement System A, and substitute them into the formula below.
Contrast = Luminance in all white display/Luminance in all black display



System A

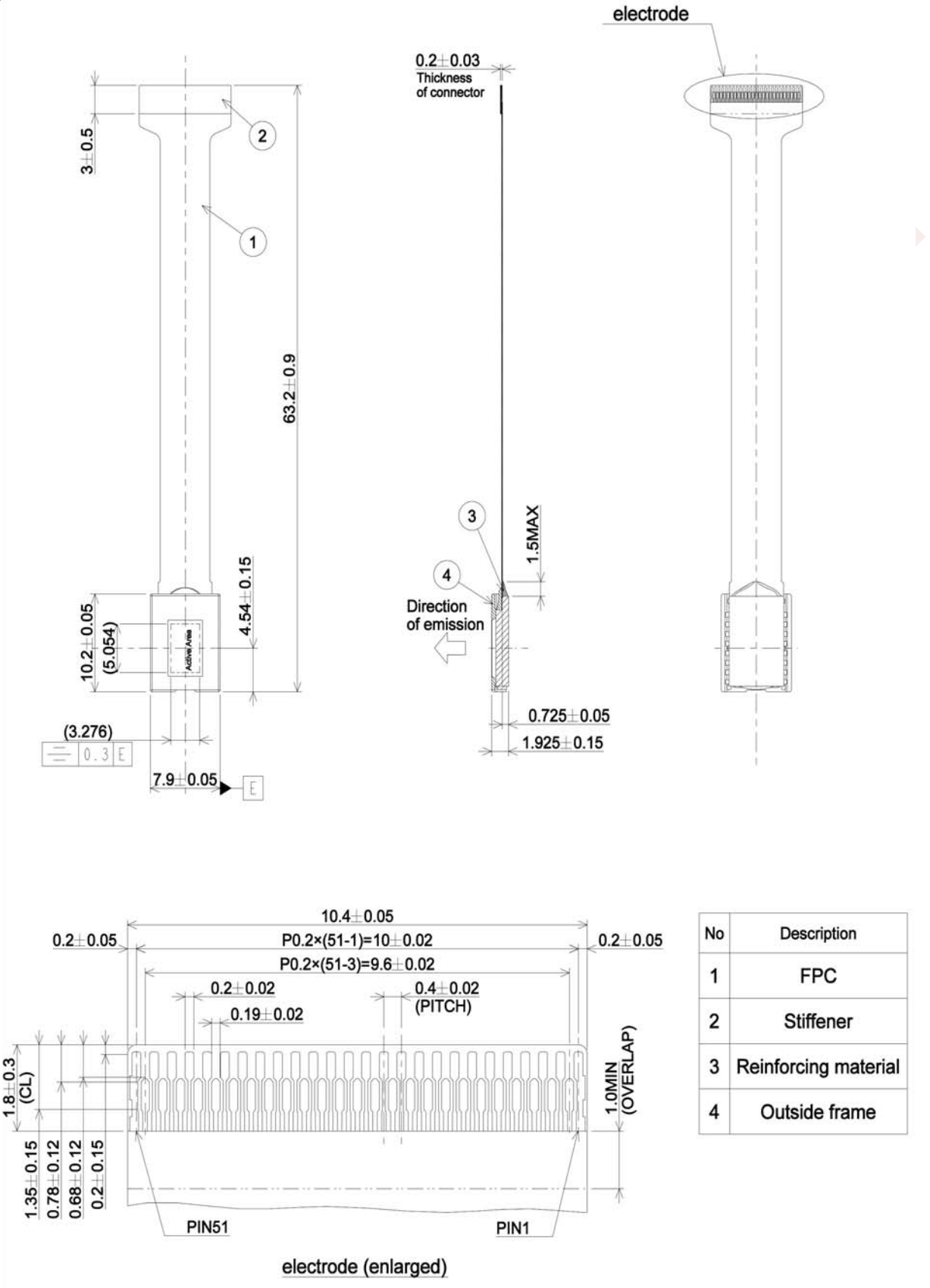
12. Pixel Alignment



※Including orbit margin

13.Package Outline (Nagasaki 200mm wafer)

(Unit: mm)

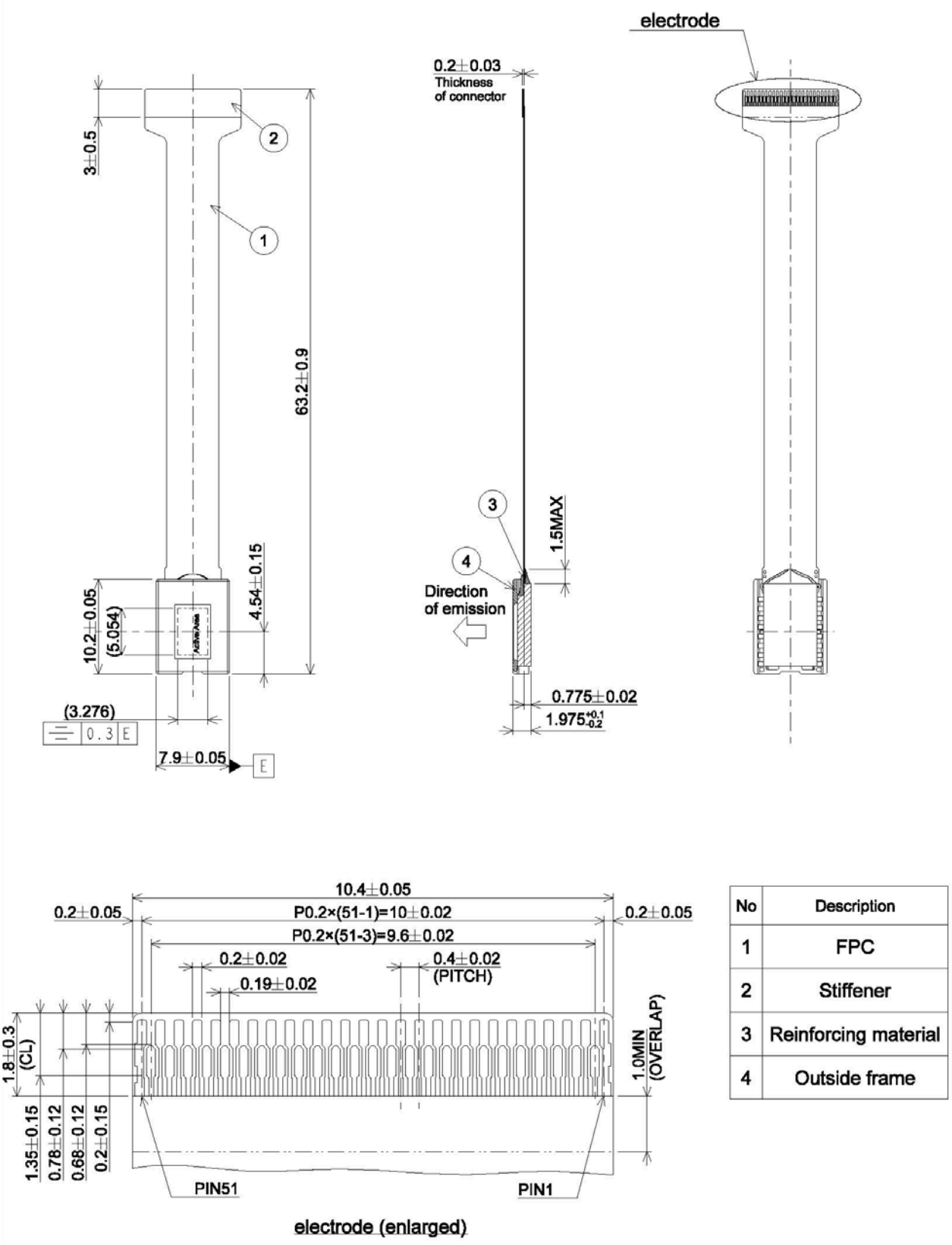


No	Description
1	FPC
2	Stiffener
3	Reinforcing material
4	Outside frame

Package Outline (Kumamoto 300mm wafer)

Tentative

(Unit: mm)



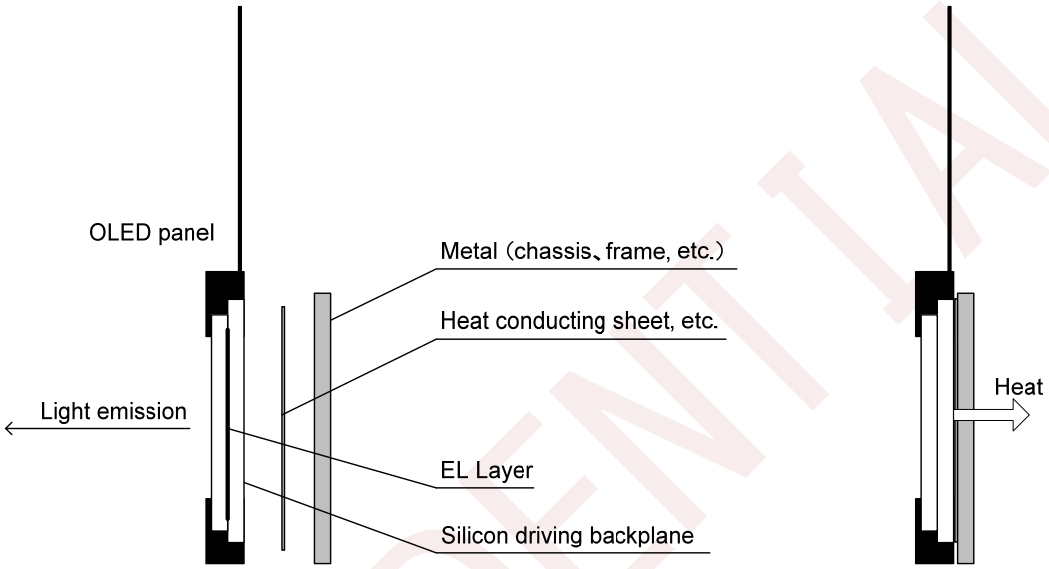
No	Description
1	FPC
2	Stiffener
3	Reinforcing material
4	Outside frame

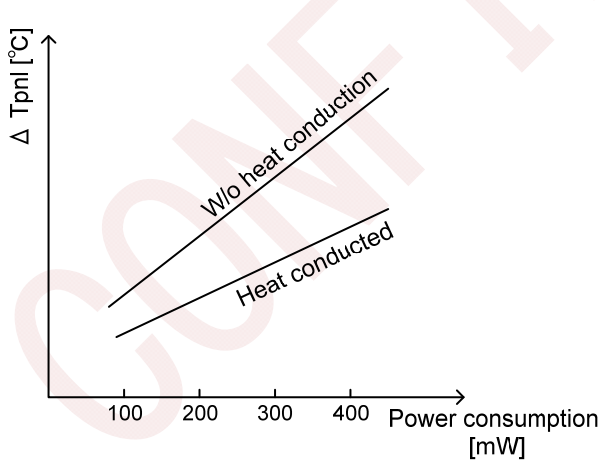
14. Recommended Items

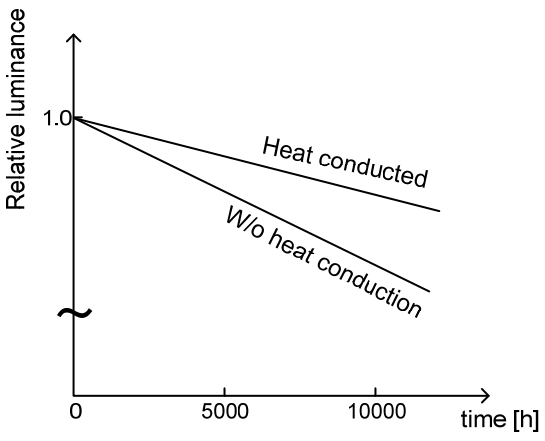
14.1. Suppression of the Panel Temperature

Temperature of organic EL panel tends to rise due to power consumption (heat generation) by the EL emissive layer and the integrated silicon drive circuits. The temperature rise may cause luminance drop over time.

The temperature rise in panel can be suppressed by establishing a thermal connection between panel rear surface (silicon substrate surface) and metal (chassis, frame, etc.) at panel mount area So, highly recommend the heat conductive sheet between them as show in below.







15. Notes on Handling

15.1. Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves or handle with bare hands.

(2) Use a wrist strap connecting ground when handling.

(3) Do not touch any electrodes on the panel.

(4) Wear non-chargeable clothes and conductive shoes.

(5) Install grounded conductive mats on the working floor and working table.

(6) Keep the panel away from any charged materials.

15.2. Protection from dust and dirt

(7) Operate in a clean environment.

(8) Do not touch the panel surface. The surface is easily scratched.
When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.

(9) Use ionized air to blow dust off the panel surface.

15.3. Others

(10) Not hold FPC (Flexible Printed Circuit) , not twist the FPC, not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.

(11) The minimum fold radius of the FPC is 1.0 mm, So, do not fold the FPC less than 1.0mm radius.

(12) Do not drop the module.

(13) Do not twist or bend the module .

(14) Keep the module away from heat sources.

(15) Not be close the module to water or other solvents.

(16) Do not store or use the module at high temperatures or high humidity circumstance,
as the circumstance may affect module specifications. .

(17) When disposing of this, regard it as industrial waste and please comply with related regulations.

(18) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications. .

This module is supposed to be delivered in a degassed aluminum laminated bag.
When storing this panel again after once unsealing the bag, please take following action. Put it into the aluminum laminated bag again.. Put in desiccant into the aluminum bag and the opening of the aluminum bag should be folded and seal the bag with tape.

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.