

DM-LCD2004-445
2004 STN(-) Y/G CHARACTER LCD
WITH PARALLEL MPU INTERFACE

Contents

[Revision History](#)

[Main Features](#)

[Pin Description](#)

[Mechanical Drawing](#)

[Electrical Characteristics](#)

[Optical Characteristics](#)

[Block Diagram](#)

[Timing Character](#)

[Write data from MPU to ST7066U](#)

[Reading data from ST7066U to MPU](#)

[Instruction Table](#)

[Instruction Description](#)

[Initializing by Instruction](#)

[Built-in Font Table](#)

[Driver/Controller Information](#)

[Reliability](#)

[Warranty and Conditions](#)

1 Revision History

| Date | Changes |
|------------|---------------|
| 2015-04-15 | First release |

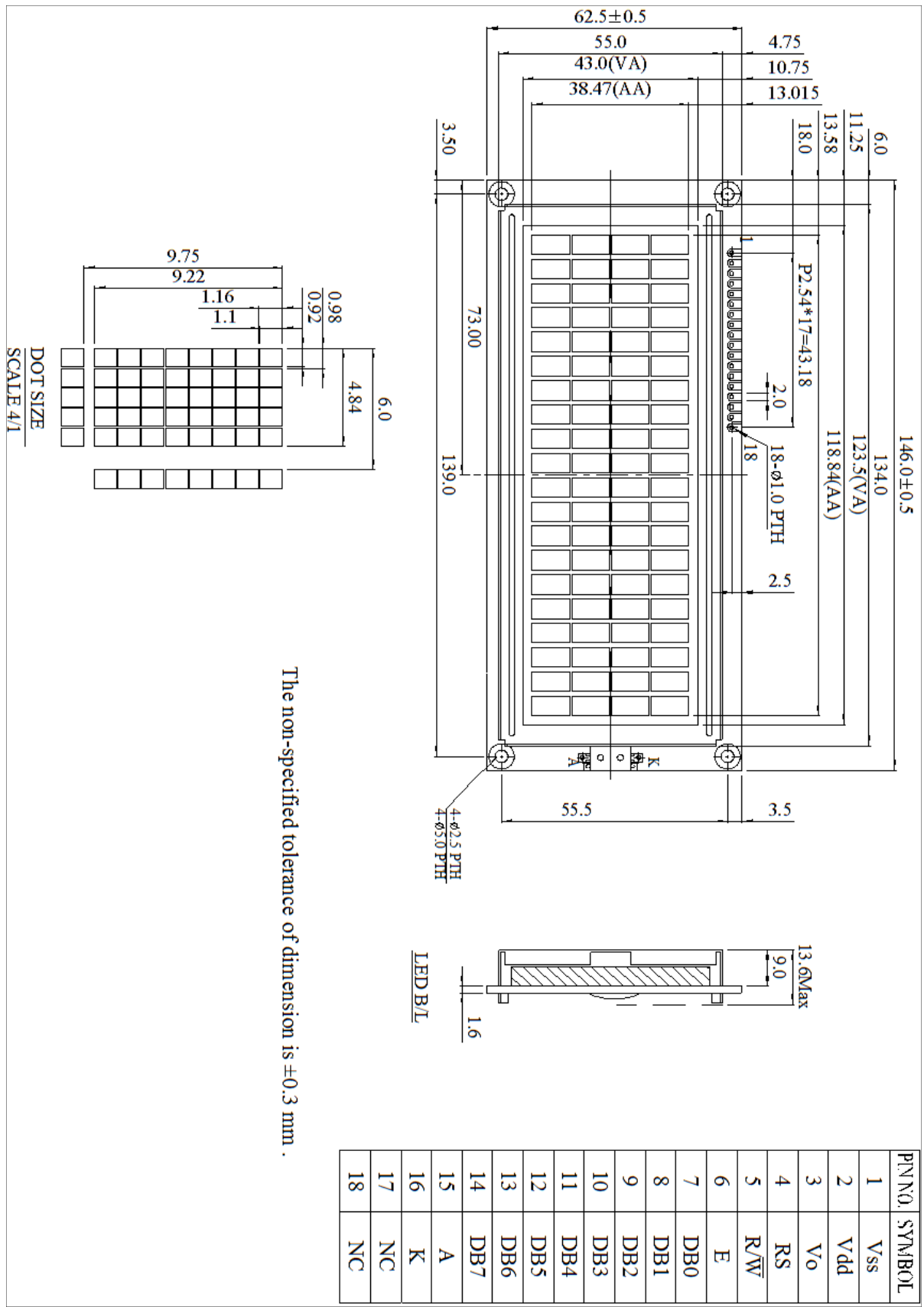
2 Main Features

| Item | Specification | Unit |
|----------------------|--|------|
| Number of Characters | 20 characters x 4 lines | |
| Display Mode | STN Positive, Yellow Green, Transmissive | - |
| Module dimension | 146.0 x 62.5 x 13.6(MAX) | mm |
| Controller IC | ST7066U | - |
| Interface | 6800 Series MPU Interface | - |
| Power Supply | 5.0 | V |
| View Direction | 6:00 | - |
| Duty | 1/16 | |
| Backlight | Yellow Green LED | - |
| Weight | 116.6 | g |

3 Pin Description

| Pin No. | Symbol | Description |
|---------|--------|--|
| 1 | VSS | Ground |
| 2 | VDD | Supply Voltage for logic |
| 3 | VO | Operation voltage for (Variable) |
| 4 | RS | H: DATA, L: Instruction code |
| 5 | R/W | H: Read(MPU→Module) L: Write(MPU→Module) |
| 6 | E | Chip enable signal |
| 7 | DB0 | Data bus line |
| 8 | DB1 | Data bus line |
| 9 | DB2 | Data bus line |
| 10 | DB3 | Data bus line |
| 11 | DB4 | Data bus line |
| 12 | DB5 | Data bus line |
| 13 | DB6 | Data bus line |
| 14 | DB7 | Data bus line |
| 15 | A | Power supply for B/L(+) |
| 16 | K | Power supply for B/L(-) |
| 17 | NC | No Connection |
| 18 | NC | No Connection |

4 Mechanical Drawing



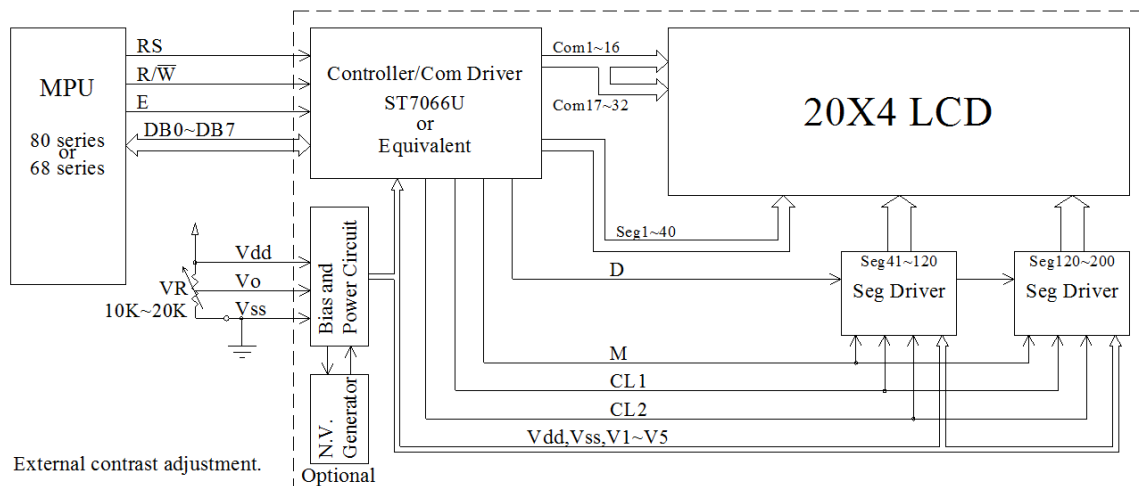
5 Electrical Characteristics

| Item | Symbol | Condition | Min | Typ. | Max | Unit |
|---------------------------|------------------|--------------|--------|------|-----|------|
| Supply Voltage For Logic | VDD | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | IDD | VDD=5.0V | 1.0 | 1.2 | 1.5 | mA |
| Low Level Input Voltage | V _{IL} | | VSS | - | 0.6 | V |
| High Level Input Voltage | V _{IH} | | 0.7VDD | - | VDD | V |
| Low Level Output Voltage | V _{OL} | | 0 | | 0.4 | V |
| High Level Output Voltage | V _{OH} | | 3.9 | | VDD | V |
| Backlight Supply Voltage | V | | 4.0 | 4.2 | 4.4 | V |
| Backlight Supply Current | I _{LED} | | 432 | 540 | 648 | mA |
| Operating Temperature | TOP | Absolute Max | -20 | - | +70 | °C |
| Storage Temperature | TST | Absolute Max | -30 | - | +80 | °C |

6 Optical Characteristics

| Item | Symbol | Min | Typ | Max | Unit | Note |
|--------------------------|---------|-----|-----|-----|-------------------|------|
| View Angles Top | AV | | 20 | | ° | |
| View Angles Bottom | AV | | 40 | | ° | |
| View Angles Left | AH | | 30 | | ° | |
| View Angles Right | AH | | 30 | | ° | |
| Response Time (25°C) | Tr + Tf | | 300 | 400 | ms | |
| Contrast Ratio | CR | | 3 | | | |
| Luminance (Without LCD) | Ly | 140 | 190 | | cd/m ² | |

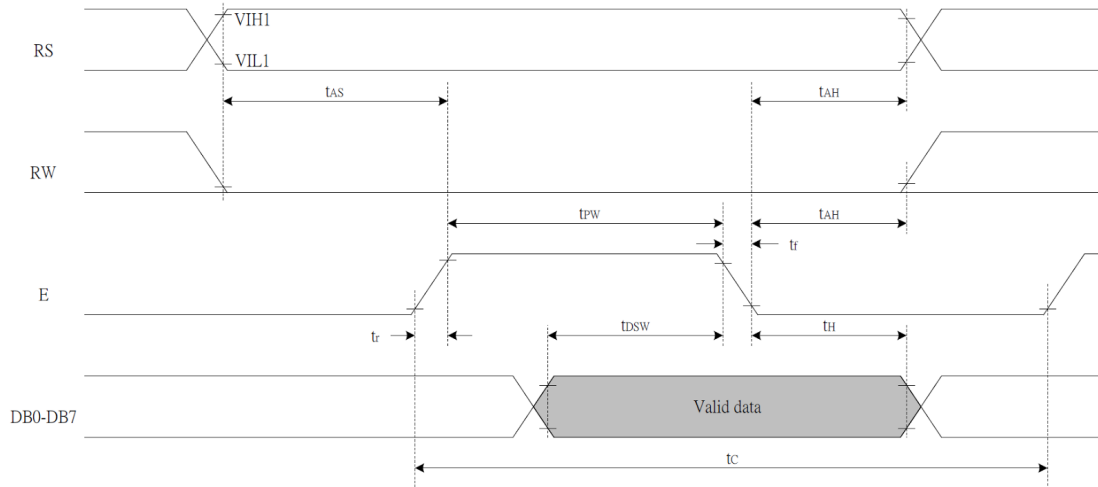
7 Block Diagram



| | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Character located | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| DDRAM address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 |
| DDRAM address | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 |
| DDRAM address | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
| DDRAM address | 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 |

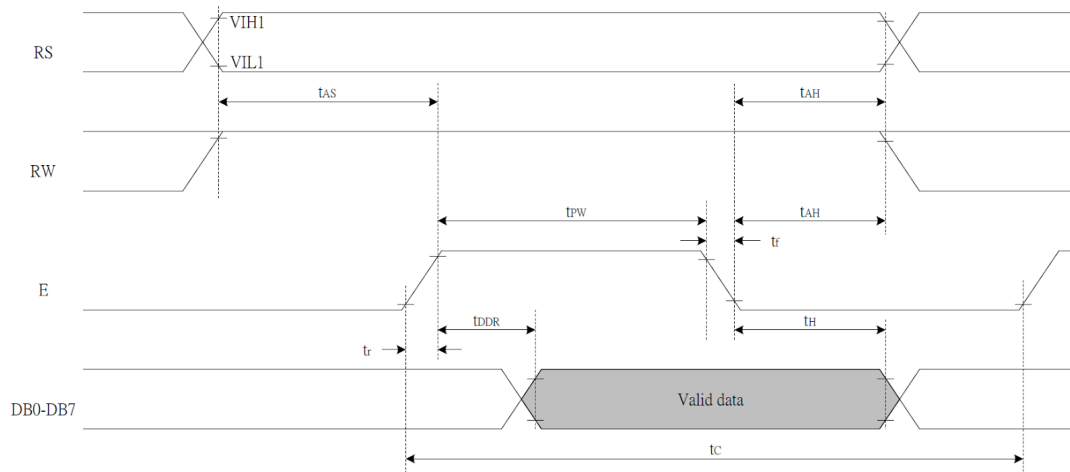
8 Timing Character

8.1 Write data from MPU to ST7066U



| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|-----------------------|------|-----|-----|------|
| T_C | Enable Cycle Time | 1200 | - | - | ns |
| T_{PW} | Enable Pulse Width | 140 | - | - | ns |
| T_{R,T_F} | Enable Rise/Fall Time | - | - | 25 | ns |
| T_{AS} | Address Setup Time | 0 | - | - | ns |
| T_{AH} | Address Hold Time | 10 | - | - | ns |
| T_{DSW} | Data Setup Time | 40 | - | - | ns |
| T_H | Data Hold Time | 10 | - | - | ns |

8.2 Reading data from ST7066U to MPU



| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|-----------------------|------|-----|-----|------|
| T_C | Enable Cycle Time | 1200 | - | - | ns |
| T_{PW} | Enable Pulse Width | 140 | - | - | ns |
| T_{R,T_F} | Enable Rise/Fall Time | - | - | 25 | ns |
| T_{AS} | Address Setup Time | 0 | - | - | ns |
| T_{AH} | Address Hold Time | 10 | - | - | ns |
| T_{DDR} | Data Setup Time | - | - | 100 | ns |
| T_H | Data Hold Time | 10 | - | - | ns |

9 Instruction Table

| Instruction | Instruction Code | | | | | | | | | | Description | Description Time (270KHz) |
|----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|------------------------------|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM, and set DDRAM address to "00H" from AC | 1.52 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.52 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 37 us |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1:entire display on C=1:cursor on B=1:cursor position on | 37 us |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | x | x | Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 37 us |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | x | x | DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8 | 37 us |
| Set CGRAM address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 37 us |
| Set DDRAM address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter | 37 us |
| Read Busy flag and address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 us |
| Write data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM) | 37 us |
| Read data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM) | 37 us |

10 Instruction Description

Clear Display

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Entry Mode Set

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Set the moving direction of cursor and display.

I/D : Increment / decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

S: Shift of entire display

When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

| S | I/D | Description |
|---|-----|--------------------------------|
| H | H | Shift the display to the left |
| H | L | Shift the display to the right |

Display ON/OFF

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit

When C = "High", cursor is turned on.

When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF control bit

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.

When B = "Low", blink is off.

Cursor or Display Shift

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

| | | | | | | | | | | |
|------|---|---|---|---|---|---|-----|-----|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | x | x |
|------|---|---|---|---|---|---|-----|-----|---|---|

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

| S/C | R/L | Description | AC Value |
|-----|-----|--|----------|
| L | L | Shift cursor to the left | AC=AC-1 |
| L | H | Shift cursor to the right | AC=AC+1 |
| H | L | Shift display to the left. Cursor follows the display shift | AC=AC |
| H | H | Shift display to the right. Cursor follows the display shift | AC=AC |

Function Set

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

| | | | | | | | | | | |
|------|---|---|---|---|---|----|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 1 | DL | N | F | x | x |
|------|---|---|---|---|---|----|---|---|---|---|

DL : Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N : Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

F : Display font type control bit

When F = "Low", it means 5 x 8 dots format display mode

When F = "High", 5 x11 dots format display mode.

| N | F | No. of Display Lines | Character Font | Duty Factor |
|---|---|----------------------|----------------|-------------|
| L | L | 1 | 5 x 8 | 1/8 |
| L | H | 1 | 5 x 11 | 1/11 |
| H | x | 2 | 5 x 8 | 1/16 |

Set CGRAM Address

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

| | | | | | | | | | | |
|------|---|---|---|---|-----|-----|-----|-----|-----|-----|
| Code | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
|------|---|---|---|---|-----|-----|-----|-----|-----|-----|

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU

Set DDRAM Address

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

| | | | | | | | | | | |
|------|---|---|---|-----|-----|-----|-----|-----|-----|-----|
| Code | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
|------|---|---|---|-----|-----|-----|-----|-----|-----|-----|

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

Read Busy Flag and Address

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

| | | | | | | | | | | |
|------|---|---|----|-----|-----|-----|-----|-----|-----|-----|
| Code | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
|------|---|---|----|-----|-----|-----|-----|-----|-----|-----|

When BF = "High", indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

Write Data to CGRAM or DDRAM

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

| | | | | | | | | | | |
|------|---|---|----|----|----|----|----|----|----|----|
| Code | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---|---|----|----|----|----|----|----|----|----|

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM

address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data from CGRAM or DDRAM

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

| | | | | | | | | | | |
|------|---|---|----|----|----|----|----|----|----|----|
| Code | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---|---|----|----|----|----|----|----|----|----|

Read binary 8-bit data from DDRAM/CGRAM.

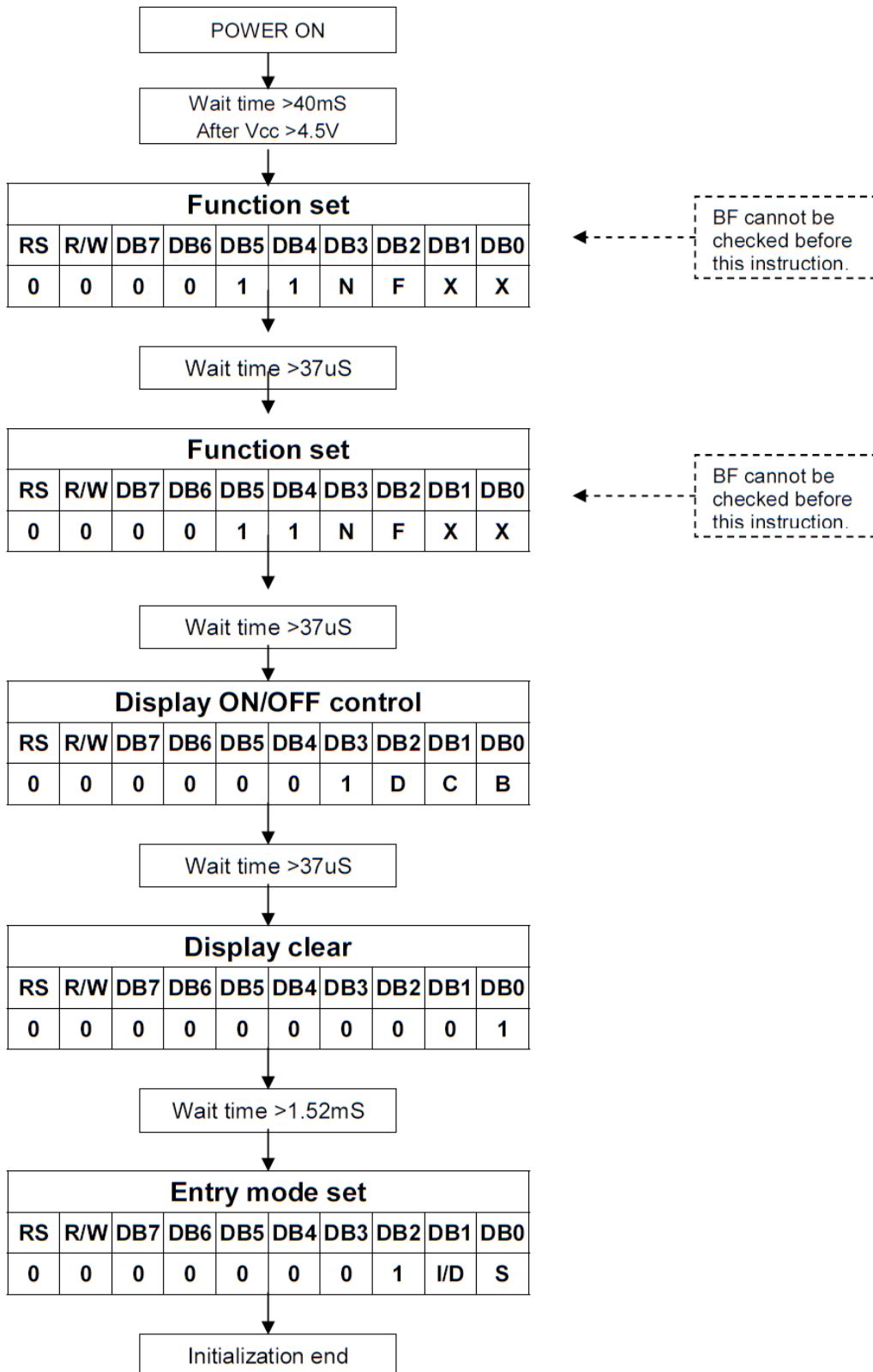
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

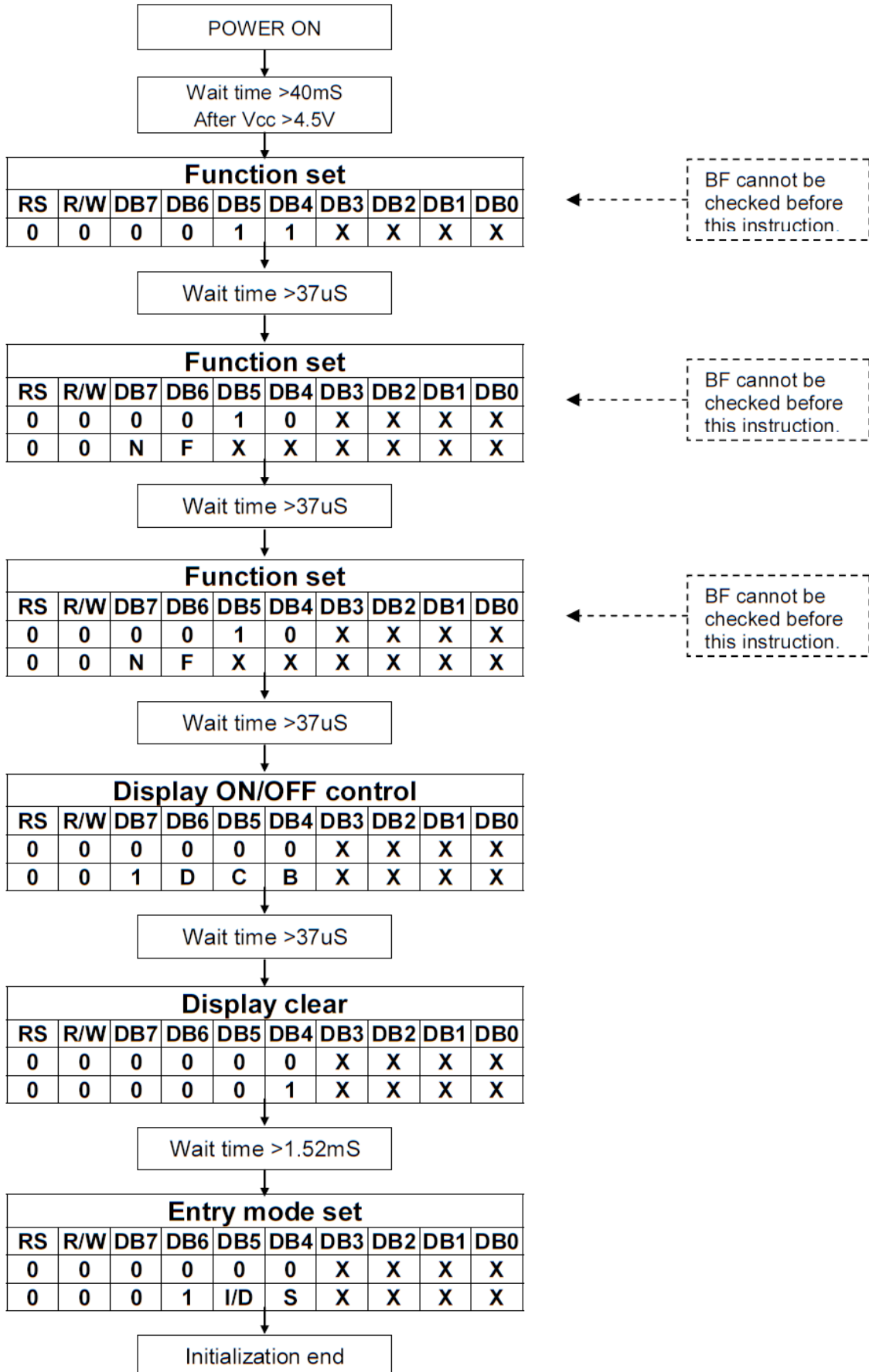
* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

11 Initializing by Instruction

8-bit Interface(focs=270KHz)



4-bit Interface (fosc=270KHz)



12 Built-in Font Table

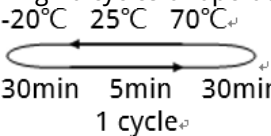
| Upper 4 bit Lower 4 bit | LLLL | LLLH | LLHL | LLHH | LHLL | LHLH | LHHL | LHHH | HLLL | HLLH | HLHL | HLHH | HHLL | HHLH | HHHL | HHHH |
|----------------------------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| LLLL | CG RAM (1) | | | 0 | 1 | 2 | 3 | 4 | | | | 5 | 6 | 7 | 8 | 9 |
| LLLH | (2) | ! | 0 | 1 | 2 | 3 | 4 | 5 | | | 6 | 7 | 8 | 9 | 0 | 1 |
| LLHL | (3) | " | 2 | 3 | 4 | 5 | 6 | 7 | | | 8 | 9 | 0 | 1 | 2 | 3 |
| LLHH | (4) | # | 3 | 4 | 5 | 6 | 7 | 8 | | | 9 | 0 | 1 | 2 | 3 | 4 |
| LHLL | (5) | \$ | 4 | 5 | 6 | 7 | 8 | 9 | | | 0 | 1 | 2 | 3 | 4 | 5 |
| LHLH | (6) | % | 5 | 6 | 7 | 8 | 9 | 0 | | | 1 | 2 | 3 | 4 | 5 | 6 |
| LHHL | (7) | & | 6 | 7 | 8 | 9 | 0 | 1 | | | 2 | 3 | 4 | 5 | 6 | 7 |
| LHHH | (8) | ' | 7 | 8 | 9 | 0 | 1 | 2 | | | 3 | 4 | 5 | 6 | 7 | 8 |
| HLLL | (1) | (| 8 | 9 | 0 | 1 | 2 | 3 | | | 4 | 5 | 6 | 7 | 8 | 9 |
| HLLH | (2) |) | 9 | 0 | 1 | 2 | 3 | 4 | | | 5 | 6 | 7 | 8 | 9 | 0 |
| HLHL | (3) | * | 0 | 1 | 2 | 3 | 4 | 5 | | | 6 | 7 | 8 | 9 | 0 | 1 |
| HLHH | (4) | + | 1 | 2 | 3 | 4 | 5 | 6 | | | 7 | 8 | 9 | 0 | 1 | 2 |
| HHLL | (5) | , | 2 | 3 | 4 | 5 | 6 | 7 | | | 8 | 9 | 0 | 1 | 2 | 3 |
| HHLH | (6) | - | 3 | 4 | 5 | 6 | 7 | 8 | | | 9 | 0 | 1 | 2 | 3 | 4 |
| HHHL | (7) | . | 4 | 5 | 6 | 7 | 8 | 9 | | | 0 | 1 | 2 | 3 | 4 | 5 |
| HHHH | (8) | / | 5 | 6 | 7 | 8 | 9 | 0 | | | 1 | 2 | 3 | 4 | 5 | 6 |

13 Driver/Controller Information

Built-in ST7066U IC

<https://drive.google.com/file/d/0B0U8oRNRy9XuN0l0WVVsRk5DR0k/view?usp=sharing>

14 Reliability

| Test Item | Content of Test | Test Condition | Note |
|---|---|--|------|
| High Temperature Storage | Endurance test applying the high storage temperature for a long time. | 80°C 200hrs | 2 |
| Low Temperature Storage | Endurance test applying the high storage temperature for a long time. | -30°C 200hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time. | 70°C 200hrs | - |
| Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time. | -20 °C 200hrs | 1 |
| High Temperature/ Humidity Operation | The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature. | 60°C,90%RH 96hrs | 1,2 |
| Thermal Shock Resistance | The sample should be allowed stand the following 10 cycles of operation.  | -20°C/70°C 10 cycles | - |
| Vibration Test | Endurance test applying the vibration during transportation and using. | Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes. | 3 |
| Static Electricity Test | Endurance test apply the electric stress to the terminal. | VS=800V, RS=1.5kΩ, CS=100pF, 1 time. | - |

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

15 Warranty and Conditions

<http://www.displaymodule.com/pages/faq>