

DM-LCD1602-430
1602 STN(+) Y/G CHARACTER LCD
WITH SPI INTERFACE

Contents

[Revision History](#)

[Main Features](#)

[Pin Description](#)

[Mechanical Drawing](#)

[Electrical Characteristics](#)

[Optical Characteristics](#)

[Block Diagram](#)

[Timing Character](#)

[Write data from MPU to IC \(Parallel 8-bit bus and 4-bit bus\)](#)

[Reading data from IC to MPU\(Parallel 8-bit bus and 4-bit bus\)](#)

[Instruction Table](#)

[Instruction Description](#)

[Initializing by Instruction](#)

[Built-in Font Table](#)

[Driver/Controller Information](#)

[Reliability](#)

[Warranty and Conditions](#)

1 Revision History

Date	Changes
2015-04-15	First release

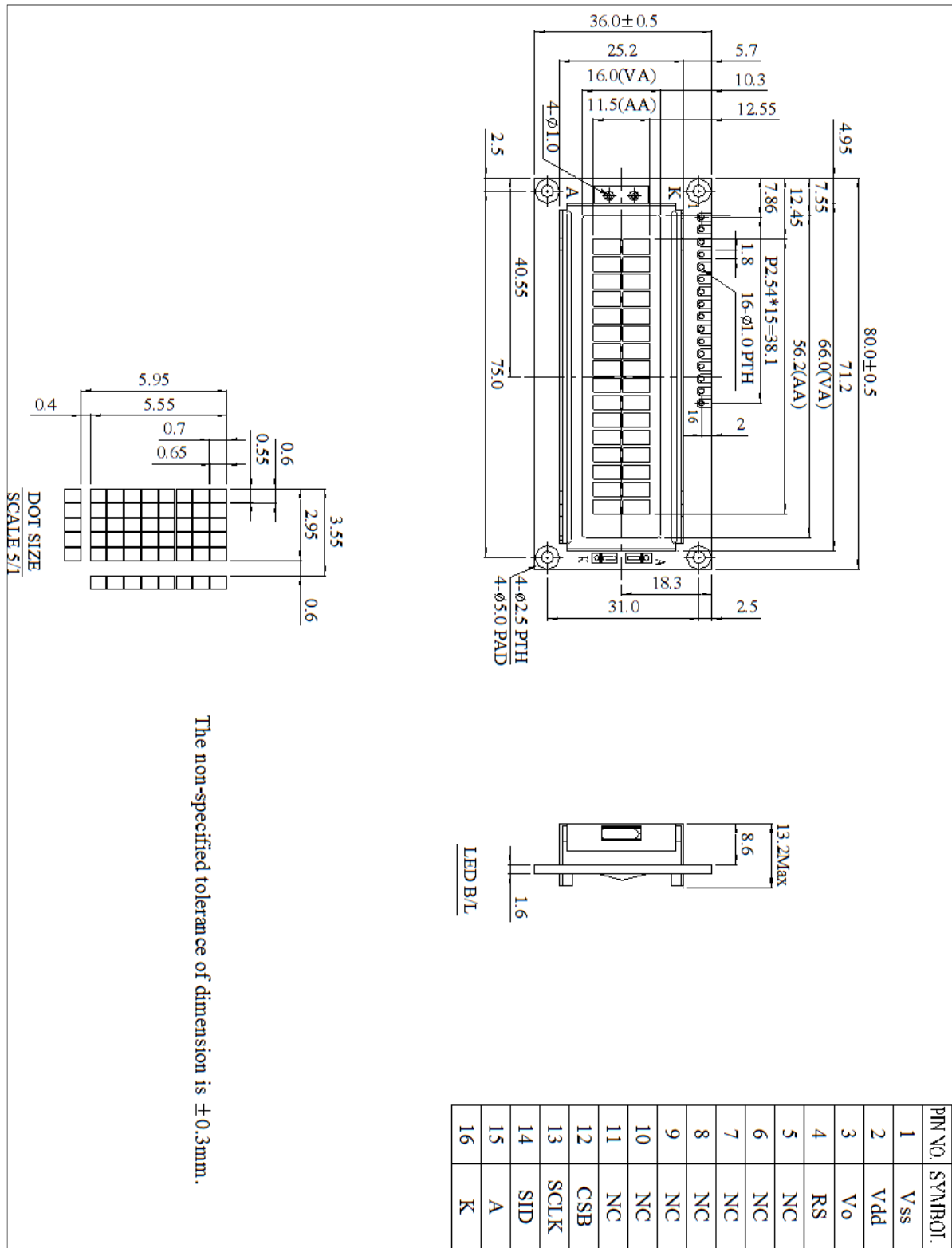
2 Main Features

Item	Specification	Unit
Number of Characters	16 characters x 2 lines	
Display Mode	STN Positive, Yellow Green, Transflective	-
Module dimension	80.0 x 36.0 x 13.2(MAX)	mm
Controller IC	DM4301C	-
Interface	SPI Interface	-
Power Supply	5.0	V
View Direction	6:00	-
Duty	1/16	
Backlight	Yellow Green LED	-
Weight	32.7	g

3 Pin Description

Pin No.	Symbol	Description
1	VSS	Ground
2	VDD	Supply Voltage for logic
3	VO	Operating voltage for LCD(Variable)
4	RS	In bus mode, used as register selection input. When RS = "High", Date register is selected. When RS = "Low", Instruction register is selected.
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	NC	No Connection
10	NC	No Connection
11	NC	No Connection
12	CSB	In 4-SPI serial mode, used as chip selection input. When CSB = "Low", selected When CSB = "High", not selected. (Low access enable)
13	SCLK	Serial clock input
14	SID	Serial data input
15	A	Power supply for B/L(+)
16	K	Power supply for B/L(-)

4 Mechanical Drawing



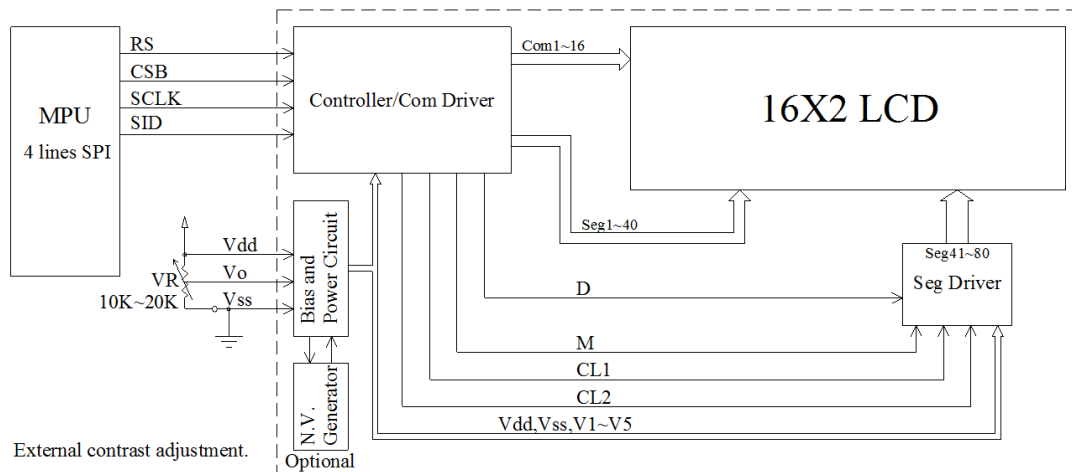
5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage For Logic	VDD		4.5	5.0	5.5	V
Supply Current	IDD	VDD=5.0V	1.0	1.2	1.5	mA
Low Level Input Voltage	V _{IL}		VSS	-	0.6	V
High Level Input Voltage	V _{IH}		0.7VDD	-	VDD	V
Low Level Output Voltage	V _{OL}		0		0.4	V
High Level Output Voltage	V _{OH}		3.9		VDD	V
Backlight Supply Voltage	V		3.9	4.1	4.3	V
Backlight Supply Current	I _{LED}		117	130	156	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	°C
Storage Temperature	TST	Absolute Max	-30	-	+80	°C

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Note
View Angles Top	AV		20		°	
View Angles Bottom	AV		40		°	
View Angles Left	AH		30		°	
View Angles Right	AH		30		°	
Response Time (25°C)	Tr + Tf		300	400	ms	
Contrast Ratio	CR		3			
Luminance (Without LCD)	L _v	216	270		cd/m ²	

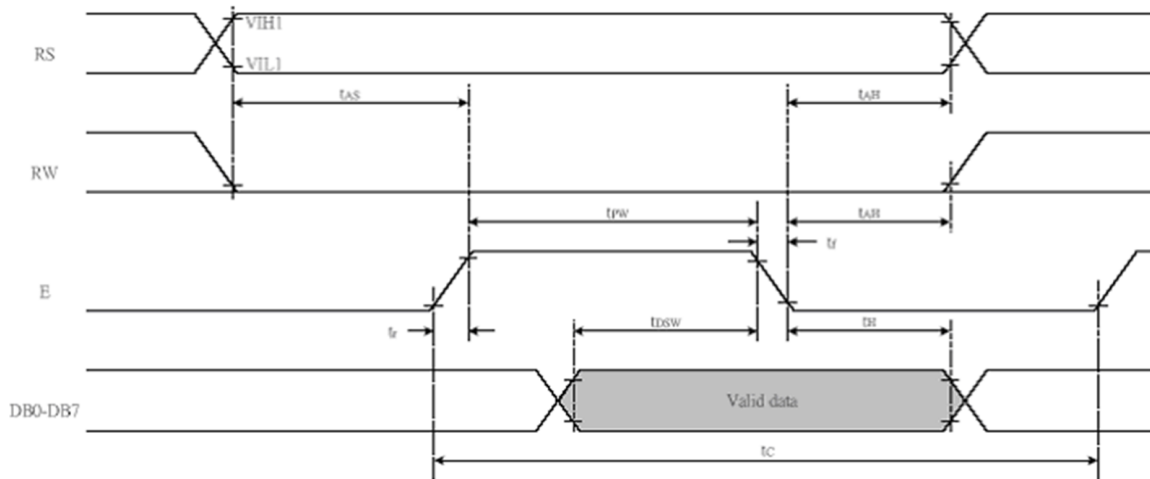
7 Block Diagram



Character located	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
DDRAM address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

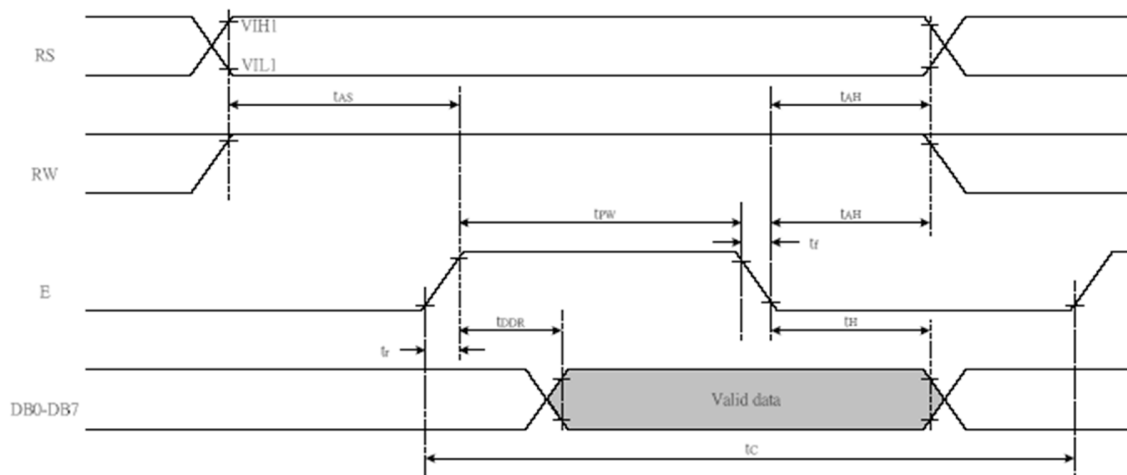
8 Timing Character

8.1 Write data from MPU to IC (Parallel 8-bit bus and 4-bit bus)



Symbol	Parameter	Min	Typ	Max	Unit
T_C	Enable Cycle Time	500	-	-	ns
T_{PW}	Enable Pulse Width	230	-	-	ns
T_{R}, T_F	Enable Rise/Fall Time	-	-	20	ns
T_{AS}	Address Setup Time	40	-	-	ns
T_{AH}	Address Hold Time	10	-	-	ns
T_{DSW}	Data Setup Time	80	-	-	ns
T_H	Data Hold Time	10	-	-	ns

8.2 Reading data from IC to MPU(Parallel 8-bit bus and 4-bit bus)



Symbol	Parameter	Min	Typ	Max	Unit
T_C	Enable Cycle Time	500	-	-	ns
T_{PW}	Enable Pulse Width	230	-	-	ns
T_{R}, T_F	Enable Rise/Fall Time	-	-	20	ns
T_{AS}	Address Setup Time	40	-	-	ns
T_{AH}	Address Hold Time	10	-	-	ns
T_{DDR}	Data Setup Time	-	-	120	ns
T_H	Data Hold Time	10	-	-	ns

9 Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Description Time (540KHz)	
Read display data	1	1	Read data								Read data into DDRAM/CGRAM/SEGRAM	18.5us	
Write display data	1	0	Write data								Write data into DDRAM/CGRAM/SEGRAM	18.5us	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM, and set DDRAM address to "00H" from AC	0.76ms	
Return Home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	0.76ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and specify display shift. These operations are performed during data read and write. I/D="1": increment I/D="0": decrement	18.5us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	Set Display /Cursor/Blink On/OFF D="1": display on D="0": display off C="1": cursor on C="0": cursor off B="1": blink on B="0": blink off	18.5us
Cursor or Display shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift S/C="1": display shift S/C="0": cursor shift R/L="1": shift to right R/L="0": shift to left	18.5us
Function Set	0	0	0	0	0	1	DL	N	F	X	X	Set Interface Data Length DL= 8-bit interface/ 4-bit interface N = 2-line/1-line display F = 5x8 Font Size / 5x11Font Size	18.5us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter		18.5us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter		18.5us
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can know internal operation is ready or not by reading BF. The contents of address counter can also be read. BF="1": busy state BF="0": ready state		0us

10 Instruction Description

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status; namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. A content of DDRAM does not change.

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D : Increment / decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

S: Shift of entire display

When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

Display ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF control bit

D = 1: entire display is turned on.

D = 0: display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit

C = 1: cursor is turned on.

C = 0: cursor is disappeared in current display, but I/D register remains its data

B : Cursor Blink ON/OFF control bit

B = 1: cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 540 kHz frequency, blinking has 185 ms interval.

B = 0: blink is off.

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to Table 4). During 2-line mode display, cursor moves to

the 2nd line after 40th digit of 1st line.

Note that display shift is performed simultaneously by the shift enable instruction. When displayed data is shifted repeatedly, all display lines shifted simultaneously. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description
0	0	Shift cursor to the left, address counter is decreased by 1
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift display to the left. Cursor moves according to the display
1	1	Shift display to the right. Cursor moves according to the display

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	X	X

DL : Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

IF using IIC and 4-SPI interface, DL bit must be setting to "1"

N : Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

F : Display font type control bit

When F = "Low", it means 5 x 8 dots format display mode

When F = "High", 5 x 11 dots format display mode.

N	F	No. of Display Lines	Character Font	Duty Factor
L	L	1	5 x 8	1/8
L	H	1	5 x 11	1/11
H	x	2	5 x 8	1/16

Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N=0), DDRAM address is from "00H" to "4FH"

In 2-line display mode (N=1), DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H"

Read Busy Flag and Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether Controller is in internal operation or not. If the resultant BF is "high", it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data from RAM (only support parallel 8-bit bus and 4 bit bus)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined.

If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

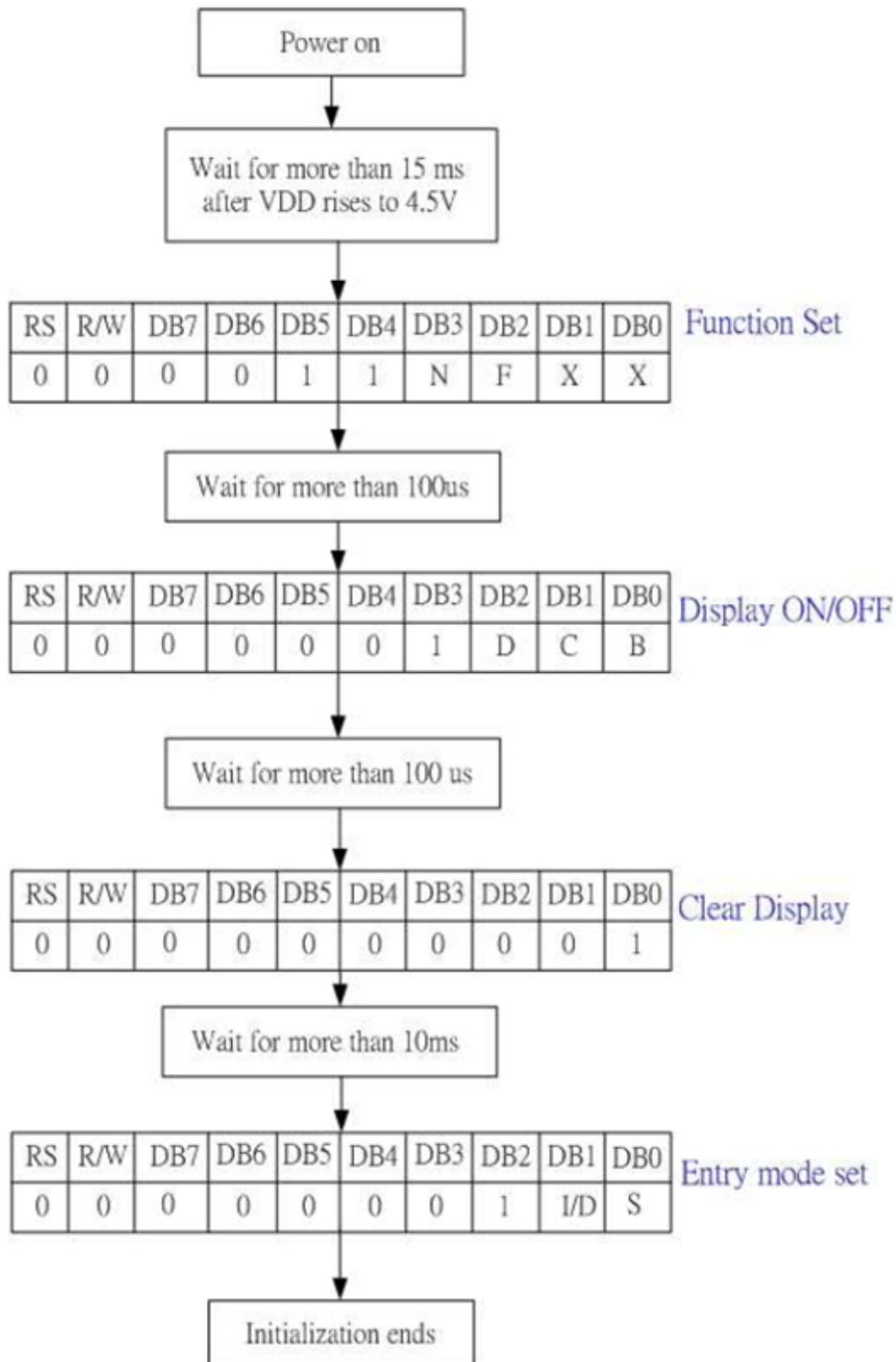
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

11 Initializing by Instruction

Serial Interface(focs=540KHz)



12 Built-in Font Table

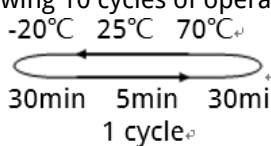
b7~4 b3~0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM [00]			0	a	P	\	P				-	9	5	o	P
0001	CG RAM [01]		!	1	A	Q	a	q			.	7	7	4	3	9
0010	CG RAM [02]		"	2	B	R	b	r			7	7	W	X	P	o
0011	CG RAM [03]		#	3	O	S	s	s			7	7	T	E	e	o
0100	CG RAM [04]		\$	4	D	T	d	t			7	7	T	P	H	a
0101	CG RAM [05]		%	5	E	U	e	u			.	*	*	1	o	o
0110	CG RAM [06]		&	6	F	V	f	v			7	7	2	3	P	2
0111	CG RAM [07]		'	7	G	W	g	w			7	7	7	7	9	x
1000	CG RAM [00]		<	8	H	X	h	x			7	7	7	7	7	7
1001	CG RAM [01]		>	9	I	Y	i	y			7	7	7	7	7	7
1010	CG RAM [02]		*	:	J	Z	j	z			7	7	7	7	7	7
1011	CG RAM [03]		+	;	K	C	k	c			7	7	7	7	7	7
1100	CG RAM [04]		,	<	L	#	l	l			7	7	7	7	7	7
1101	CG RAM [05]		-	=	M	I	m	i			7	7	7	7	7	7
1110	CG RAM [06]		.	>	N	^	n	^			7	7	7	7	7	7
1111	CG RAM [07]		/	?	O	_	o	_			7	7	7	7	7	7

13 Driver/Controller Information

Built-in DM4301C IC

<https://drive.google.com/file/d/0B5IkVYnewKTGWUxUE5qc0hsbkk/view?usp=sharing>

14 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20°C/70°C 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

15 Warranty and Conditions

<http://www.displaymodule.com/pages/faq>