DisplayModule

DM-COG12864-714

12864 COG GRAPHIC LCD WITH PARALLEL OR SERIAL MPU INTERFACE

Contents

1 Revision History

Date	Changes
2015-03-13	First release

2 Main Features

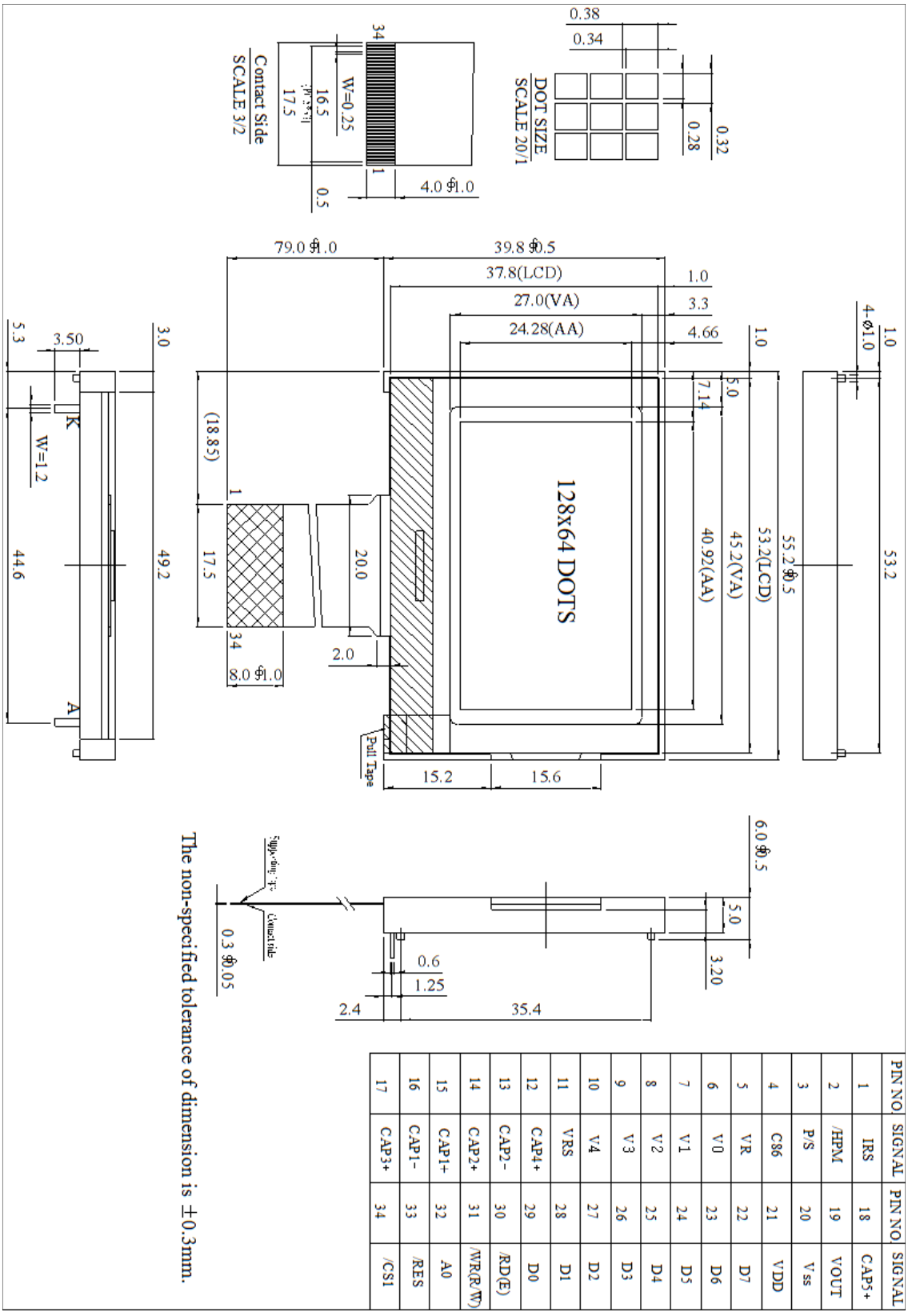
Item	Specification	Unit
Resolution	128 x 64	dots
LCD Type	STN Positive Yellow/Green	
Driver Mode	Transflective	-
Controller IC	ST7565P	-
Interface	Parallel or Serial MPU Interface	-
Power Supply	3.0	V
View Direction	6:00	-
Duty	1/64 duty, 1/9 bias	
Backlight	Yellow/Green LED	-
Weight		g

3 Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function Description</th></tr>
<tr><td>1</td><td>IRS</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal</td></tr>
<tr><td>2</td><td>/HPM</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM = “H”: Normal mode
/HPM = “L”: High power mode</td></tr>
<tr><td>3</td><td>P/S</td><td>This is the parallel data input/serial data input switch terminal.
P/S = “H”: Parallel data input.
P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>D0 toD7</td><td>/RD,/WR</td><td>X</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI(D7)</td><td>Write only</td><td>SCL(06)</td></tr>
</table>
When P/S = “L”, D0 to D5 fixed “H”.
/RD (E) and /WR (R/W) are fixed to either “H” or “L”.
With serial data input, It is impossible read data from RAM</td></tr>
<tr><td>4</td><td>C86</td><td>This is the MPU interface selection pin.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 Series MPU interface</td></tr>
<tr><td>5</td><td>NR</td><td>Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider.
IRS = “L” : the V0 voltage regulator internal resistors are not used.
IRS = “H” : the V0 voltage regulator internal resistors are used.</td></tr>
<tr><td>6~10</td><td>V0~V4</td><td>This is a multi-level power supply for the liquid crystal drive.</td></tr>
<tr><td>11</td><td>VRS</td><td>This is the internal-output VREG power supply for the LCD power supply voltage regulator.</td></tr>
<tr><td>12</td><td>CAP4+</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td></tr>
<tr><td>13</td><td>CAP2-</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.</td></tr>
<tr><td>14</td><td>CAP2+</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td></tr>
<tr><td>15</td><td>CAP1+</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>16</td><td>CAP1-</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.</td></tr>
<tr><td>17</td><td>CAP3+</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>18</td><td>CAP5+</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>19</td><td>VOUT</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and vss or VDD</td></tr>
<tr><td>20</td><td>VSS</td><td>Ground</td></tr>
<tr><td>21</td><td>VDD</td><td>Power supply</td></tr>
<tr><td>22~29</td><td>D7~D0</td><td>Data bus line</td></tr>
<tr><td>30</td><td>/RD(E)</td><td>When connected to 8080 series MPU, this pin is treated as the “/RD” signal of the 8080 MPU and is LOW-active.
The data bus is in an output status when this signal is “L”.</td></tr>
</table>

		When connected to 6800 series MPU, this pin is treated as the “E” signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
31	/WR(RW)	When connected to 8080 series MPU, this pin is treated as the “/WR” signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to 6800 series MPU, this pin is treated as the “R/W” signal of the 6800 MPU and decides the access type : When R/W = “H”: Read. When R/W = “L”: Write.
32	A0	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.
33	/RES	When RES is set to “L”, the setting are initialized.
34	/CS1	This is the chip select signal.

4 Mechanical Drawing



PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	IRS	18	CAP5+
2	/HPM	19	VOUT
3	P/S	20	Vss
4	C86	21	VDD
5	VR	22	D7
6	V0	23	D6
7	V1	24	D5
8	V2	25	D4
9	V3	26	D3
10	V4	27	D2
11	VRS	28	D1
12	CAP4+	29	D0
13	CAP2-	30	/RD(E)
14	CAP2+	31	/WR(R/W)
15	CAP1+	32	A0
16	CAP1-	33	/RES
17	CAP3+	34	/CS1

5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage For Logic	VDD		2.7	3.0	3.3	V
Digital Operation Current	IDD	-	-	0.49	1.0	mA
Low Level Input Voltage	V_{IL}		VSS	-	0.2VDD	V
High Level Input Voltage	V_{IH}		0.8VDD	-	VDD	V
Low Level Output Voltage	V_{OL}		VSS		0.2VDD	V
High Level Output Voltage	V_{OH}		0.8VDD		VDD	V
Backlight Forward Voltage	V_{LED}		3.4	3.5	3.6	V
Backlight Forward Current	I_{LED}			48	60	mA
Operating Temperature	TOP	Absolute Max	-20		70	℃
Storage Temperature	TST	Absolute Max	-30		80	℃

6 Optical Characteristics

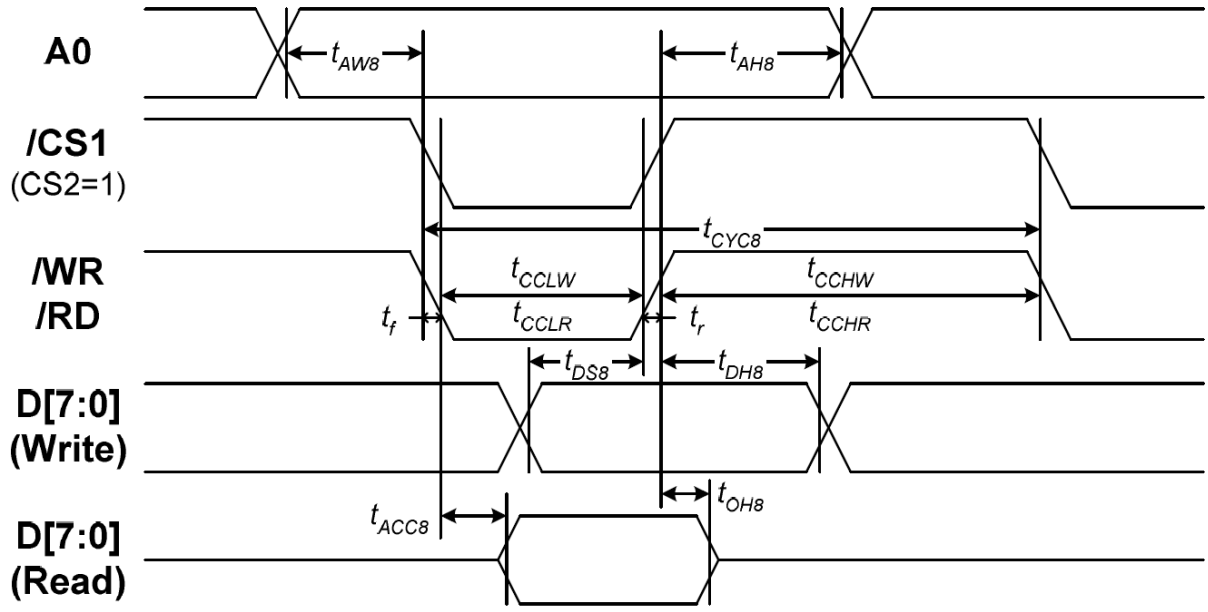
Item	Symbol	Min	Typ	Max	Unit	Note
View Angles-Top	AH	0		20	°	
View Angles-Bottom	AH	0		40	°	
View Angles-Right	AV	0		30	°	
View Angles-Left	AV	0		30	°	
Response Time (25°C)	Tr + Tf		450	650	us	
Contrast Ratio	CR		3			

7 Table of Commands

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	0	1	Set the V_0 output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value						
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

8 Timing Characteristics

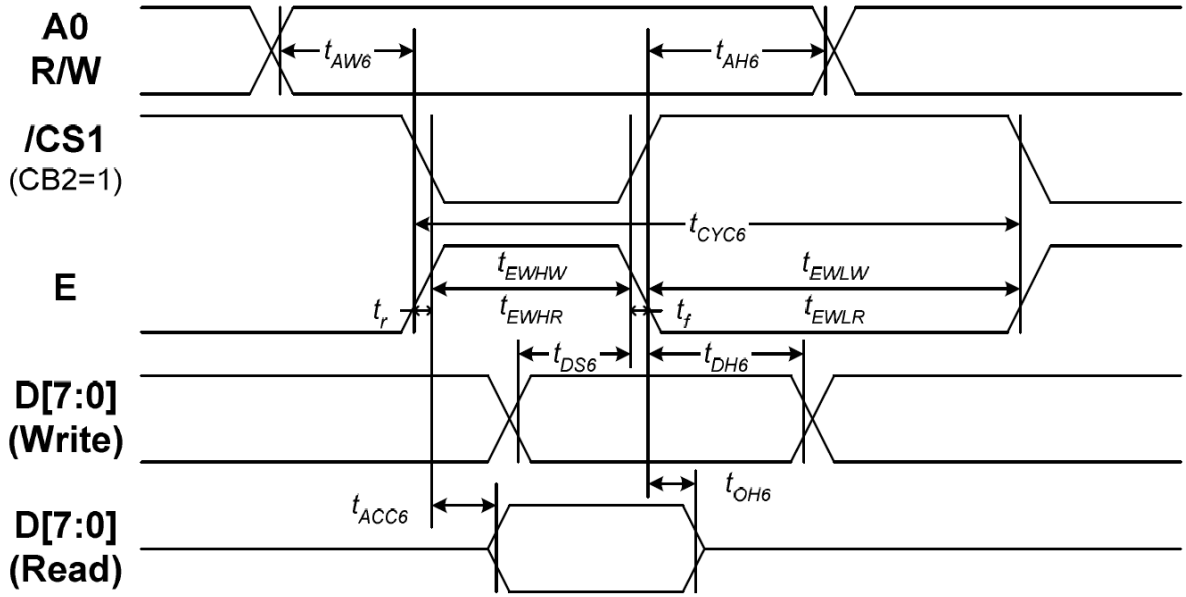
8.1 System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



VDD=3.3V, TA=-30 to 85℃

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{AH8}	Address hold time	0	-	-	ns
t_{AW8}	Address setup time	0	-	-	ns
t_{CYC8}	System cycle time	240	-	-	ns
t_{CCLW}	Write L pulse width	80	-	-	ns
t_{CCHW}	Write H pulse width	80	-	-	ns
t_{CCLR}	Read L pulse width	140	-	-	ns
t_{CCHR}	Read H pulse width	80	-	-	ns
t_{DS8}	Write Data setup time	40	-	-	ns
t_{DH8}	Write Address hold time	0	-	-	ns
t_{ACC8}	Read access time	-	-	70	ns
t_{OH8}	Read Output disable time	5	-	50	ns

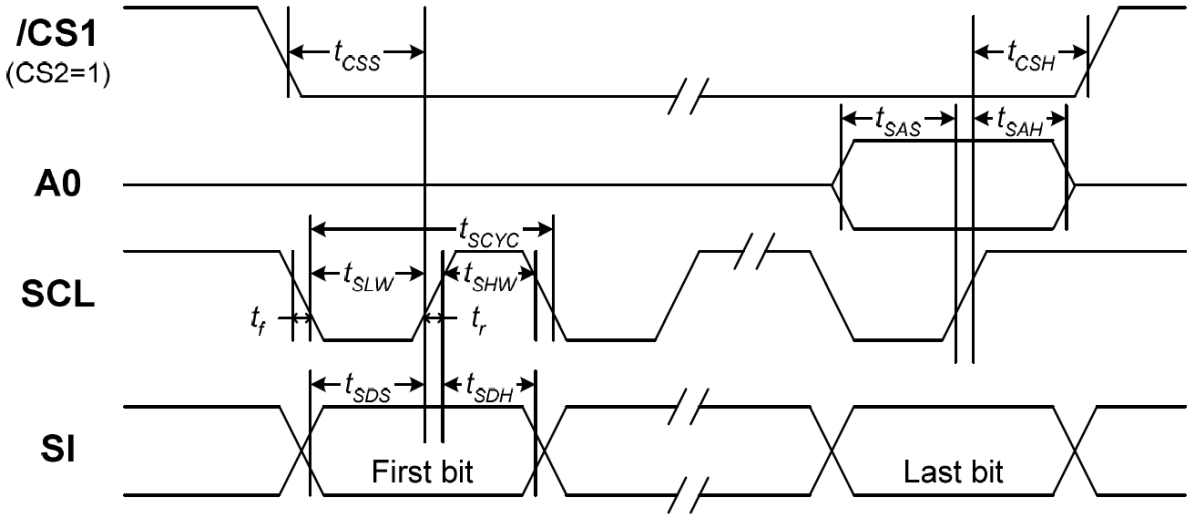
8.2 System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)



VDD=3.3V,TA=-30~85℃

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{AH6}	Address hold time	0	-	-	ns
t_{AW6}	Address setup time	0	-	-	ns
t_{CYC6}	System cycle time	240	-	-	ns
t_{EWLW}	Enable L pulse width (Write)	80	-	-	ns
t_{EWHW}	Enable H pulse width(Write)	80	-	-	ns
t_{EWLR}	Enable L pulse width(Read)	80	-	-	ns
t_{EWHR}	Enable H pulse width(Read)	140	-	-	ns
t_{DS6}	Write Data setup time	40	-	-	ns
t_{DH6}	Write Address hold time	0	-	-	ns
t_{ACC6}	Read access time	-	-	70	ns
t_{OH6}	Read Output disable time	5	-	50	ns

8.3 Serial Interface



Symbol	Parameter	Min.	Typ.	Max	Unit
t_{SCYC}	Serial Clock Period	50	-	-	ns
t_{SHW}	SCL “H” pulse width	25	-	-	ns
t_{SLW}	SCL “L” pulse width	25	-	-	ns
t_{SAS}	Address setup time	20	-	-	ns
t_{SAH}	Address hold time	10	-	-	ns
t_{SDS}	Data setup time	20	-	-	ns
t_{SDH}	Data hold time	10	-	-	ns
t_{CSS}	CS-SCL time	20	-	-	ns
t_{CSH}	CS-SCL time	40	-	-	ns

9 MPU Interface

9.1 Selecting the Interface Type

With the ST7565P chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SI). By setting the P/S terminal to “H” or “L”, it sets the access mode to be either parallel or serial mode as shown follow:

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H:6800 Series	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L:8080 Series	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

“—” indicates fixed to either “H” or to “L”

9.2 The Parallel Interface

When the parallel interface has been selected (P/S =“H”), the interface can be connected directly to either 8080 or 6800 Series MPU (as shown follow) by setting the C86 terminal to either “H” or “L”.

C86 (P/S=H)	/CS1	CS2	A0	E(/RD)	R/W(/WR)	D7~D0
H:6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L:8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

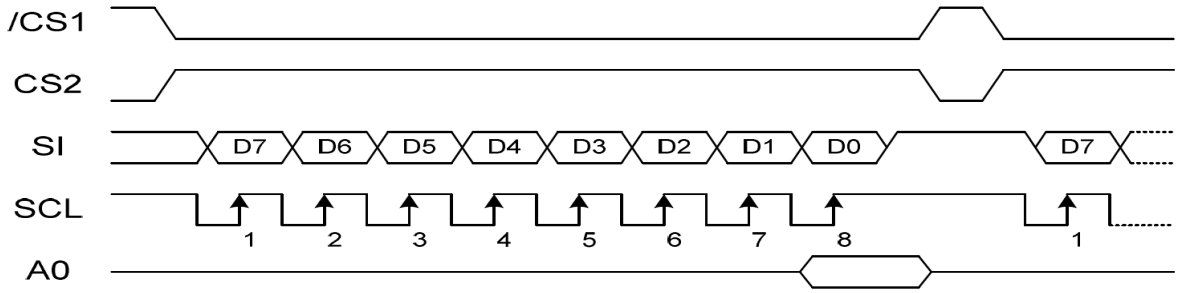
Moreover, data bus signals are recognized according to the combination of A0, /RD (E), /WR (R/W) signals. The functions are shown as below.

Shared	6800 Series	8080 Series		Function
A0	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

9.3 The Serial Interface

When the serial interface has been selected (P/S = “L”) then when the chip is in active state (/CS1 = “L” and CS2 = “H”) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.



Notes:

When the chip is not active, the shift registers and the counter are reset to their initial states.

Reading is not possible while in serial interface mode.

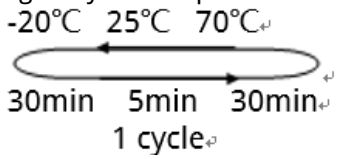
Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

10 Driver/Controller Information

Built-in ST7565P Controller

https://drive.google.com/file/d/0B_HGldxxTS9iMjE1Mk54OEZqekk/view?usp=sharing

11 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 ℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: The packing have to including into the vibration testing.

12 Warranty and Conditions

http://www.displaymodule.com/pages/faq