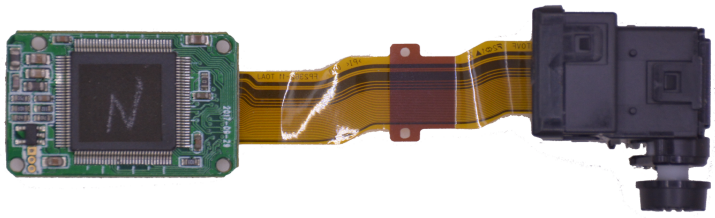
DisplayModule



DM-ADTTR-023

1. Specification summary

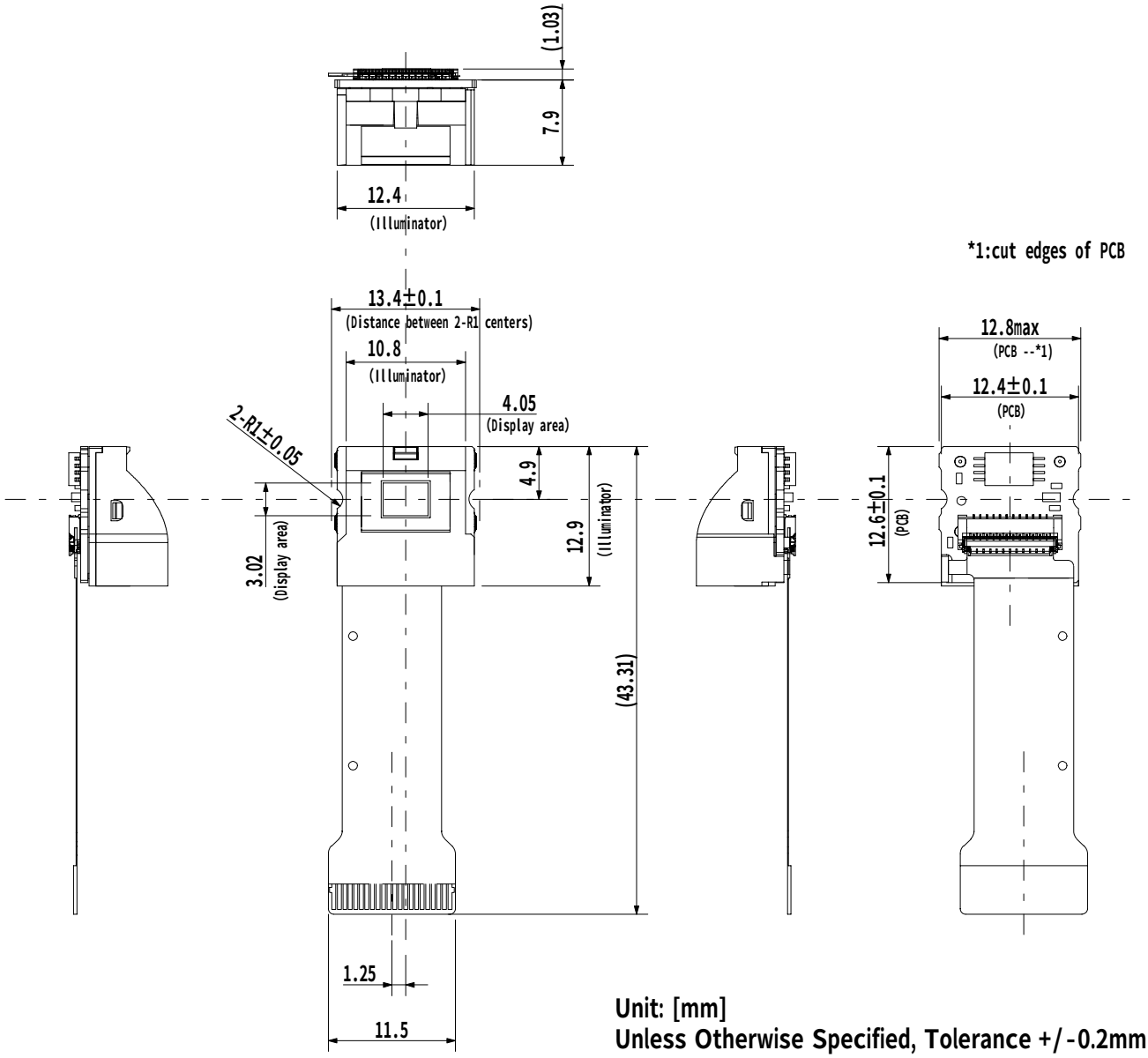
Table1: Specification summary

Parameter	Specification
Display technology	Ferroelectric Liquid Crystal (FLC) on reflective CMOS
Display mode	Field sequential color
Display format	300 (H) x 224 (V)
Display panel active area	4.05 x 3.02 mm (4:3 aspect ratio)
Display panel diagonal	5.0 mm (0.20")
Input Grayscale	256 levels
Display pixel pitch	13.5 x 13.5 um
Pixel fill factor	94%
Color depth	4.2Million unique colors (YCrCb video interface)
Display frame rate	120 Hz (NTSC), 100 Hz (PAL)
Data clock rate	27 MHz
Digital display interface	CCIR 601 CCIR 656 RGB 8bit serial data
Control interface	4 wire serial
Operating supply voltages	2.5 V (core), 5.0 V (LED, Analog)
Power consumption *1	90 mW (Reference)
Operating temperature	-10deg.C to +70deg.C
Storage temperature	-30deg.C to +83deg.C

*1 Typical value at 60 Hz NTSC (gamma correction of 2.1),
CCIR-601 operation with flat field video pattern at room temperature.

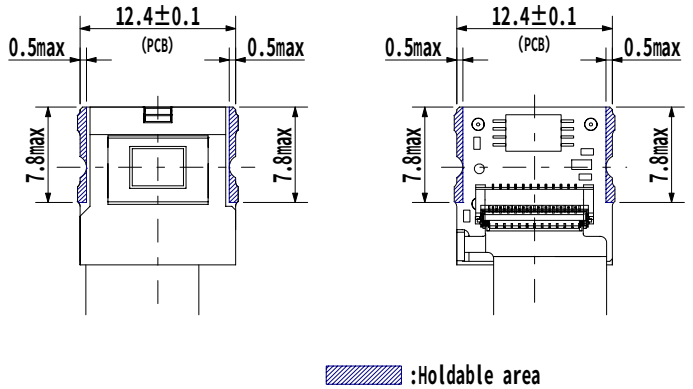
3.Product Appearance

3.1 Appearance Specifications



Unit: [mm]
Unless Otherwise Specified, Tolerance +/-0.2mm

Fig1-1: Appearance Specifications



Product should be held at the specified area of PCB which is shown in Fig.1-2.
Do not hold other area of PCB, illuminator, and electrical parts, to prevent the product damage.

Unit: [mm]

Fig1-2: Holdable area of PCB

3.2 Flex Specifications

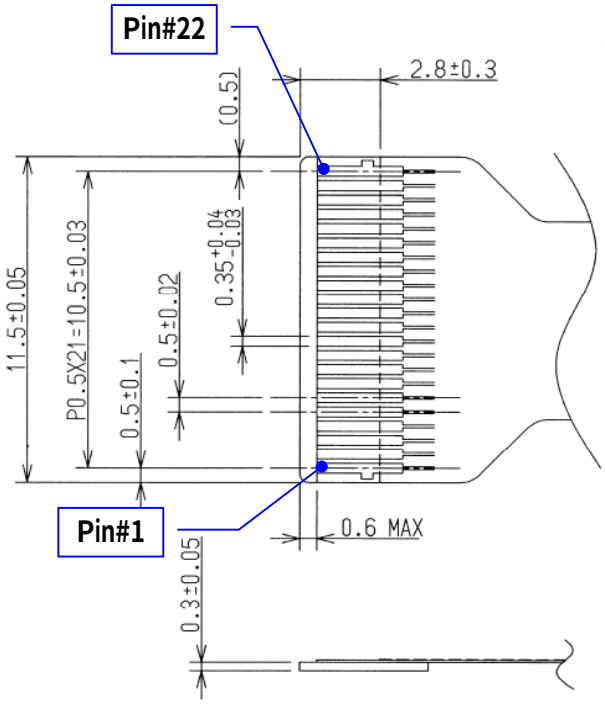


Fig2: Connector Tab Details

3.3 Pixel Specifications

The rectangular microdisplay of 4.05 by 3.02 mm consists of 300 by 224 pixels of 0.0135 mm (pixel dimensions include a 0.0005 mm interpixel gap). This means that the viewing lens cutoff frequency should be above 37 lines/mm. The individual pixels have a hexagon shape, with each row being offset from the previous row. Fig.3 shows details of the pixel layout, including corner and edge pixel shape.

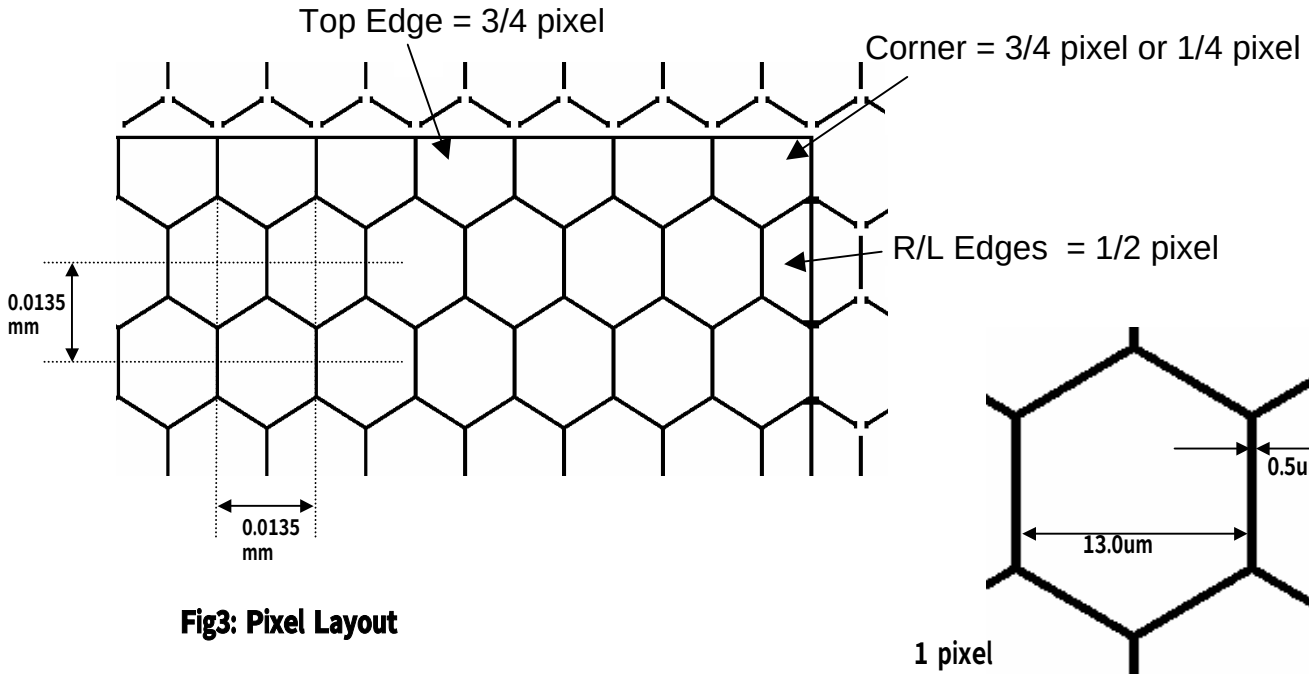


Fig3: Pixel Layout

4.Electrical Specifications

4.1 Pin Descriptions

Table2: Pin Descriptions

Pin Num.	Pin Name	Pin Direction	Pin Function		
			CCIR-601	CCIR-656	RGB 8bit serial
22	VDD	Power	Core power supply (+2.5V)		
21	GND	Ground	Power and signal return		
20	NRESET	Input	System reset		
19	CLOCK	Input	CLOCK		
18	HSYNC	Input	HSYNC	GND	HSYNC
17	VSYNC	Input	VSYNC	GND	VSYNC
16	VALID	Input	VALID*1	GND	VALID*1
15	DATA 0	Input	Y/Cr/Cb 0	Y/Cr/Cb 0	R/G/B 0
14	DATA 1	Input	Y/Cr/Cb 1	Y/Cr/Cb 1	R/G/B 1
13	DATA 2	Input	Y/Cr/Cb 2	Y/Cr/Cb 2	R/G/B 2
12	DATA 3	Input	Y/Cr/Cb 3	Y/Cr/Cb 3	R/G/B 3
11	NC	-	Not used		
10	DATA 4	Input	Y/Cr/Cb 4	Y/Cr/Cb 4	R/G/B 4
9	DATA 5	Input	Y/Cr/Cb 5	Y/Cr/Cb 5	R/G/B 5
8	DATA 6	Input	Y/Cr/Cb 6	Y/Cr/Cb 6	R/G/B 6
7	DATA 7 (MSB)	Input	Y/Cr/Cb 7	Y/Cr/Cb 7	R/G/B 7
6	SDAT	Input	Serial interface data input		
5	SOUT	Output (Open Drain)	Serial interface data output (not required for operation)		
4	SCLK	Input	Serial interface clock input		
3	SEN	Input	Serial interface chip select		
2	GND	Ground	Power and signal return		
1	VCC	Power	Analog and illumination power supply (+5.0V)		

*1 Use of the VALID signal to indicate when data should be sampled is not required.
See CCIR 601 Video Format description or RGB Serial Video Format description for details.
(Connect VALID pin to GND when it is not used.)

4.2 Electrical Circuit

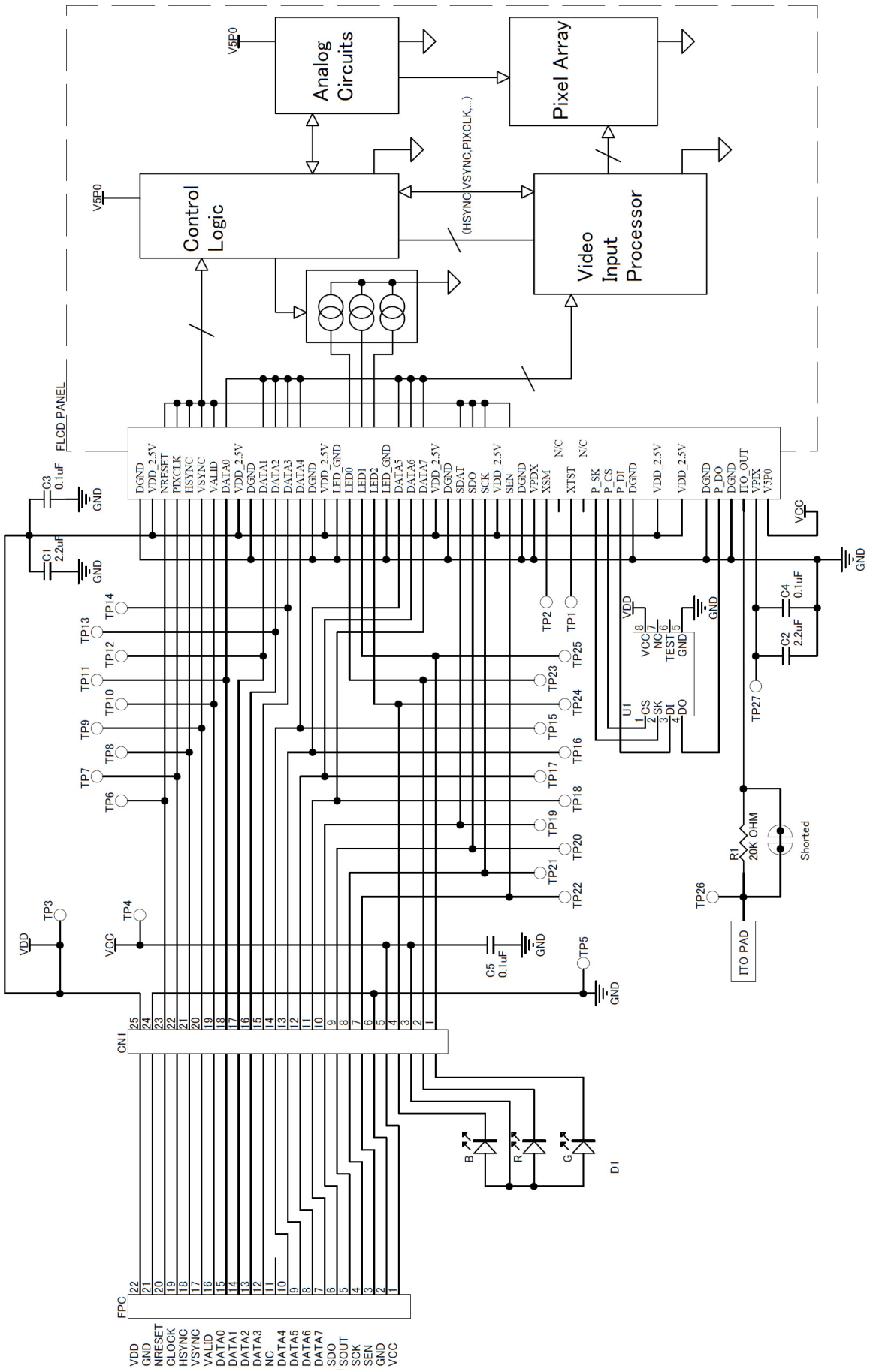


Fig4: Electrical circuit

4.3 Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each input pin, except for Vdd, Vcc and GND (Vss) inputs.
The equivalent circuit of the input pins is shown below (Resistance values shown typical):

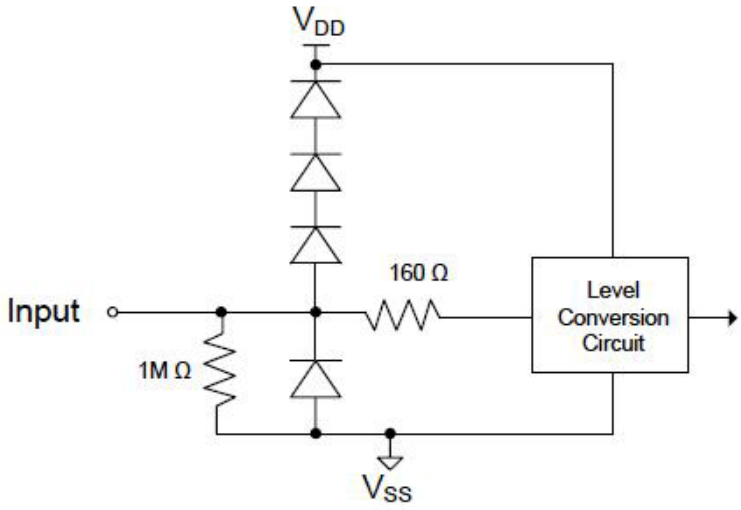


Fig5: Input Equivalent Circuit

4.4 Absolute Maximum Ratings

Table3: Absolute Maximum Ratings

Item	Min.	Max.	Unit
VDD (+2.5V)		3.0	V
VCC(+5V)		6.0	V
Voltage on any Input Pin to GND	GND-0.4	VDD+1.4	V

4.5 Operating Conditions

Table4: Operating Conditions (DC characteristics)

Item	Symbol	Note	Min.	Typ.	Max.	Unit
Supply voltage	VDD		2.3	2.5	2.7	V
	VCC		4.5	5.0	5.5	V
Input Voltage	V_{IH}	For all inputs	2.3		VDD+1.4	V
	V_{IL}	For all inputs	GND-0.4		0.5	
Input Capacitance	I_C	For all inputs 3.3V Sqr @27Mhz		8	16	pF
Input Leakage Current	I_{IL}	$V_I = V_{IL}$	-10			uA
	I_{IH}	$V_I = V_{IH}$			10	
Average Supply Current *1	I_{VDD}	Normal Mode		22	28	mA
		Sleep Mode		3.8	5.3	
	I_{VCC}	Normal Mode		7 (reference)	12 (reference)	
		Sleep Mode		0.3	0.9	

*1) Measurement condition: Brightness register=maximum, Gamma correction=2.1,
Input video data=flat field pattern of white.

5. Video Input Interface

5.1 Supported Video Formats

This product supports CCIR-601, CCIR-656 and RGB 8bit serial data video formats.

For CCIR-601 and RGB serial video sources, separate HSync and VSync signals must be provided. The sampling of video data can be configured to use either the VALID signal to indicate valid image data, or a configurable delay after the assertion of HSync or VSync including adjustment of delay between odd and even fields. The odd and even video fields must be correctly indicated by the relation of the VSync and HSync pulses per the CCIR-601 specification.

For the CCIR-656 video sources, the odd and even field must be correctly indicated by the 'F' bit of the SAV and EAV codes per the CCIR-656 specification.
Video input sources can be at either 50Hz or 60Hz vertical frequency and can be displayed with or without overscan.

5.2 Video Scaling and Cropping

Scaling coefficients are calculated as follows.
Horizontal (or Vertical) scale step = (display resolution/post crop input resolution)*512
Horizontal (or Vertical) scale cycle = display resolution/GCD(display resolution, post crop input)
*1: Decimal places truncated.
*2: "GCD" means Greatest Common Divisor.

Video data for the CCIR video formats must be either 720 by 242, 720 by 240, or 720 by 288 resolution.
Table5 shows scaling settings for each video formats.

Table5 : Scaling and Cropping Options for Supported Video Formats

Input Resolution		Overscan	Valid Delay *1		Post-Crop Resolution		Interpolation Register Settings			
H	V		H	V	H	V	H Coef.	H Cycle	V Coef.	V Cycle
720	240	None	0	0	720	240	214	5	478	14
720	240	7.0%	48	8	672	224	229	25	512	1
720	242	None	0	1	720	240	214	5	478	14
720	242	7.0%	48	9	672	224	229	25	512	1
720	288	None	0	0	720	288	214	5	399	7
720	288	8.3%	60	12	660	264	233	5	435	28

*1 Valid Delay settings must be adjusted when not using the VALID signal to indicate when data should be sampled. See CCIR 601 Video Format description for details.

5.3 CCIR-601 Video Format

5.3-1 Video Input Vertical Timing, CCIR-601 Video Formats

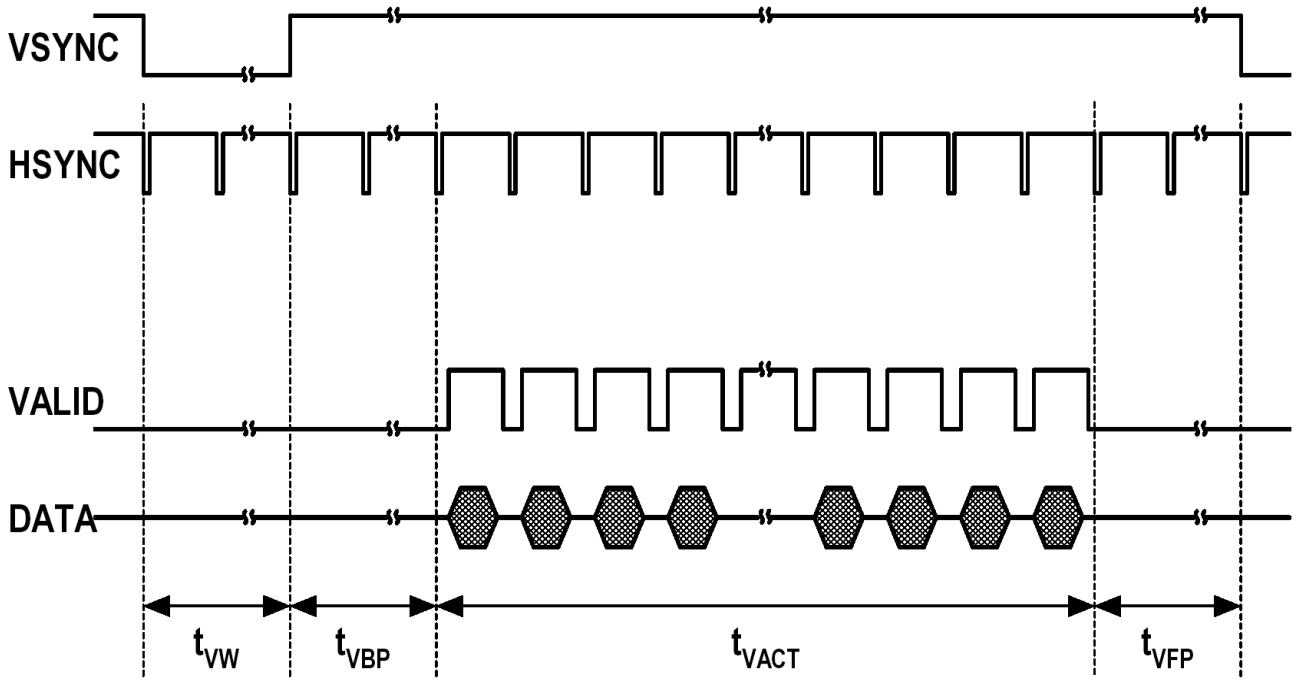


Fig6-1: CCIR-601 Video input vertical timing

5.3-2 Video Input Horizontal Timing, CCIR-601 Video Format

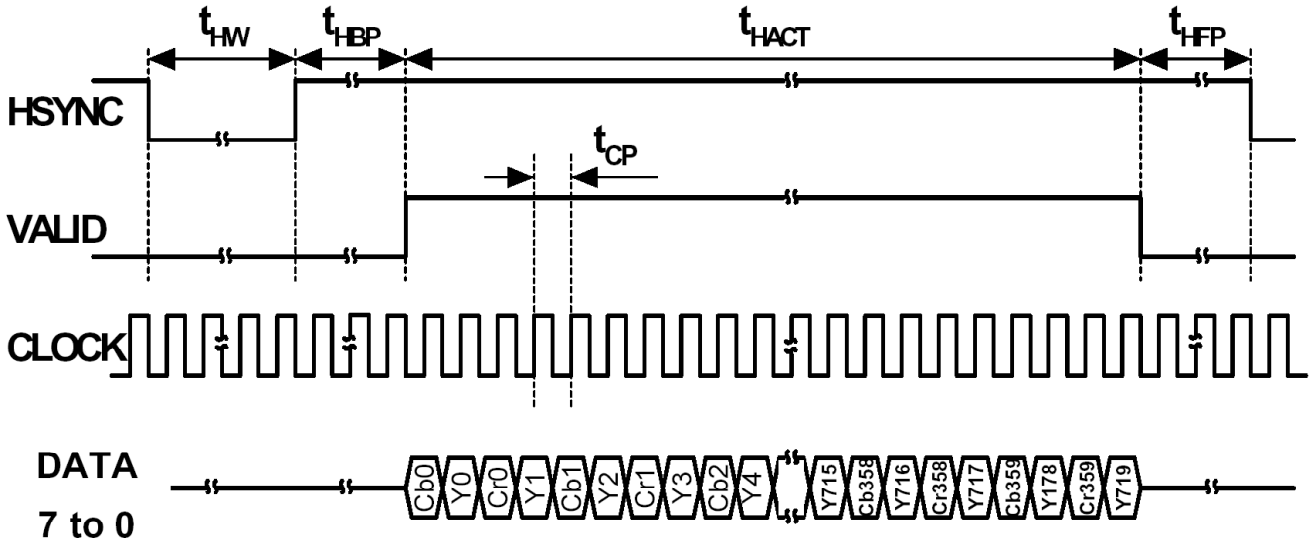


Fig6-2: CCIR-601 Video input horizontal timing

Table6-1: AC Characteristics, CCIR-601 240/242-line, 60Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	59	60	61	Hz
VSYNC, total lines	t_{VTOT} $t_{VBLK} + t_{VACT}$	260	262	266	Lines
VSYNC, active lines	t_{VACT}	240	242	242	Lines
VSYNC, blanking	t_{VBLK}= $t_{VFP} + t_{VW} + t_{VBP}$	18	22	26	Lines
VSYNC, front porch	t_{VFP}	3	3	7	Lines
VSYNC, pulse width	t_{VW}	3	3	7	Lines
VSYNC, back porch	t_{VBP}	12	16	20	Lines
HSYNC, total clocks	t_{HTOT} $t_{HBLK} + t_{HACT}$	1690	1716	1746	Clocks
HSYNC, active clocks	t_{HACT}	1440	1440	1440	Clocks
HSYNC, blanking	t_{HBLK} $t_{HFP} + t_{HW} + t_{HBP}$	250	276	306	Clocks
HSYNC, front porch	t_{HFP}	15	32	62	Clocks
HSYNC, pulse width	t_{HW}	100	126	156	Clocks
HSYNC, back porch	t_{HBP}	92	118	148	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	$1/4\ t_{HTOT}$	$1/2\ t_{HTOT}$	$3/4\ t_{HTOT}$	Clocks

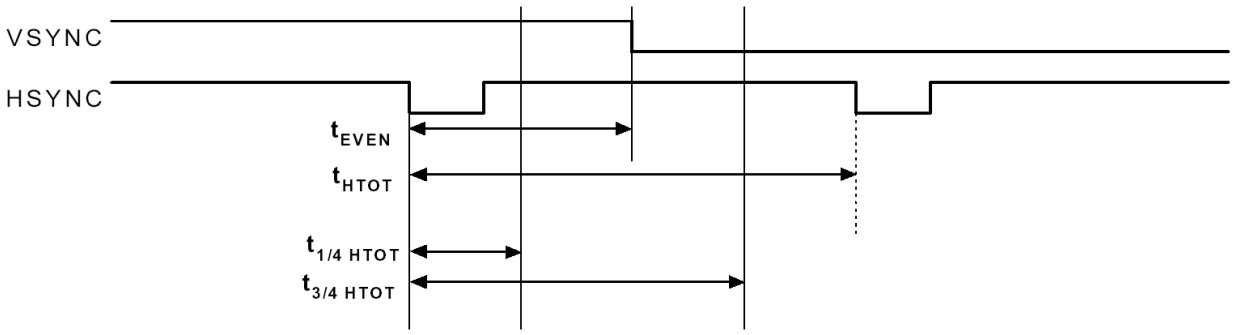


Fig7: Video Input Field Detection

Table6-2: AC Characteristics, CCIR-601 288-line, 50Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	49	50	51	Hz
VSYNC, total lines	t_{VTOT} $t_{VBLK} + t_{VACT}$	306	312	318	Lines
VSYNC, active lines	t_{VACT}	288	288	288	Lines
VSYNC, blanking	t_{VBLK}= $t_{VFP} + t_{VW} + t_{VBP}$	18	24	30	Lines
VSYNC, front porch	t_{VFP}	3	3	9	Lines
VSYNC, pulse width	t_{VW}	3	3	9	Lines
VSYNC, back porch	t_{VBP}	12	18	24	Lines
HSYNC, total clocks	t_{HTOT} $t_{HBLK} + t_{HACT}$	1698	1728	1766	Clocks
HSYNC, active clocks	t_{HACT}	1440	1440	1440	Clocks
HSYNC, blanking	t_{HBLK} $t_{HFP} + t_{HW} + t_{HBP}$	258	288	326	Clocks
HSYNC, front porch	t_{HFP}	15	24	62	Clocks
HSYNC, pulse width	t_{HW}	96	126	164	Clocks
HSYNC, back porch	t_{HBP}	108	138	176	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	$1/4\ t_{HTOT}$	$1/2\ t_{HTOT}$	$3/4\ t_{HTOT}$	Clocks

5.3-3 CCIR 601 Without VALID

When the SyncMode bits of the Video Configuration Register0 are programmed to "01", the product will ignore the VALID input pin and begin sampling video data after a specified delay from the assertion of HSYNC and VSYNC. The Vertical Field Offset Register, the Horizontal Valid Delay Register, and the Vertical Valid Delay Register are used to specify these delays. The values to program these register fields are as follows.

Table7: Register Values Enabling CCIR 601 Without Valid

Register Field	Calculation	Unit
HVldDelay	$t_{HW} + t_{HBP}$ + (horizontal overscan delay) - 2	Clocks
VVldDelay	$t_{VW} + t_{VBP}$ + (vertical overscan delay)	Lines
VldDelOffset	$(t_{VW} + t_{VBP})_{even\ field} - (t_{VW} + t_{VBP})_{odd\ field}$	Lines

5.4 CCIR-656 Video Format

5.4-1 Video Input Timing, CCIR-656 Video Format

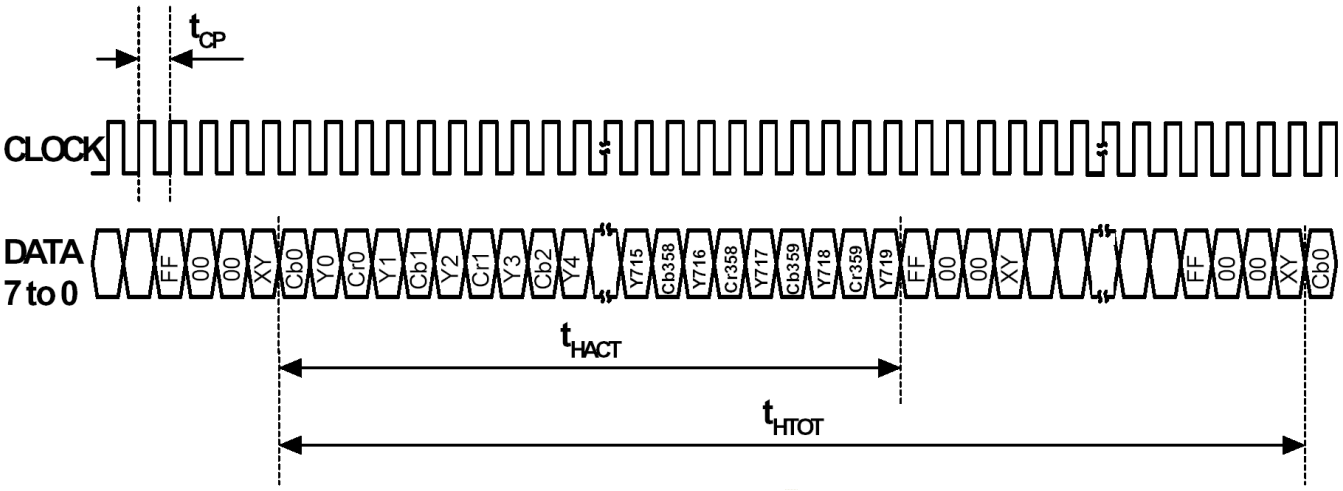


Fig8: CCIR-656 Video input timing

Table8-1: AC Characteristics, CCIR-656 240/242-line, 60Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
Vertical frequency	t_{VF}	59	60	61	Hz
Total lines per field	t_{VTOT}	258	262	266	Lines
Active lines per field	t_{VACT}	240	242	242	Lines
Total clocks per line	t_{HTOT}	1690	1716	1746	Clocks
Active clocks per line	t_{HACT}	1440	1440	1440	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz

Table8-2: AC Characteristics, CCIR-656 288-line, 50Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
Vertical frequency	t_{VF}	49	50	51	Hz
Total lines per field	t_{VTOT}	306	312	318	Lines
Active lines per field	t_{VACT}	288	288	288	Lines
Total clocks per line	t_{HTOT}	1698	1728	1766	Clocks
Active clocks per line	t_{HACT}	1440	1440	1440	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz

Table9: Bit Arrangement for CCIR-656 SAV and EAV Codes

CCIR-656 Information	Pin Name	First Word	Second Word	Third Word	Fourth Word
Data 7 (MSB)	Data 7 (MSB)	1	0	0	1
Data 6	Data 6	1	0	0	F
Data 5	Data 5	1	0	0	V
Data 4	Data 4	1	0	0	H
Data 3	Data 3	1	0	0	P3
Data 2	Data 2	1	0	0	P2
Data 1	Data 1	1	0	0	P1
Data 0 (LSB)	Data 0	1	0	0	P0

Note 1: Bit codes F, V, and H are defined as
F = 0 during field 1 and 1 during field 2
V = 1 during field blanking and 0 elsewhere
H = 0 in SAV and 1 in EAV

Note 2: Protection bits P3-P0 are ignored by this product.

5.5 RGB 8bit Serial Video Format

5.5-1 Video Input Vertical Timing, RGB 8bit Serial Video Formats

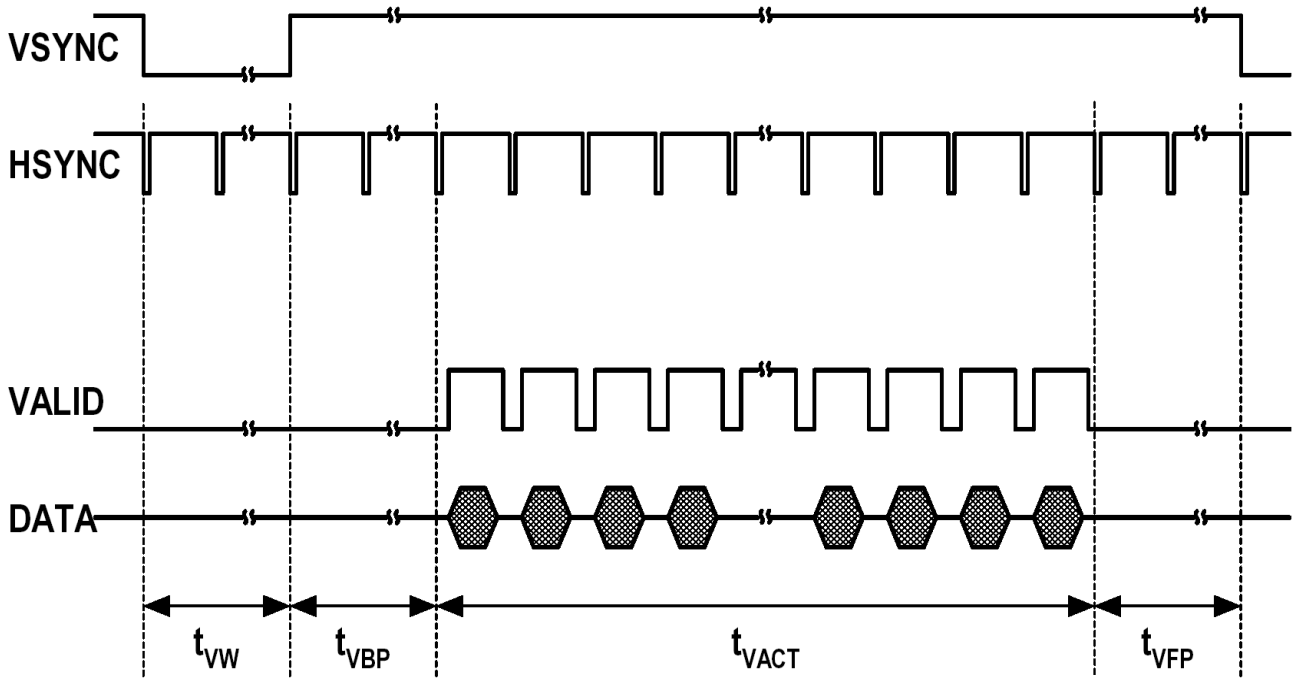


Fig9-1: RGB Serial Video input vertical timing

5.5-2 Video Input Horizontal Timing, RGB 8bit Serial Video Format

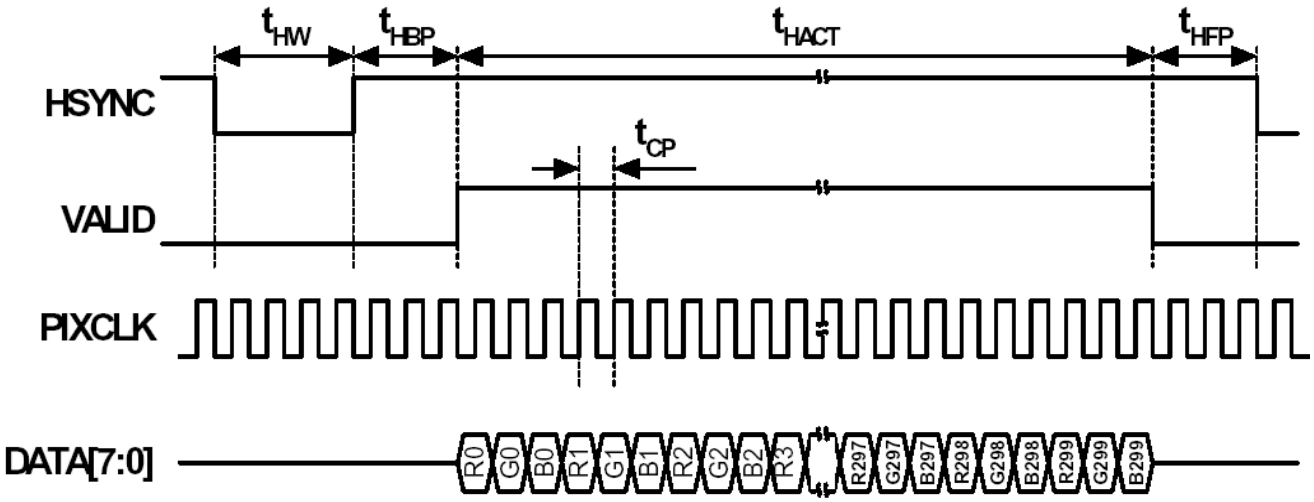


Fig9-2: RGB Serial Video input horizontal timing

Table10-1: AC Characteristics, RGB 8bit Serial 60Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	59	60	61	Hz
VSYNC, total lines	t_{VTOT} $t_{VBLK} + t_{VACT}$	252	262	384	Lines
VSYNC, active lines	t_{VACT}	224	224	240	Lines
VSYNC, blanking	t_{VBLK}= $t_{VFP} + t_{VW} + t_{VBP}$	12	22	44	Lines
VSYNC, front porch	t_{VFP}	3	3	25	Lines
VSYNC, pulse width	t_{VW}	3	3	25	Lines
VSYNC, back porch	t_{VBP}	6	6	38	Lines
HSYNC, total clocks	t_{HTOT} $t_{HBLK} + t_{HACT}$	1690	1716	1746	Clocks
HSYNC, active clocks	t_{HACT}	900	900	960	Clocks
HSYNC, blanking	t_{HBLK} $t_{HFP} + t_{HW} + t_{HBP}$	32	816	846	Clocks
HSYNC, front porch	t_{HFP}	14	572	602	Clocks
HSYNC, pulse width	t_{HW}	4	126	156	Clocks
HSYNC, back porch	t_{HBP}	14	118	688	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	1/4 t_{HTOT}	1/2 t_{HTOT}	3/4 t_{HTOT}	Clocks

Table10-2: AC Characteristics, RGB 8bit Serial 50Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	49	50	51	Hz
VSYNC, total lines	t_{VTOT} $t_{VBLK} + t_{VACT}$	288	312	384	Lines
VSYNC, active lines	t_{VACT}	224	224	240	Lines
VSYNC, blanking	t_{VBLK}= $t_{VFP} + t_{VW} + t_{VBP}$	48	88	94	Lines
VSYNC, front porch	t_{VFP}	3	19	73	Lines
VSYNC, pulse width	t_{VW}	3	3	73	Lines
VSYNC, back porch	t_{VBP}	6	66	88	Lines
HSYNC, total clocks	t_{HTOT} $t_{HBLK} + t_{HACT}$	1698	1728	1766	Clocks
HSYNC, active clocks	t_{HACT}	900	900	960	Clocks
HSYNC, blanking	t_{HBLK} $t_{HFP} + t_{HW} + t_{HBP}$	32	828	858	Clocks
HSYNC, front porch	t_{HFP}	14	564	602	Clocks
HSYNC, pulse width	t_{HW}	4	126	164	Clocks
HSYNC, back porch	t_{HBP}	14	138	716	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	1/4 t_{HTOT}	1/2 t_{HTOT}	3/4 t_{HTOT}	Clocks

5.5-3 RGB 8bit Serial Video Without VALID

When the SyncMode bits of the Video Configuration Register0 are programmed to "01", the product will ignore the VALID input pin and begin sampling video data after a specified delay from the assertion of HSYNC and VSYNC. The Vertical Field Offset Register, the Horizontal Valid Delay Register, and the Vertical Valid Delay Register are used to specify these delays. The values to program these register fields are as follows.

Table10-3: Register Values Enabling RGB Serial Video Without Valid

Register Field	Calculation	Unit
HVldDelay	$t_{HW} + t_{HBP}$ + (horizontal overscan delay) - 2	Clocks
VVldDelay	$t_{VW} + t_{VBP}$ + (vertical overscan delay)	Lines

5.6 Video Input Signal Timing Requirements

All video input signals must meet the timing requirements below.

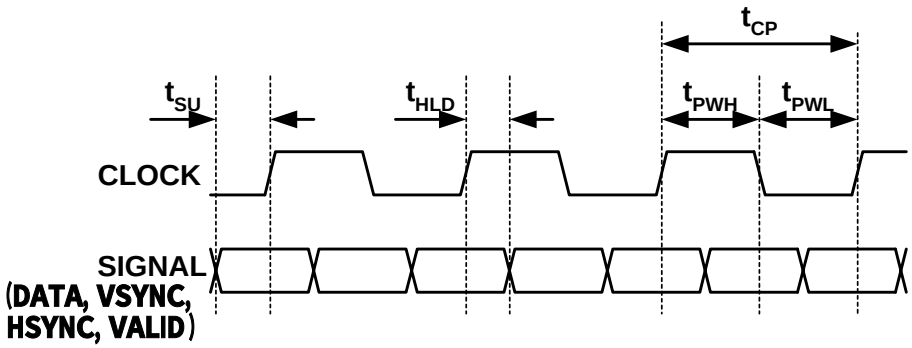


Fig10-1: Video Input Signal Timing

Table11: AC Characteristics, Video Input Signal Timing

Item	Symbol	Min	Typ	Max	Unit
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
CLOCK, pulse width high	t_{PWH}	45% t_{CP}	50% t_{CP}	55% t_{CP}	NA
CLOCK, pulse width low	t_{PWL}	45% t_{CP}	50% t_{CP}	55% t_{CP}	NA
DATA, VSYNC, HSYNC, VALID setup time	t_{SU}	5			ns
DATA, VSYNC, HSYNC, VALID, hold time	t_{HLD}	1			ns

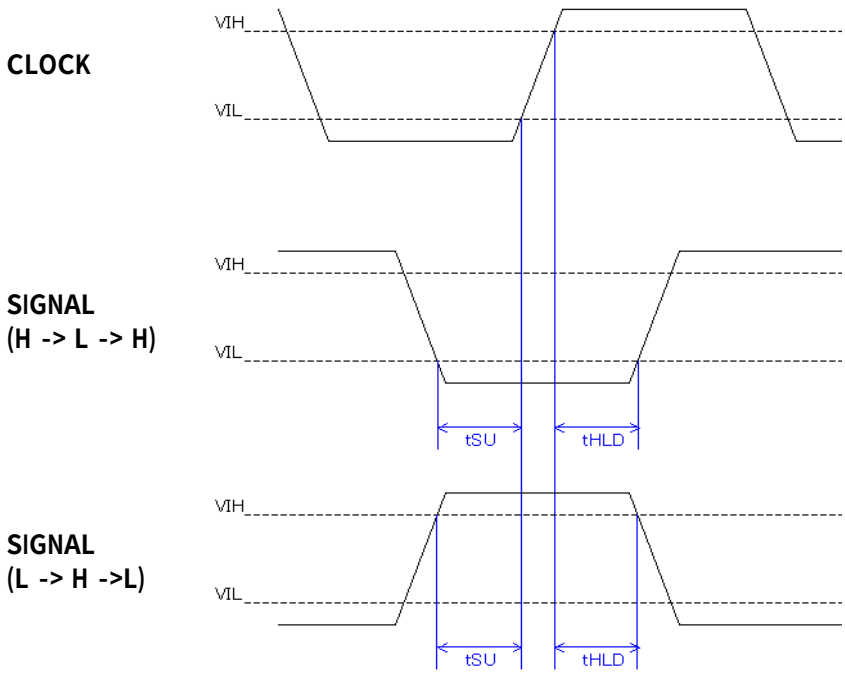


Fig10-2: setup and hold time definition

6.Serial Interface

6.1 Communication Specification

The serial interface signal timing reqirements are as follows.

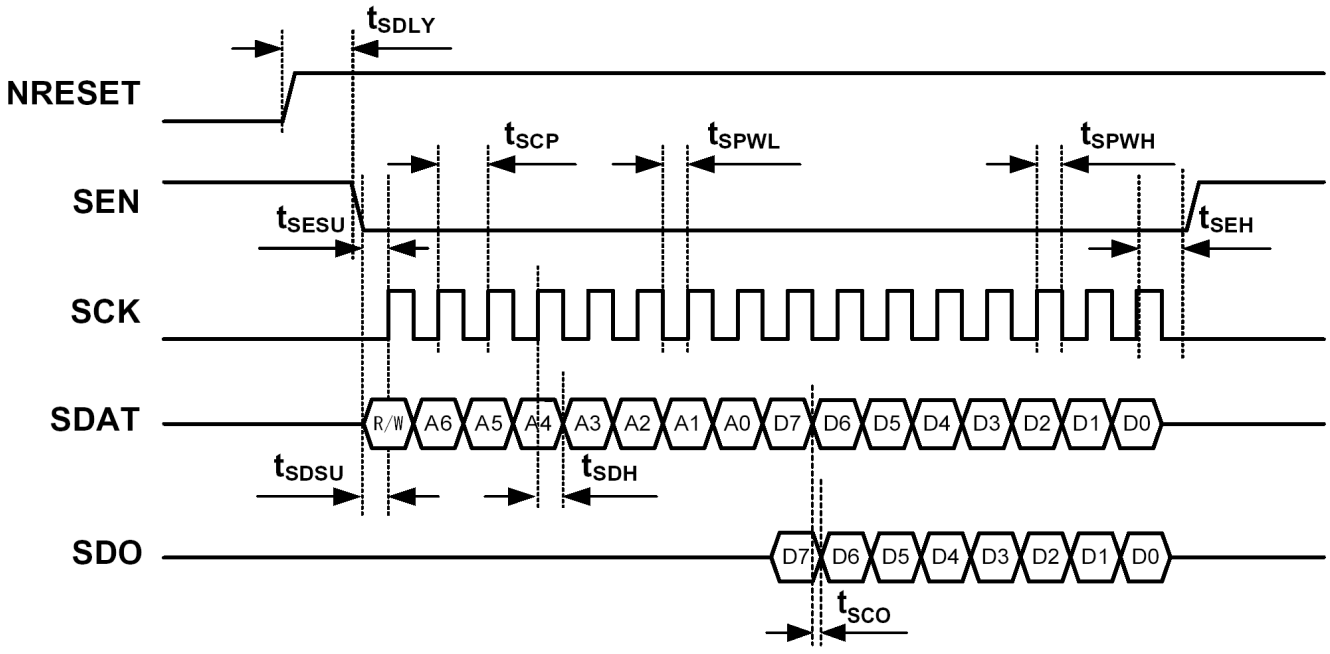


Fig11: Serial Interface Signal Timing

Table12: AC Characteristics, Serial Interface Signal Timing

Item	Symbol	Min	Typ	Max	Unit
Delay from reset to serial transfer	t_{SDLY}	8	-	-	ms
SCK, rate	$1/t_{SCP}$	100	400	800	KHz
CLOCK, pulse width high	t_{SPWH}	45% t_{SCP}	50% t_{SCP}	55% t_{SCP}	
CLOCK, pulse width low	t_{SPWL}	45% t_{SCP}	50% t_{SCP}	55% t_{SCP}	
SDAT, setup time	t_{SDSU}	150	-	-	ns
SDAT, hold time	t_{SDH}	150	-	-	ns
SDO, clock to out time	t_{SCO}	-	-	250	ns
SEN, setup time	t_{SESU}	150	-	-	ns
SEN, hold time	t_{SEH}	150	-	-	ns

6.2 Control Sequence Requirements

This product requires particular power-up and shutdown sequences which dictate the application and removal of control signals relative to the power supplies.

As specified in [4.4 Absolute Maximum Ratings], no input may exceed the VDD supply by more than 1.4V. It is therefore necessary to apply the VDD supply before any control signal and remove the control signals prior to the removal of the VDD supply. This requirement is due to the ESD protection diodes present on the input pins.

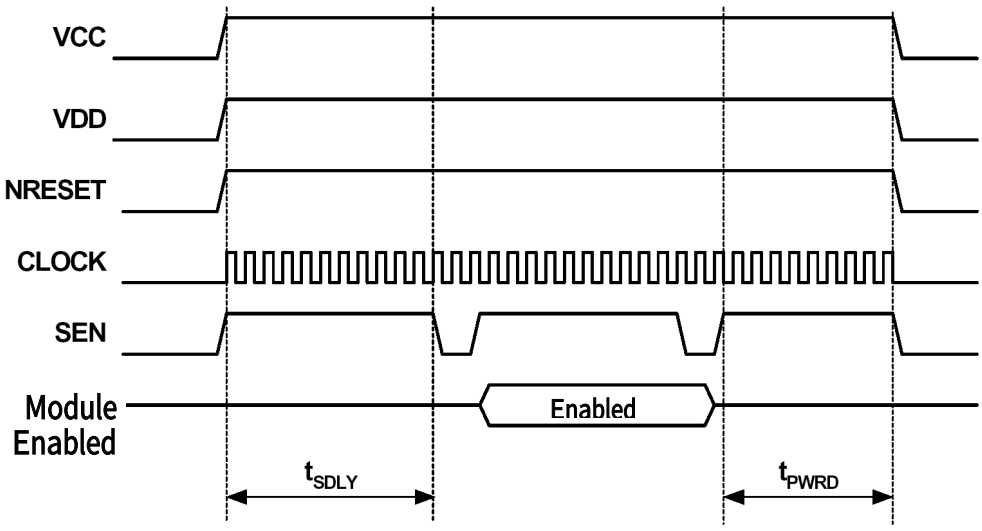
This product will load default register values from EEPROM after the VDD supply is present, the NRESET control signal has been set high, and the CLOCK input is toggling. During this process, the serial interface is ignored as indicated by the timing parameter tSDLY given in Table12.

This product is enabled by using the serial interface to set the NSleepMode bit of the Video Configuration Register 3. When the NSleepMode bit is cleared this product enters the sleep mode.

This product can be repeatedly enabled and disabled as desired. In the sleep mode, all programmed register values are maintained and the Display Module is ready for immediate use.

Once this product has been enabled, This product must be disabled using the serial interface, for a time period tPWRD prior to the removal of any power supply, during which time CLOCK and NRESET inputs must be present. The required control sequence of the product is shown in Fig.12 and Table12.

If it is desired to further reduce sleep mode power, the CLOCK input can be stopped after a time period tPWRD after the product has been disabled. As soon the CLOCK input is restored, This product is ready to begin a serial transfer to be enabled.



Symbol	Min
t_{PWRD}	1500us

Fig12: Control Sequence

6.3 Power Supply Requirements

This product has up to 2.2uF of bulk capacitance connected to the VDD supply. Inrush current during the application of the VDD supply is determined by the impedance of the source supply.

This product will exhibit large peak current sinks on the VDD power supply relative to the average currents specified in [4.5 Operating Conditions]. To limit these peak currents and ensure that the VDD supply voltage is maintained within specifications, it is required that a minimum of 22uF of bulk capacitance be connected to the VDD power supply and located adjacent to connector.

The voltage requirements specified in [4.5 Operating Conditions] for the VDD and VCC power supplies must be maintained or an internal power-on-reset could result. If an internal reset occurs, power sequencing from the initial start condition, as stated, above is required. If an internal reset occurs after the initial power up sequence any previous data programmed into the product are erased and the display will re-enter sleep mode. After such an occurrence, all configuration registers are set to default values within the display requiring the user to reprogram the display.

7. Configuration Registers

1.Display Configuration Register

Register index : 00h

Bit	7	6	5	4	3	2	1	0
Meaning	Res							
Example value	01h							

This register must be set to 01h for proper operation.
* "Res" means "Reserved."

2.Video Configuration Register 0

Register index : 01h

Bit	7	6	5	4	3	2	1	0
Meaning	Res	SyncMode		DitherMode		DataMode		
Example value	0	0	0	1	0	1	0	1

Reserved ([7]): Must be set to 0.

SyncMode: 00=Use Inputs for video timing
01=Use HSync and VSync inputs, Valid timing specified from Valid delay registers
10= Reserved
11= Use 656 SAV/EAV control codes

DitherMode: 00=No Dither, Input data rounded to 6-bit values
01=1/2 bit spatial, 1/4 bit temporal
10=1/2 bit temporal, 1/4 bit spatial
11=1/2 bit spatial

DataMode: 101 = CCIR 601/656
000 = RGB serial video data

3.Video Configuration Register 1

Register index : 02h

Bit	7	6	5	4	3	2	1	0
Meaning	Vpol	Hpol	ValidPol	Arctic ModeEn	Res	Res	VideoMask	
Example value	1	1	0	0	0	0	0	0

Vpol (Vertical sync polarity) : 0=Active High, 1=Active Low

Hpol (Horizontal sync polarity) : 0=Active High, 1=Active Low

ValidPol (Valid input polarity) : 0=Active High, 1=Active Low

ArcticModeEn (Enable Arctic mode) : 0=Disable, 1=Enable

Reserved ([3:2]): Must be set to 00.

VideoMask (Mask LSB data bits) : 01=Input video data is considered 7bits ([7:1] of input video data)
11=Input video data is considered 6bits ([7:2] of input video data)

4.LED Brightness Register

Register index : 03h

Bit	7	6	5	4	3	2	1	0
Meaning	Res	Res	Brightness Ratio					
Example value	1	1	3Fh					

Reserved ([7:6]): Must be set to 11.

Brightness Ratio : These bits determine the duty cycle for driving the illumination LEDs.
3Fh=The duty cycle is 64/64(=100%) and the maximum brightness results.
00h=The duty cycle is 1/64 and the minimum brightness results.

5.Vertical Field Offset Register

Register index : 04h

Bit	7	6	5	4	3	2	1	0
Meaning	VVldDelOffset[3:0] (-8 to +7)				VertInterpMode		HVldDelay[9:8]	
Example value	0h				1	0	0	0

VVldDelOffset : Offset of even field Valid delay.

VertInterpMode : 00=No Vertical Interpolation
01=Odd lines not interpolated, Even lines interpolated up 1/2line.
10=Odd lines interpolated down 1/4line, Even lines interpolated up 1/4line.

HVldDelay[9:8] : The most significant two bits of the horizontal valid delay setting.

6.Horizontal Valid Delay Register

Register index : 05h

Bit	7	6	5	4	3	2	1	0
Meaning	HVldDelay[7:0]							
Example value	00h							

HVldDelay: Horizontal sampling delay.

The meaning of this register is determined by the value programmed for SyncMode in the Video Configuration 0 register.

SyncMode	HVldDelay Meaning
00	Number of clocks to delay sampling of video data after the assertion of VALID
01	Number of clocks minus two to delay sampling of video data after the assertion of HSYNC
11	Number of clocks to delay sampling of video after SAV

7.Video Configuration Register 3

Register index : 06h

Bit	7	6	5	4	3	2	1	0
Meaning	Res	VFlip	HFlip	Res	NSleep Mode	Res		
Example value	0	0	0	0	0	0	0	0

Reserved ([7], [4], [2:0]): Must be set to 0 each.

Vflip (Flip display vertically) : 0=Don't flip, 1=Flip

Hflip (Flip display horizontally) : 0=Don't flip, 1=Flip

NSleepMode : 0=Power Save Mode, 1=Normal Mode

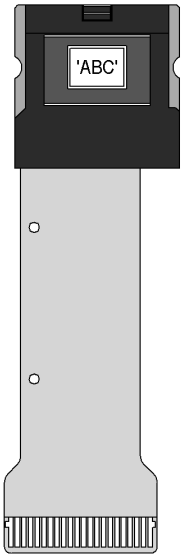


Fig13: Display Orientation with VFlip=0 and HFlip=0

8.Scaling Coefficient Upper Register

Register index : 07h

Bit	7	6	5	4	3	2	1	0
Meaning	Res	Res	Res	HScale Cycle[8]	VScaleStep[9:8]		HScaleStep[9:8]	
Example value	0	0	0	0	0	1	0	0

Reserved ([7:5]): Must be set to 000.

HScaleCycle[8] : Most significant bit of the HScaleCycle value.

VScaleStep[9:8] : Most significant two bits of the VScaleStep value.

HScaleStep[9:8] : Most significant two bits of the HScaleStep value.

9.Horizontal Scaling Coefficient Register

Register index : 08h

Bit	7	6	5	4	3	2	1	0
Meaning	HScaleStep[7:0]							
Example value	D6h							

HScaleStep : Horizontal scaling coefficient.

10.Horizontal Scaling Cycle Register

Register index : 09h

Bit	7	6	5	4	3	2	1	0
Meaning	HScaleCycle[7:0]							
Example value	05h							

HScaleCycle : Horizontal scaling repeat count.

11.Vertical Scaling Coefficient Register

Register index : 0Ah

Bit	7	6	5	4	3	2	1	0
Meaning	VScaleStep[7:0]							
Example value	DEh							

VScaleStep : Vertical Scaling Coefficient.

12.Vertical Scaling Cycle Register

Register index : 0Bh

Bit	7	6	5	4	3	2	1	0
Meaning	VScaleCycle[7:0]							
Example value	0Eh							

VScaleCycle : Vertical scaling repeat count.

13.Vertical Valid Delay Register

Register index : 0Ch

Bit	7	6	5	4	3	2	1	0
Meaning	VVldDelay[7:0]							
Example value	01h							

VVldDelay : Vertical Valid Delay.

The meaning of this register is determined by the value programmed for SyncMode in the Video Configuration 0 register.

SyncMode	VertValidDel Meaning
00	Number of VALID lines to delay sampling of video
01	Number of HSYNC periods to delay sampling of video data after the assertion of VSYNC
11	Number of EAV codes to delay sampling of video after clearing the VBlank bit

14.Cinema Mode Register

Register index : 0Dh

Bit	7	6	5	4	3	2	1	0
Meaning	Res				CinemaLines			
Example value	0h				0h			

Reserved ([7:4]): Must be set to 0h.

CinemaLines : Black lines added to the top and bottom of the display in Cinema or widescreen mode. The number of lines added will be 2x the CinemaLines register setting at both the top and bottom of the display. For approximately 16:9 aspect ratio, CinemaLines would be set to 0Eh, resulting in 168 active display lines centered vertically in the display.

Note: CinemaLines register is not independent of the vertical scaling. Vertical scaling coefficients should be re-adjusted if CinemaLines are set.

15.Gamma Register

Register index : 0Eh

Bit	7	6	5	4	3	2	1	0
Meaning	Res				GammaValue			
Example value	0h				9h			

Reserved ([7:4]): Must be set to 0h.

GammaValue : The gamma value selected from the following table.

GammaValue	Display Gamma	GammaValue	Display Gamma
0h	1.0	8h	2.0
1h	1.2	9h	2.1
2h	1.4	Ah	2.2
3h	1.5	Bh	2.3
4h	1.6	Ch	2.4
5h	1.7	Dh	2.6
6h	1.8	Eh	2.8
7h	1.9	Fh	3.0

Note: The display brightness is not independent of Display Gamma, the maximum brightness will be reduced as the gamma of the display is increased.

16.Color Space Gain Registers

Register index : 0Fh-17h

Index	Bit	7	6	5	4	3	2	1	0
0Fh	Meaning	ColorSpace11 (-128 to +127)							
	Example value	00h							
10h	Meaning	ColorSpace12 (-128 to +127)							
	Example value	00h							
11h	Meaning	ColorSpace13 (-128 to +127)							
	Example value	00h							
12h	Meaning	ColorSpace21 (-128 to +127)							
	Example value	00h							
13h	Meaning	ColorSpace22 (-128 to +127)							
	Example value	00h							
14h	Meaning	ColorSpace23 (-128 to +127)							
	Example value	00h							
15h	Meaning	ColorSpace31 (-128 to +127)							
	Example value	00h							
16h	Meaning	ColorSpace32 (-128 to +127)							
	Example value	00h							
17h	Meaning	ColorSpace33 (-128 to +127)							
	Example value	00h							

ColorSpace# : Parameters for color space settings.
Explained in the item of Color Space Offset Registers.

17.Hardware Configuration Register

Register index : 18h

Bit	7	6	5	4	3	2	1	0
Meaning	ProductCode							
Example value	-							

ProductCode : Product management code for CITIZEN FINETECH MIYOTA

* ProductCode is used for recognition in the production line. Written value will be ignored.

18.Color Space Offset Registers

Register index : 19h-1Bh

Index	Bit	7	6	5	4	3	2	1	0
19h	Meaning	ColorOffset1 (-128 to +127)							
	Example value	00h							
1Ah	Meaning	ColorOffset2 (-128 to +127)							
	Example value	00h							
1Bh	Meaning	ColorOffset3 (-128 to +127)							
	Example value	00h							

ColorOffset# : Parameters for color space settings.

* The color space may be set to standard RGB color spaces. The scaling or offset of each color can be changed independently for the optional color space scaling or white point adjustment. Refer to the below formula when setting Color Space Gain & Offset Registers.

$$\begin{bmatrix} R_O \\ G_O \\ B_O \end{bmatrix} = \frac{1}{128} \begin{bmatrix} 128+cs_{11} & 0+cs_{12} & 175+cs_{13} \\ 128+cs_{21} & -42+cs_{22} & -90+cs_{23} \\ 128+cs_{31} & 222+cs_{32} & 0+cs_{33} \end{bmatrix} \bullet \begin{bmatrix} Y_I + O_1 \\ Cb_I - 128 + O_2 \\ Cr_I - 128 + O_3 \end{bmatrix}$$

Fig14: Color Space Gain & Offset selection figure

19.Minimum Vertical Frequency Register

Register index : 1Ch

Bit	7	6	5	4	3	2	1	0
Meaning	Res	MinVFreq[6:0]						
Example value	0	2Fh						

Reserved: Must be set to 0.

MinVFreq : The minimum vertical frequency, in Hz.

20.Maximum Vertical Frequency Register

Register index : 1Dh

Bit	7	6	5	4	3	2	1	0
Meaning	Res	MaxVFreq[6:0]						
Example value	0	3Fh						

Reserved: Must be set to 0.

MaxVFreq : The maximum vertical frequency, in Hz.

8. Display Characteristics

8.1 Panel Optical Characteristics

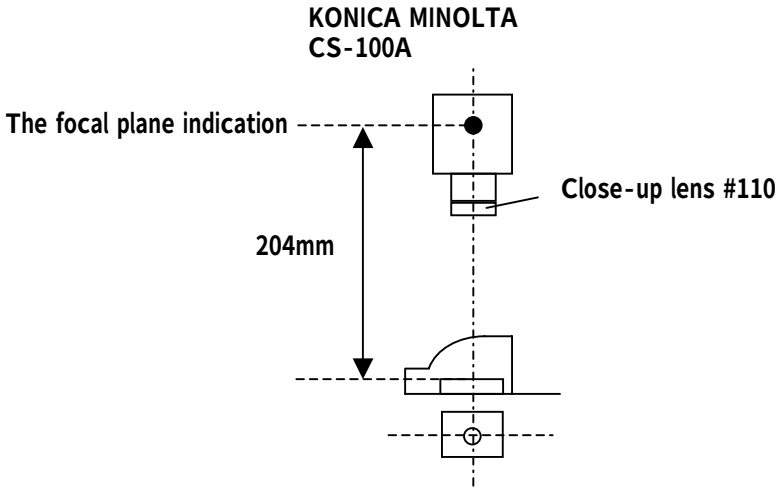
Table13: Optical Characteristics

Item	Min.	Typ.	Max.	Unit
Maximum brightness (White)	225	250	275	cd/m^2
Contrast Ratio (White:Black)	60:1	80:1		-
Color Temperature (White)	6,000	6,500	7,000	deg.K

Measuring condition :

Ta=25deg.C, VDD and VCC voltages are typical values of [4.5 Operating Conditions], Brightness Ratio register is set to maximum (100%), input video data are CCIR-601 typical values at 60 Hz NTSC, gamma correction is 2.1, displayed image is flat field pattern of white /black.

Optical measuring system is as below.



Measured point is the center of display area and has approx. 1.3mm diameter.

Fig15: Optical measuring system

8.2 Visual Specifications

Table14: Display area defects

Defect	Size (Average) [Unit : Pixel]	Quantity [Unit : pcs]	
		Bright /White	Dark /Black
Line Out	1 pixel line (line/colmun)	0	0
Large Spot	2 > S > 1	1	1
Medium Spot	1 >= S > 1/2	3	3
Small Spot	1/2 >= S	No clumping	

Measuring condition : viewing through the x18 lens, focusing on the displayed image.

Display area is defined as below.

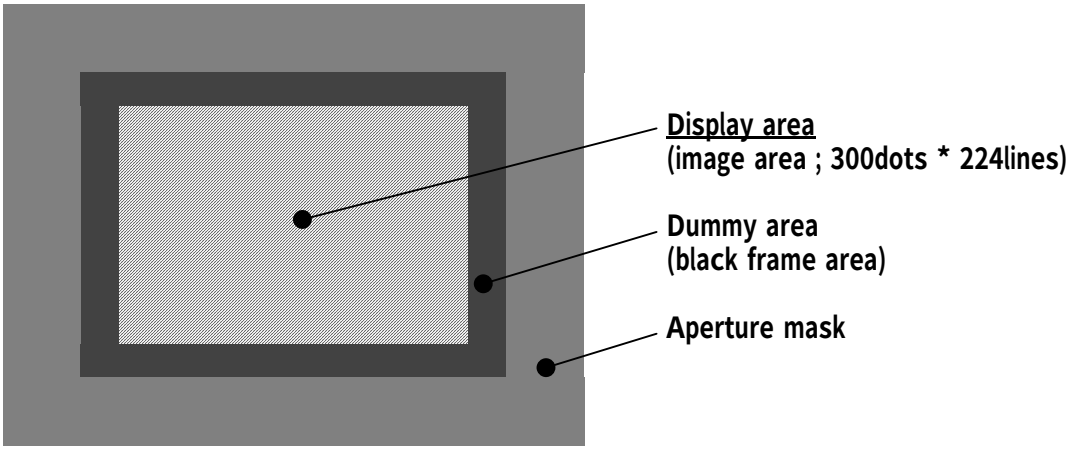


Fig16: Display area

9. Reliability Test

Table15: Reliability test

Test	Test condition	Spec.
High Temperature Storage Test	Ta=83deg.C 240hrs	Should not have any electrical or mechanical damage which affects proper operation. *Before judge, leave a tested product at room temperature for one hour after test.
Low Temperature Storage Test	Ta=-30deg.C 240hrs	
High Temperature humidity Storage Test	Ta=60deg.C Ha=90%R.H. 240hrs	
High Temperature Operation	Tp=65deg.C VDD=2.5V VCC=5V 240hrs	
Low Temperature Operation	Ta=-10°C VDD=2.5V VCC=5V 240hrs	
Air to Air Thermal Shock	Ta=-30°C/80°C strage time: 30min/30min 10 cycle	
ESD test (Machine model)	C=200pF,R=0ohm,V=+/-200V. Test between VDD/GND and each signal pin, 3times each.	Should not have any electrical or mechanical damage which affects proper operation.
Vibration test (in package)	Acceleration = 19.6m/s2 f=10-50Hz X, Y, Z 3 direction each 30min	

10. Environmental Standards

This product complies to RoHS(2002/95/EC).

11. Packaging

TBD

12. General Handling

• Cleanliness

It is recommended that the product is handled in a class 10,000 clean-room or under a positive pressure, laminar flow bench filtering to 0.5um.

• Electro Static Discharge (ESD)

All clothing of personnel working with the product should be static-free and non-chargeable. Display-handling personnel should always be fully grounded and follow standard ESD procedures. All work areas must have grounded, conductive flooring (or mats) and a grounded, conductive work surface. Personnel handling display components should wear a grounding heel strap or a grounded, conductive wristband.

• Radiation

Limit the exposure of the product to unfiltered ultraviolet (UV) radiation. Long periods of exposure may degrade the product and its performance and have negative effects on the device materials.

• Mechanical

At no time should the product be disassembled for cleaning of the integrated microdisplay module. This product does not have hermiticity. In case of strong air blow cleaning very close to the product, particles may intrude into the product. Cleanroom procedures should be observed at all times to prevent dust contamination or smudges. Handle the flex connection by the edge of the flex. Take care not to touch exposed traces with unprotected hands.

• Environmental

During either integration or storage, do not allow any moisture or solvent to contact the polarizing film and do not allow condensation to form on the display module. This will maintain a clean optical film surface by avoiding contamination from residue left from evaporation of the moisture of solvent. Be sure to follow the specified storage temperatures for the module of -30deg.C to 83deg.C during assembly, storage and shipping.

• Shipping and Packing

The products arrive in a custom molded ESD safe tray with a static protective bag. These trays were sealed prior to leaving the manufacturing facility in a Class 10,000 clean room. To prevent dust and particulate contamination, it is recommended to open the seal on these trays in a Class 10,000 or equivalent room for incoming inspection or manufacturing integration. Do not stack trays higher than 15, or place other heavy material on the trays to prevent damage to the sensitive optical components on the display.

13. Others

When the issue that is not described in this document arises, the both parties will mutually solve it.