OV5640 Camera Board (C) User Manual

OVERVIEW

The module OV5640 Camera Board (A) contains is a video camera based on video sensor OV5640 (CMOS), takes 5 megapixel image in QSXGA mode (2592x1944), uses DVP data interface and SCCB control interface. It supports RGB565\RGB555\RGB444, YUV(422/420), YCbCr422 and JPEG pixel/image formats. The module can adjust white balance, saturation, hue, sharpness, and gamma correction. The resolution and frame rate are adjustable as well.

FEATURES

- Number of pixels: 5M
- Highest resolution: 2592x1944
- Video sensor: OV5640
    - uses 1.4 x 1.4 um pixels OmniBSI technology, high sensitivity, low crosstalk and noise
    - supports automatic exposure, white balance, elimination of light stripes, black level calibration, band pass filter, and other automatic functions
    - supports adjustment of saturation, hue, gamma correction, sharpness, and lens calibration, etc
    - supports zoom, window parallel translation and window settings
- Camera:
    - CCD size: 1/4 inches
    - Aperture (F): 3.0
    - Focal Length: 3.8mm
    - View angle (diagonal): 60 degrees
- Output modes:
    - YUV(422/420)/YCbCr422
    - RGB565/555/444

  - CCIR656
  - RAW RGB
  - Compressed Data
- Operating voltage: 3.3V
- Control interface: SCCB (compatible with I2C)
- Data interface: DVP 8-bits
- Size: 35.70 mm × 23.90 mm

INTERFACE DESCRIPTION

OV5640 Camera Board (B)	**Pin descriptions**
3.3V	Power input 3.3V
GND	Ground
SIOC	SCCB clock signal
SIOD	SCCB data signal
VSYNC	Frame synchronization signal
HREF	Line synchronization signal
PCLK	Pixel clock
XCLK	External oscillator clock input
D0 ~ D7	Pixel data output
RST	Reset (active low)
PWDN	Save energy mode (high effective)

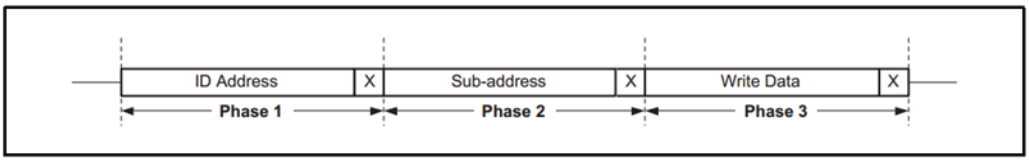
SCCB CONTROL INTERFACE

SCCB (Serial Camera Control Bus) is a serial control bus of a camera. SCCB is similar to I2C, because start and stop signals are same as in I2C, SCCB defines basic data transfer unit (phase), each phase of data transfer takes one byte. SCCB contains only three kinds of transmission cycle:

1) 3-phase write transmission cycle

3-phase cycle includes: device address, register address, data

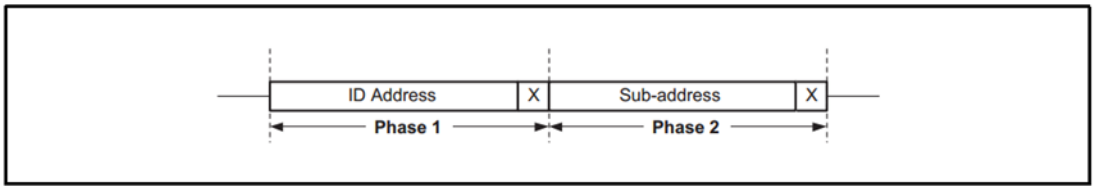
Figure 3-5 3-Phase Write Transmission Cycle



2) 2-phase write transmission cycle

2-phase cycle includes: device address, register address

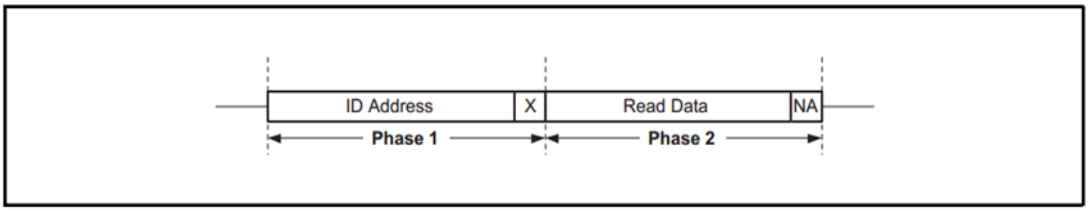
Figure 3-6 2-Phase Write Transmission Cycle



3) 2-phase write transmission cycle

2-phase cycle includes: device address, data

Figure 3-7 2-Phase Read Transmission Cycle



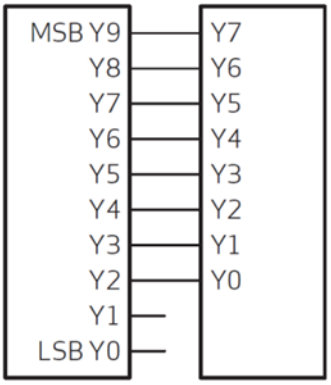
While writing: use 3-phase write cycle directly

While Reading: first use 2-phase write cycle, then use 2-phase read cycle

More detailed information about SCCB protocol see in “OmniVision Technologies Serial Camera Control Bus (SCCB) Specification”

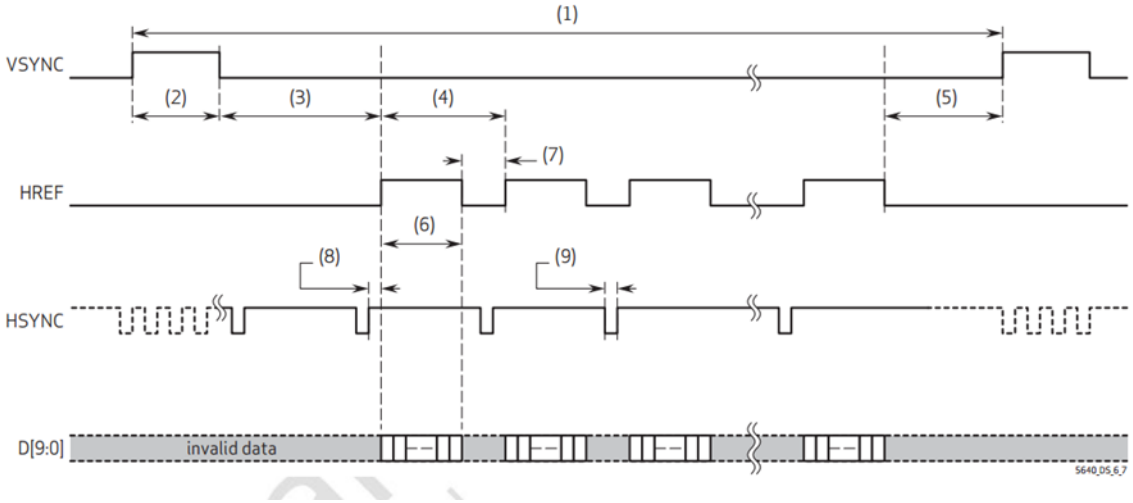
DVP DATA INTERFACE

The module OV5640 uses DVP data transfer interface, because camera driver interface (DCMI) in our STM32F407\429\746 boards only supports DVP. OV5640 sensor has 10-bits DVP interface, but we usually use 8-bits data processing. For example, in the following picture there are: OV5640 8 highest bits at the left side connected to 8 bits of STM32F407\429\746 board at the right site.



DVP interface timing diagram:

figure 6-7 DVP timing diagram



DCMI INTERFACE

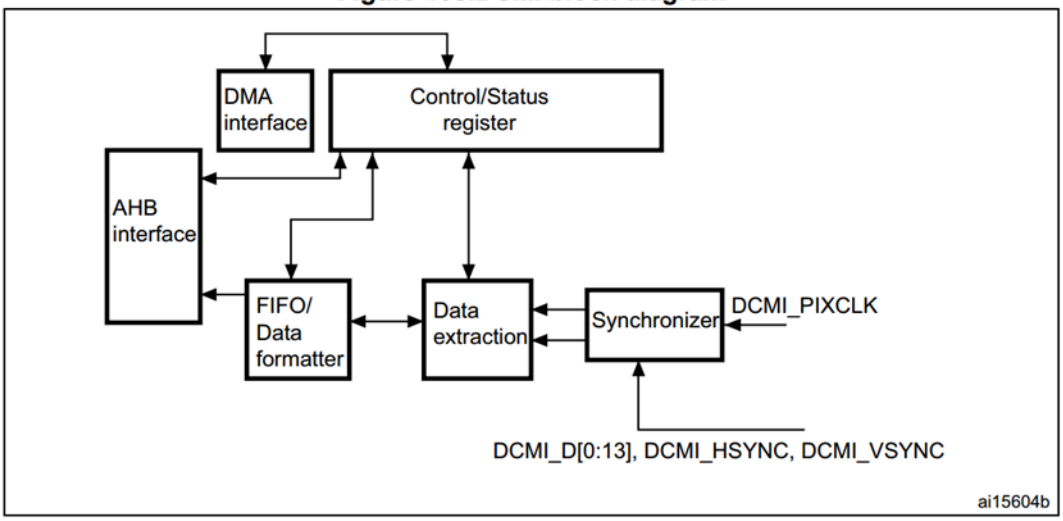
DCMI (Digital camera media interface) is digital camera interface, integrated into STM32F4xx, F7xx series of MCU. DCMI is synchronous parallel interface, capable receive 8-, 10-, 12- or 14-bits data stream from CMOS camera module. It can support various data modes: YCbCr422, RGB565 and compressed data (JPEG).

DCMI interface can support input data stream speed up to 54 MB/s. The interface contains 14 data pins (D13-D0) and pixel clock pin (PIXCLK). The pixel clock polarity can be programmed

and therefore data can be caught at the rising or falling front. These data come to 32-bit register (DCMI_DR), and then are transmitted via DMA. The image buffer is controlled by DMA, not by camera interface. Data received from camera can be restored to original image lines of frames (YUB/RGB modes) or series of JPEG files. To enable receiving JPEG images the JPEG bit (the 3rd DCMI_CR bit) must be set to 1. Data stream can be synchronized by HSYNC (horizontal synchronization) signal and VSYNC (vertical synchronization) signal, otherwise by synchronization signals embedded into the data stream.

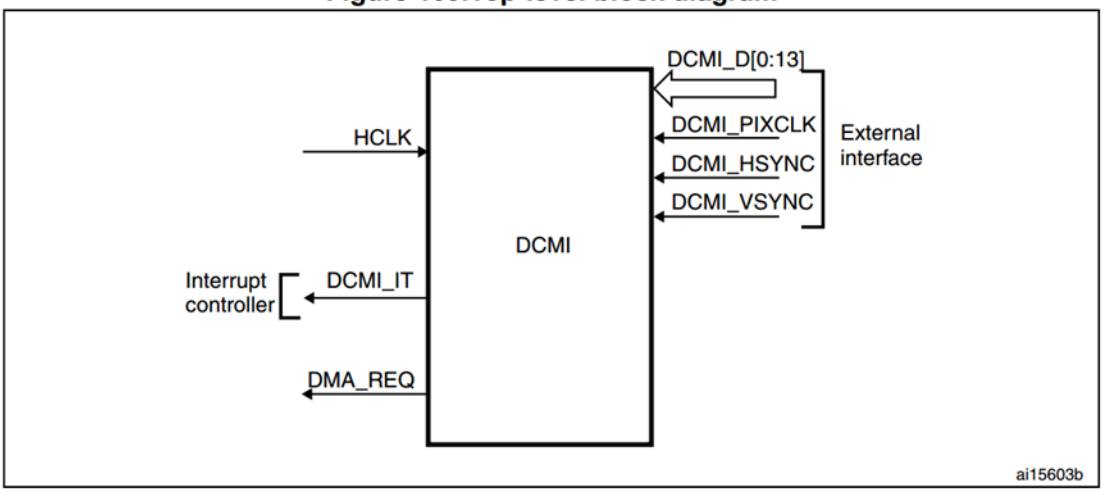
DCMI block diagram:

Figure 108.DCMI block diagram



Top-level block diagram:

Figure 109.Top-level block diagram



The DMA interface active when the CAPTURE bit of DCMI_CR is set to 1. Every time the camera receive full 32-bits block will trigger a DMI request.

More detailed information about SCCB protocol see in datasheet

USAGE DESCRIPTION

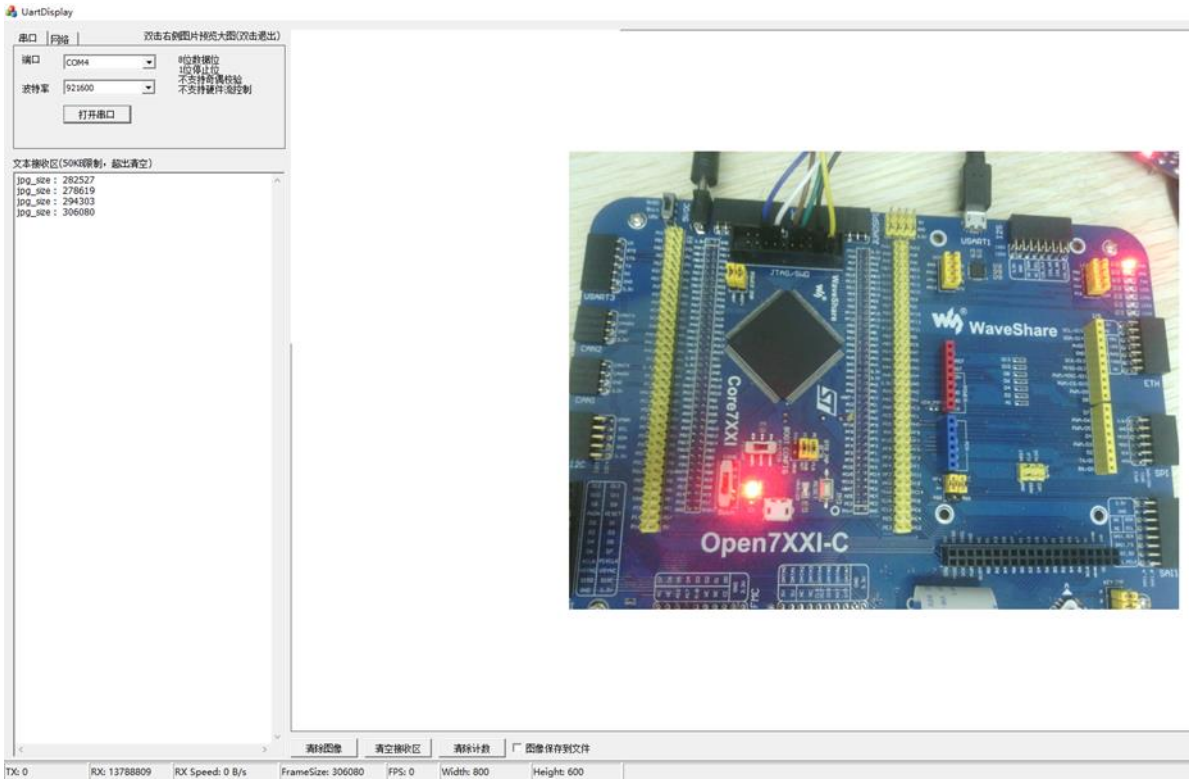
This module provides STM32F407\429\746 routines, here are demonstration examples for Waveshare Open746I-C development board:

1. Connect the module to DCMI port of the development board, connect USB-to-serial adapter to USART1 serial port on the board and to USB port on computer.

2. Open UartDisplay (camera data receiving software) on your computer, set number of port and its rate 921600, and the open the port.

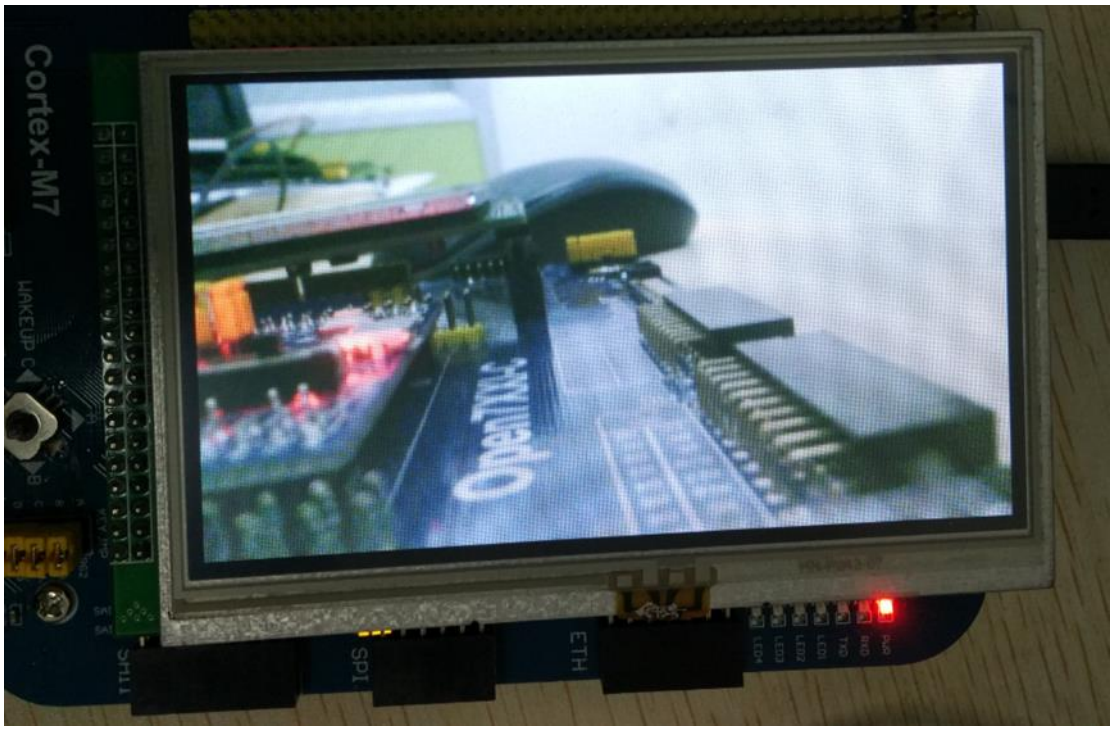
3. Download the program into the board, push RESET button and after some initialization period it shows following data:

4. Push WAKE UP button and the board will start to sent continuously JPEG images via serial port and UartDisplay will show them.

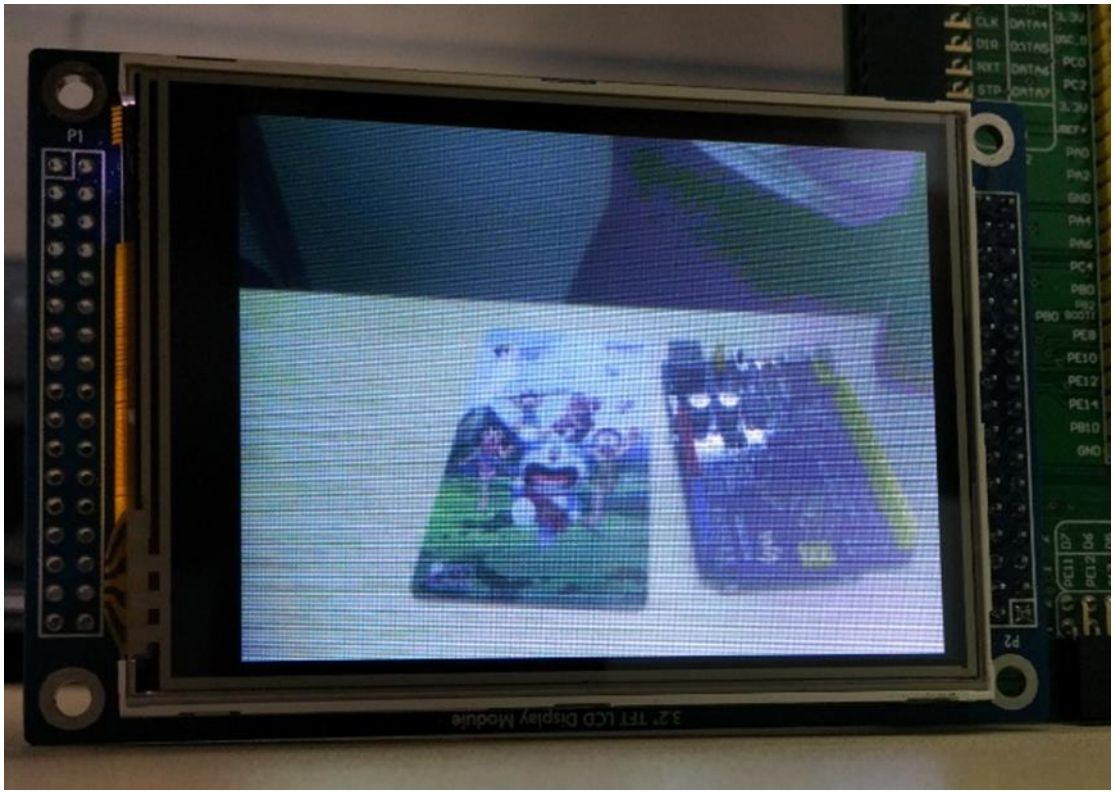


5. Push middle key of the board's joystick and OV5640 module will keep image on LCD screen in RGB565 mode continuously.

Open746I-C+7inch LCD



Open746I-C+4.3inch LCD



Open407V-C+3.2inch LCD