Graphenea

GFAB Services

Guidelines and design rules
Process Flow #3 High-K Metal Gate (HKMG)

The Process Flow #3 (PF3) is the platform to manufacture graphene-based devices which are gated through a High-K dielectric. It allows for graphene patterning for channel definition, metallization for S/D contact definition, gate dielectric deposition and metal gate definition. We can tailor the thickness and material for the S/D and gate contacts, as well as the gate dielectric thickness. The HKMG can be produced in a back-gate scheme (PF3A) or in a top-gate scheme (PF3B).
The present document describes the requirements and tolerances that need to be met within the GFAB service for a successful manufacture.

Process details and materials

- Graphene patterning
- Graphenea's Au contacts (50 nm)

- Optional wetting layers: Ti, Ni, Cr.
- Optional contacts material: Al, Ni.
- Thickness range: 10-80 nm

PF3A: Back-gate

- Dielectric material: Al_2O_3
- Min. Gate dielectric thickness (EOT): 5nm
- Max. Gate dielectric thickness (EOT): 150nm
- Thickness accuracy: +/- 1 nm
- Via opening for back-gate contacts

PF3B: Top-gate

- Dielectric material: Al_2O_3
- Min. Gate dielectric thickness (EOT): 20nm
- Max. Gate dielectric thickness (EOT): 150nm
- Thickness accuracy: +/- 1 nm
- Via opening for S/D contacts

Design Rules

The layout can be prepared by the customer or by Graphenea under request (a design fee will be charged). Failure to adhere to the following design rules may result in unsuccessful GFET fabrication, a reduction in yield or in reduced device performance.

Alignment marks willl be added by Graphenea after the rest of the layout has been fixed. The customer can include their own alignment marks for further processing.

Designs must be approved by both the client and Graphenea before mask designs are submitted for manufacture (mask tapeout)

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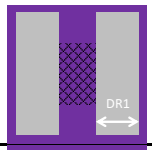
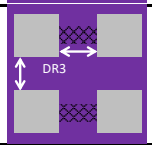
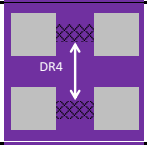
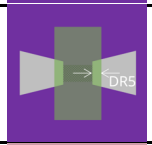
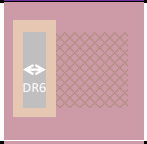
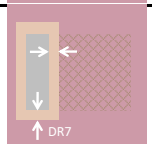
DR1	Minimum feature size – metal	5 µm	
DR2	Minimum feature size – graphene	10 µm	
DR3	Minimum feature separation – metal	10 µm	
DR4	Minimum feature separation - graphene	5 µm	
DR5	Minimum contact overlap between backgate and S/D metal	10 µm	
DR6	Minimum backgate via opening size – metal	5 µm	
DR7	Minimum backgate via opening to metal edge distance	10 µm	

Substrate Requirements

The substrate should be compatible with the various microfabrication processes involved in the GFET process. These include the following:

1. Compatible with solvents including acetone, dimethyl sulfoxide, isopropanol, and water
2. Compatible with developers based on tetramethylammonium hydroxide or buffered sodium hydroxide
3. Compatible with annealing temperatures of 300º C in an inert environment
4. Compatible with baking temperatures on a hotplate of up to 200º C in air
5. Compatible with exposure to oxygen plasma

Quality control

We carry out several quality checkpoints with different techniques, such as optical microscopy, Raman, AFM and electrical measurements (field-effect mobility, Dirac point and hysteresis).

We set the following thresholds to define a successful run.

AFM roughness

- RMS roughness < 1.5 nm
- Ra roughness < 1.0 nm

Raman

- I(G/2D) < 0.5
- Pos(G) < 1600 cm^{-1}
- FWHM(2D) < 45 cm^{-1}

Carrier transport

- Mobility within aspect ratio specifications.
- Dirac point equivalent to < 5 V in EOT=5nm
- Hysteresis < 20 V @10 mV/s

We set the following thresholds to define a successful die

Optical microscopy

- Channel integrity/coverage > 95%
- Device yield within die > 75%

We provide the QC summary of your run with the most relevant information.

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Aspect ratio considerations

We strongly recommend you to adhere to the aspect ratio guidelines to enhance or worsen the mobility of your device. Deviations from these aspect ratios can result in anomalous mobilities.

Device width (µm)	L/W
<20 µm	>4
20-50	>2
>100	>1

Device architecture