Graphenea

GFAB Services

Guidelines and design rules
Process Flow #1

The Process Flow #1 (PF1) is the platform to manufacture basic, general purpose graphene-based devices. It allows for graphene patterning for channel definition and metallization for S/D contact definition. We can also tailor the thickness and material for the S/D contacts if needed.
The present document describes the options, requirements and tolerances that need to be met within the GFAB service for a successful job manufacture.

Process details and materials

- Graphene patterning
- Graphenea's Au contacts (50 nm)

- Optional wetting layers: Ti, Ni, Cr (from 2 up to 15 nm)
- Optional contacts material: Al, Ni (from 5 up to 75 nm)
- Thickness accuracy: +/- 1 nm

- Substrate: p-doped Si/SiO_2 (90nm)
- Optional substrates: glass, quartz and SiNx.

Custom substrate requirements

We have expertise manufacturing graphene-based devices on many substrates, including nitrides, III-V's and II-VI's. You can send us your custom substrate to have graphene devices manufactured; this custom substrate can be pre-patterned with certain structures which we can align with. The substrate should be compatible with the various microfabrication processes involved in the GFET process. These include the following:

1. Compatible with solvents including acetone, dimethyl sulfoxide, isopropanol, and DI-water
2. Compatible with strongly alkaline solutions (pH>13)
3. Compatible with annealing temperatures of 300º C in an inert environment
4. Compatible with baking temperatures on a hotplate of up to 200º C in air
5. Compatible with exposure to plasma gas

Please note that certain QC metrics may not be carried out and provided due to incompatibilities with the device architecture and/or the custom substrate

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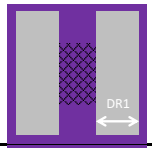
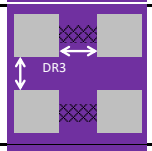
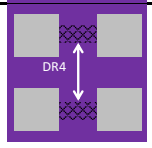
Tolerances and architecture

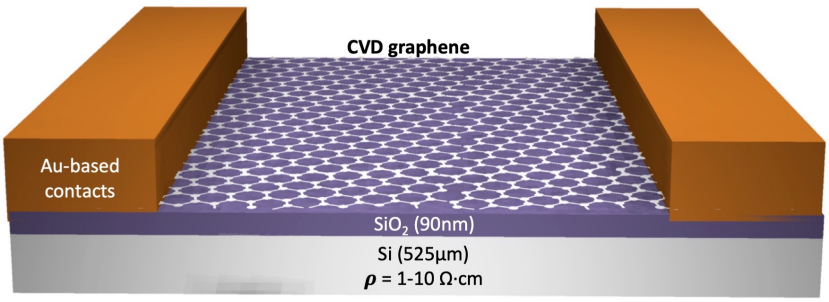
The layout can be prepared by the customer or by Graphenea under request (a design fee will be charged). Failure to adhere to the following design rules may result in unsuccessful GFET fabrication, a reduction in yield or in reduced device performance.

Alignment marks willl be added by Graphenea after the rest of the layout has been fixed. The customer can include their own alignment marks for further processing.

Designs must be approved by both the client and Graphenea before mask designs are submitted for manufacture (mask tapeout)

DR1	Minimum feature size – metal	5 µm	
DR2	Minimum feature size – graphene	10 µm	
DR3	Minimum feature separation – metal	10 µm	
DR4	Minimum feature separation - graphene	5 µm	

Device architecture



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Aspect ratio considerations

We strongly recommend you to adhere to the aspect ratio guidelines to enhance or worsen the mobility of your device. Deviations from these aspect ratios can result in anomalous mobilities.

Device width (μm)	L/W
<20 μm	>4
20-50	>2
>100	>1

Quality control

We carry out several quality checkpoints with different techniques, such as optical microscopy, Raman, AFM and electrical measurements (field-effect mobility, Dirac point and hysteresis).
We set the following thresholds to define a successful run.

AFM roughness

- RMS roughness < 1.5 nm
- Ra roughness < 1.0 nm

Raman

- I(G/2D) < 0.5
- Pos(G) < 1600 cm^{-1}
- FWHM(2D) < 45 cm^{-1}

Carrier transport

- Mobility within aspect ratio specifications.
- Dirac point < 50 V in 90 nm SiO_2 backgate
- Hysteresis < 20 V @10 mV/s

We set the following thresholds to define a successful die

Optical microscopy

- Channel integrity/coverage > 95%
- Device yield within die > 75%

We provide the QC summary of your run with the most relevant information.