Graphenea

Technical Datasheet

Graphene Field-Effect Transistor Chip: mGFET 4x4

General Description

The mGFET 4x4 chip from Graphenea is designed for sensing applications, and it is compatible with measurements in a liquid medium. The metal pads are passivated to avoid degradation and reduce leakage currents. It also includes a non-encapsulated electrode at the center of the chip, which allows for liquid gating without the need of an external gate electrode (such as Ag/AgCl probes). This device architecture enhances signal-to-noise ratio and reduces parasitics.

This version provides 14 graphene devices: 7 of them are one-channel devices and 7 of them are three-channel devices (a total of 28 graphene channels). These two geometries add flexibility to the measurement scheme (ΔV_D or ΔI_{sd}). The die is packaged and wirebonded to a leadless chip carrier (LCC) and it is fully compatible with the Graphenea Card.

Features

- State-of-the-art GFETs utilizing Graphenea's established consistently high-quality graphene
- Semiencapsulated geometry + central gate electrode for measurements in liquid environments.
- Packaged die for easy integration into readout schemes.
- 7x one-channel + 7x three-channel devices per chip.

Applications

- Graphene device research
- Chemical/gas sensing
- Biosensors
- Chemical sensors
- Bioelectronics
- Healthcare
- Industrial safety

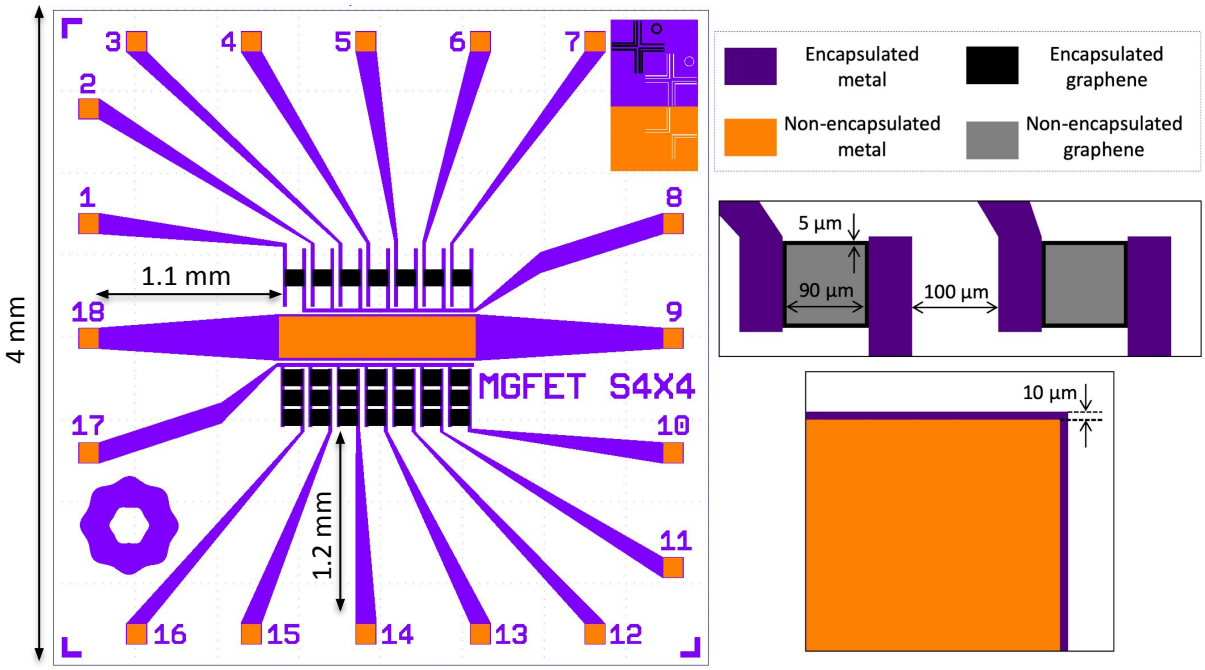
Typical Specifications

Die dimensions	4 mm x 4 mm
Chip thickness	525 µm
Number of channels per chip	28
Gate Oxide thickness	90 nm
Gate Oxide material	SiO_2
Resistivity of substrate	1-10 Ω·cm
Metallization	Au contacts
Encapsulation	50 nm Al_2O_3
Dirac point (liquid gating in PBS)	<1.5 V
Yield	>75 %

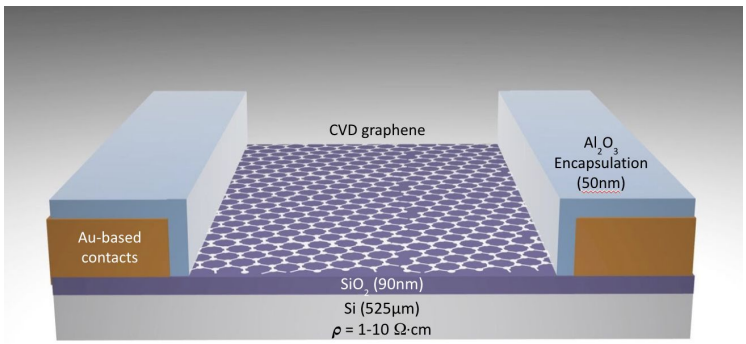
Absolute Maximum Ratings

Maximum gate-source voltage (liquid gating in PBS)	± 2V
Maximum temperature rating	150 °C
Maximum drain-source current density	10^7 A·cm^{-2}

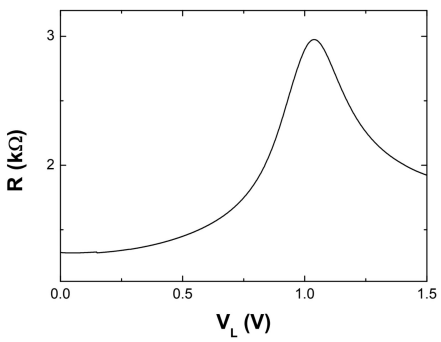
miniGFET 4x4 Layout



Device cross-section

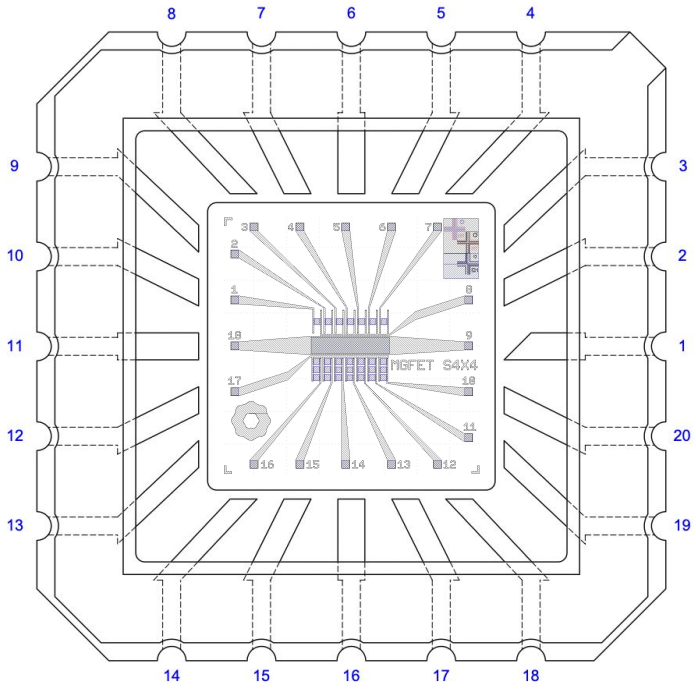


Typical characteristics



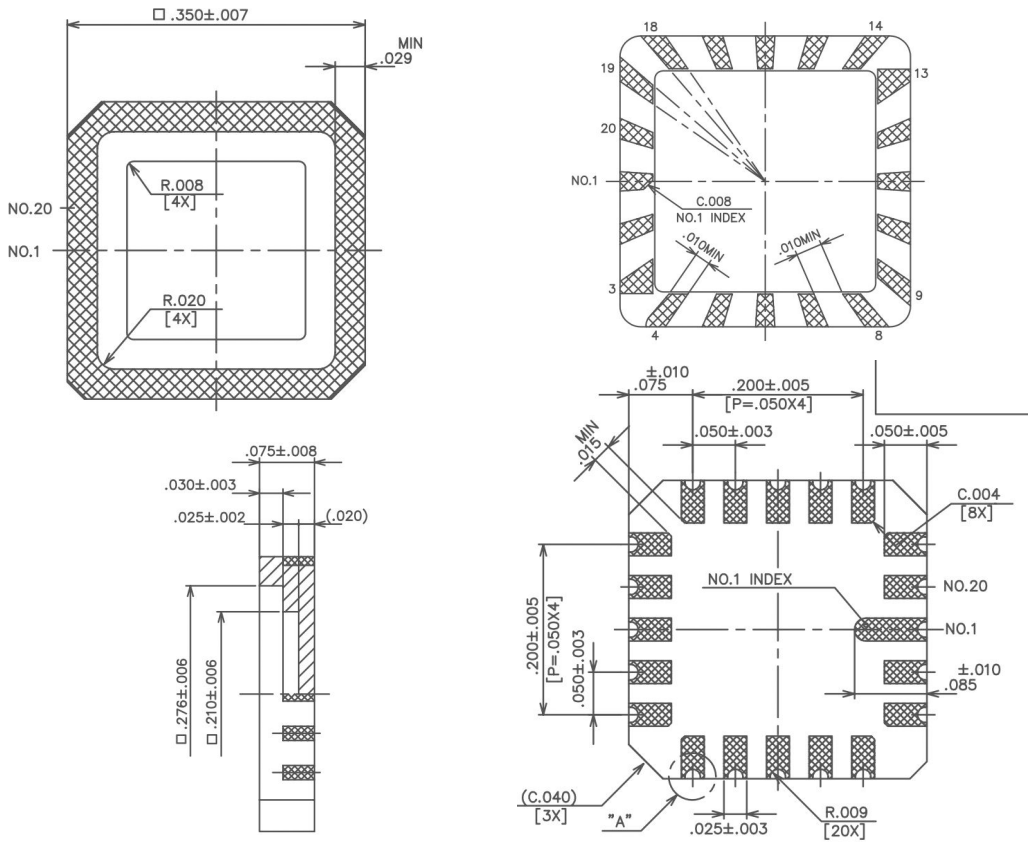
Transfer curve measured at source-drain voltage of 200mV under liquid gating through Phosphate Buffered Saline (PBS, 0.001X), using the on-chip electrode as gate electrode.

Die to carrier Layout



Label	Die pad	LCC pad
Source 1	1	10
Source 2	2	9
Source 3	3	8
Source 4	4	7
Source 5	5	6
Source 6	6	5
Source 7	7	4
Drain 1-7	8	2
On-chip gate	9	1
Source 8	10	20
Source 9	11	19
Source 10	12	18
Source 11	13	17
Source 12	14	16
Source 13	15	15
Source 14	16	14
Drain 8-14	17	12
On-chip gate	18	11

LCC dimensions (inches)



LCC specifications

LCC Model	SSM P/N LCC02034
Standard	JEDEC Type C
Number of pads	20
Body material	Ceramic and black alumina
Contact material	Ni + Au plated