Graphenea

Technical Datasheet

Graphene Field-Effect Transistor Chip: S-21

General Description

The GFET S-21 chip from Graphenea is designed for measurements in liquid medium. The new version provides 12 graphene devices connected in parallel, with encapsulation on the metal pads to avoid degradation and reduce leakage currents; the probe pads are located near the periphery of the chip. It also includes a non-encapsulated electrode at the center of the chip, which allows liquid gating without the need of an external gate electrode (such as Ag/AgCl probes). This device architecture enhances signal-to-noise ratio and reduces parasitics. It also removes device-to-device variation, smoothing device response and improving reliability.

Features

- State-of-the-art GFETs utilizing Graphenea's established consistently high-quality graphene
- Semiencapsulated geometry + central gate electrode for measurements in liquid environments.
- Perfect platform device for new sensor research and development
- 1 GFET (12 in parallel) per chip. Reliability.
- Mobilities typically in excess of 1000 $cm^2/V{\cdot}s$

Applications

- Graphene device research
- Biosensors
- Chemical sensors
- Bioelectronics

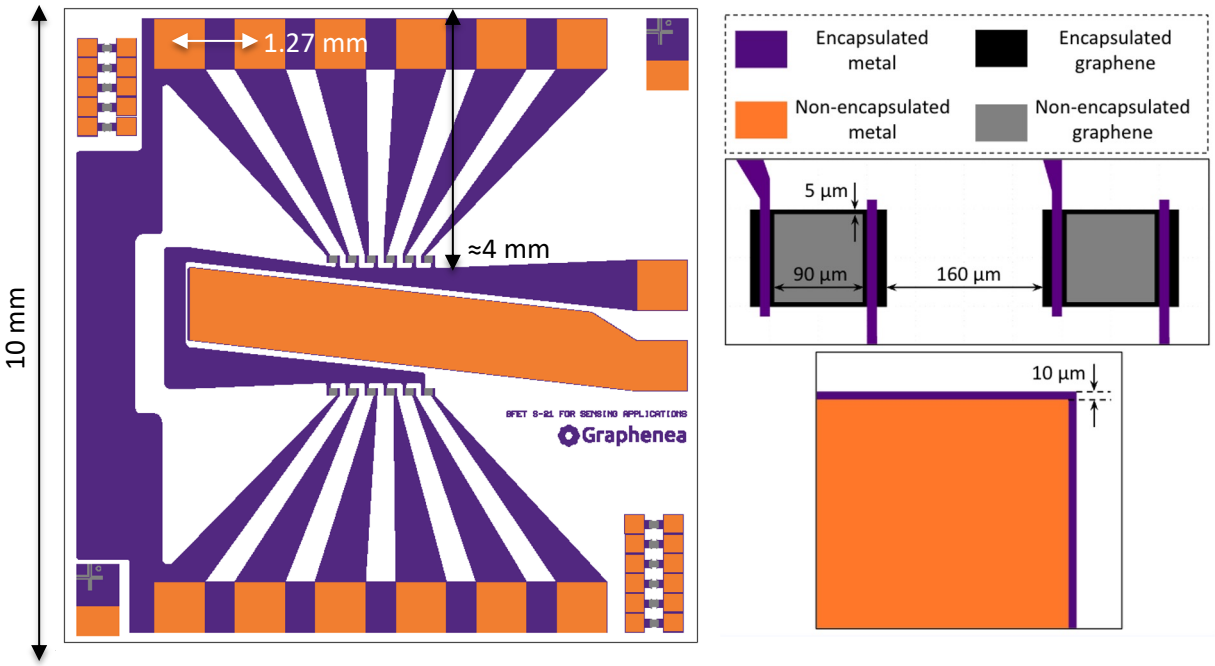
Typical Specifications

Chip dimensions	10 mm x 10 mm
Chip thickness	675 µm
Number of GFETs per chip	12
Gate Oxide thickness	90 nm
Gate Oxide material	SiO_2
Resistivity of substrate	1-10 Ω·cm
Metallization	Au contacts
Encapsulation	50 nm Al_2O_3
Graphene field-effect mobility (back gating)	>1000 $cm^2/V{\cdot}s$
Dirac point (liquid gating in PBS)	<1 V
Number of graphene channels with integrity	>75 %

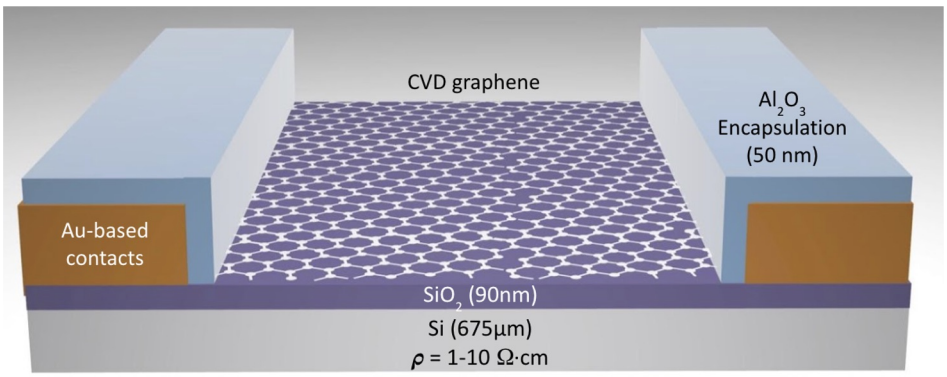
Absolute Maximum Ratings

Maximum gate-source voltage (back gating)	± 50V
Maximum gate-source voltage (liquid gating in PBS)	± 2V
Maximum temperature rating	150 °C
Maximum drain-source current density	10^7 $A{\cdot}cm^{-2}$

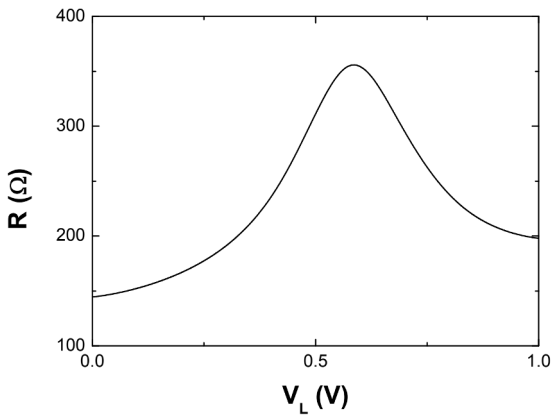
GFET-S21 Layout



Device cross-section



Typical characteristics



Transfer curve under liquid gating through Phosphate Buffered Saline (PBS, pH=7.3), using the on-chip electrode as gate electrode.