Measurement Protocols and Handling Instructions

Graphene Field-Effect Transistor Chip: GFET-S31/EOT20nm

Typical Measurement Configurations

The following explains the electrical measurements that can be performed on the different devices in GFET-S31.

Measurement type

These devices allow field-effect measurements by simultaneously applying two voltages:

- Source-drain voltage (V_{SD}): applied between the two probes (source and drain), while one of them is grounded (see Figure 1a). V_{SD} enables the transport of charge carriers through the graphene channel, with an associated source-drain current (I_{SD}). V_{SD} can be varied in order to get the desired I_{SD} outcome (see Figure 1b).
- Gate voltage (V_G): applied to the backgate contact (doped Si substrate). V_G creates an electric field on the graphene channel, modulating the conductivity of graphene (see Figure 1c).

Alternatively, the Si substrate can be contacted either from the top surface by scratching the 90 nm-thick SiO_2 with a diamond pen in one of the chip corners; or alternatively from the underside of the chip, for instance using a probe station chuck.

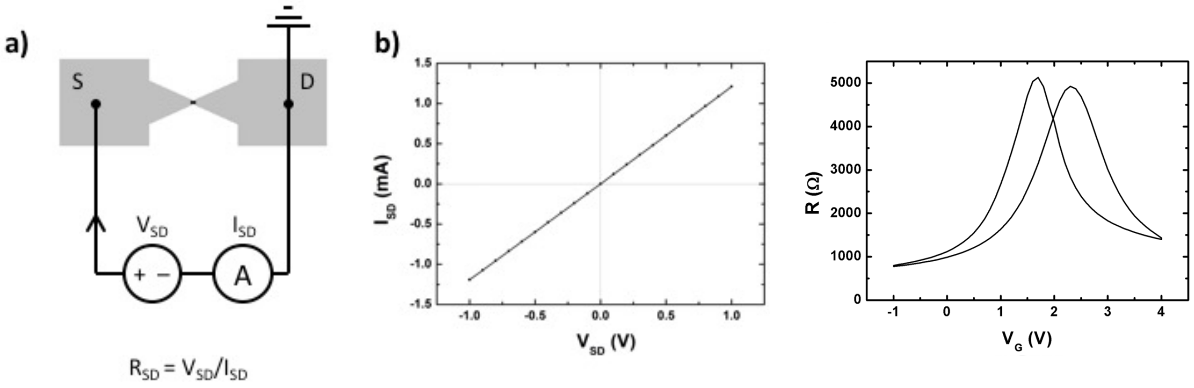


Figure 1. a) Scheme of the 2-probe device, with the corresponding electrical measurement configuration. b) Typical output curve measured at room temperature and vacuum conditions. c) Typical transfer curve measured at V_{SD}= 20mV (right), measured at the same conditions as in b).

3-probe measurements

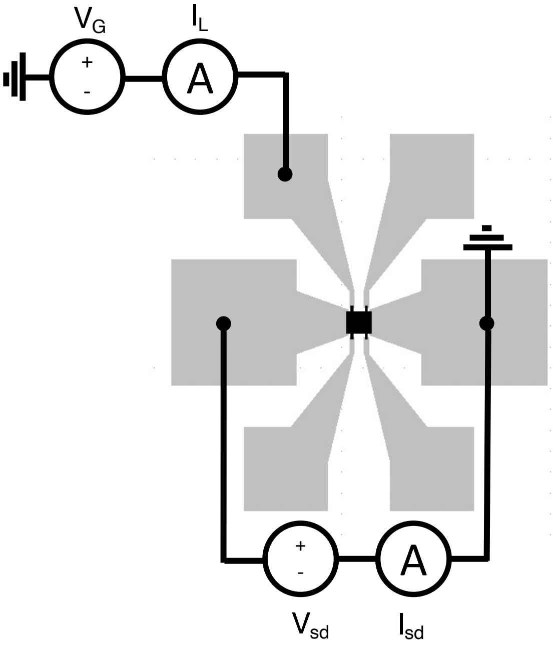


Figure 2. Scheme of the 3-probe measurement in a device, with the corresponding electrical measurement configuration.

Field-effect measurement through top-gate

With the S31 die, local gating can be achieved through the 3-probe measurement scheme (see Figure 2). The method is to apply a source-drain voltage (V_{sd}) between two outer contacts, measure the current between those two contacts (I_{sd}) and additionally apply a gate voltage (V_G) through the backgate electrode while monitoring the leakage current (I_L). The benefit of this is that the resistance of the graphene channel alone can be tuned with a voltage, and this can be done contacting a pad and not the substrate itself which eases integration.

Due to the aggressive scaling of the gate dielectric and the channel passivation, the device can be operated within a 5V window which is ≈10 times less operation voltage than using the substrate as a backgate.

The resistivity of graphene is usually expressed per thickness unit, i.e. the so-called sheet resistance:

$$R_S = R_{CH}\frac{W}{L},$$

being R_{CH} the resistance of the graphene channel, and W and L the width and inner length of the graphene channel, respectively. The field-effect mobility (μ_{FE}) can be calculated by using the following equation:

$$\mu_{FE} = g \cdot \frac{1}{C_{gate}},$$

where:

- $g = d\sigma/dV_G$ is the transconductance, being $\sigma = 1/R_S$,
- C_{gate} is the capacitance per unit area of the gate dielectric.

μ_{FE} is usually calculated using the maximum transconductance.

4-probe measurements

An alternative measurement scheme (see Figure 3) is to apply a source-drain voltage (V_{sd}) between two outer contacts, measure the current between those two contacts (I_{sd}) and additionally apply a voltage (V_J) through the backgate electrodes while monitoring the heating current (I_J).
This current I_J will generate heat by Joule effect, effectively heating the graphene channels which sits on top. This can be used to carry out temperature dependent measurements.

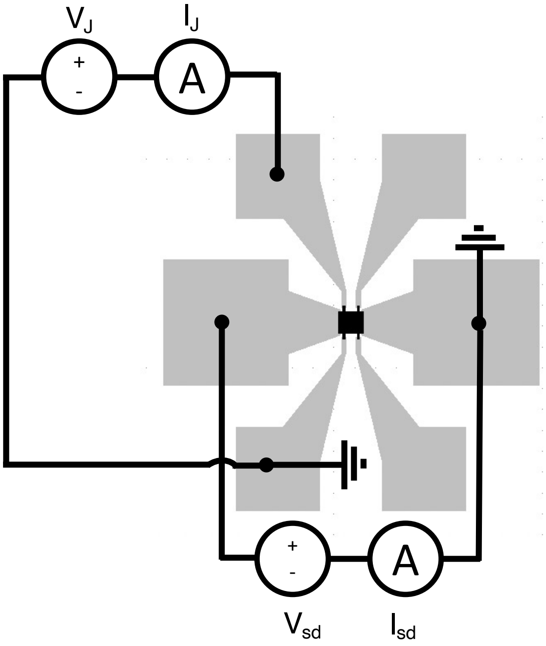
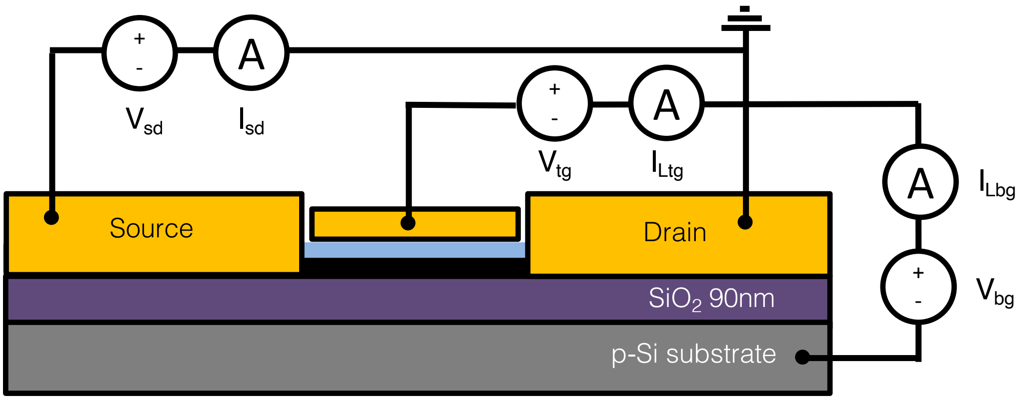


Figure 3. Scheme of the 4-probe measurement in a device, with the corresponding electrical measurement configuration.

Double-gated measurements

In analogy to Silicon On Insulator (SOI) devices, a double-gated scheme can be also easily implemented in the S31: biasing both the substrate (V_{bg}) and the top gate (V_{tg}) with two different voltages; these voltajes will have associated two different leakage currents, I_{Lbg} and I_{Ltg} and respectively. In this way, one can modulate globally the Fermi level, accesing either the Dirac point, p-type or n-type branch of the ambipolar transistor, and individually modulate the conductance of each transistor around those points; this will be reflected in the current I_{sd} that flows due to the V_{sd} bias.



Storage recommendations

In addition, storage of the chips in a low humidity environment (N_2 cabinet, desiccator, or vacuum) is highly recommended.

Basic handling instructions

The graphene used in our GFETs is high-quality monolayer CVD graphene and highly prone to damage by external factors. To maintain the quality of your devices, we recommend taking the following precautions:

- Be careful when handling the GFET chip that tweezers do not make contact with the device area. Metallic tweezers should be avoided, as they can damage/scratch the chip edges/surface
- Treat the devices as sensitive electronic devices and take precautions against electrostatic discharge
- Ideally store in inert atmosphere or under vacuum in order to minimize adsorption of unknown species from the ambient air
- Do not ultrasonicate the GFET dies
- Do not apply any plasma treatment to the GFET dies
- Do not subject the GFET dies to strongly oxidizing reagents