1 GENERAL DESCRIPTION

The CLC2622 is a LCD Driver with either static mode driving up to 40 segments or multiplexing mode driving up to 8 rows and 32 columns. A display storage is available via a dual RAM to be addressed by 8x40 words.

The large voltage range and a low current consumption makes the driver suitable for a variety of different LCD display. Also large pixel size applications are supported due to the low driver impedance. Several CLC2622 can be easily cascaded, no external resistor bias chain and no external clock is necessary.

1.1 FEATURES

- Static- or multiplexing LCD driver
- Programmable mux mode
- Mux2: 2 rows and 38 columns
- Mux4: 4 rows and 36 columns
- Mux8: 8 rows and 32 columns
- Drives up to 40 segments in static mode
- Dual RAM for display storage addressable as 8 x 40 words
- LCD blanking by BLANK bit and STR signal
- All segments on by SET bit
- On chip LCD bias voltage generation
- On chip display refresh
- Synchronize feature for large LCD applications
- On chip FR clock generation
- Serial data input/output
- Schmitt trigger inputs
- 0.8µm HV-CMOS process

1.2 SCHEMATIC

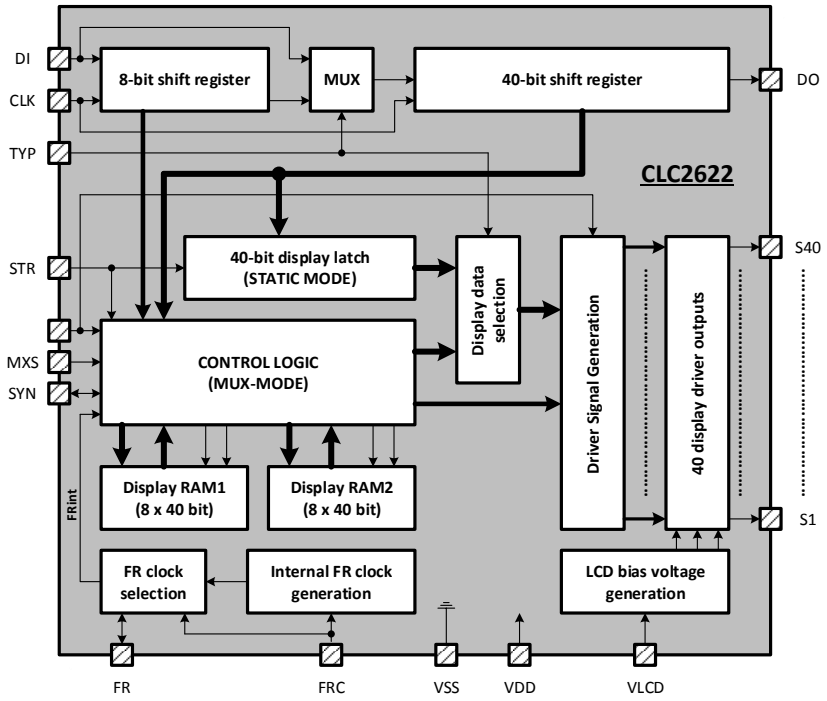


Figure 1 – CLC2622 Block Diagram

2 PINOUT

2.1 PACKAGE BUMPED DIE

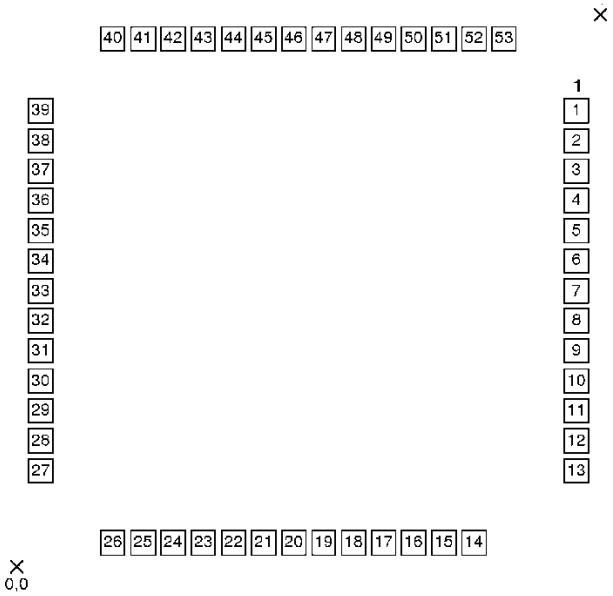


Figure 2 - CLC2622 – CSP Chip Scale Package

2.2 PACKAGE QFN56

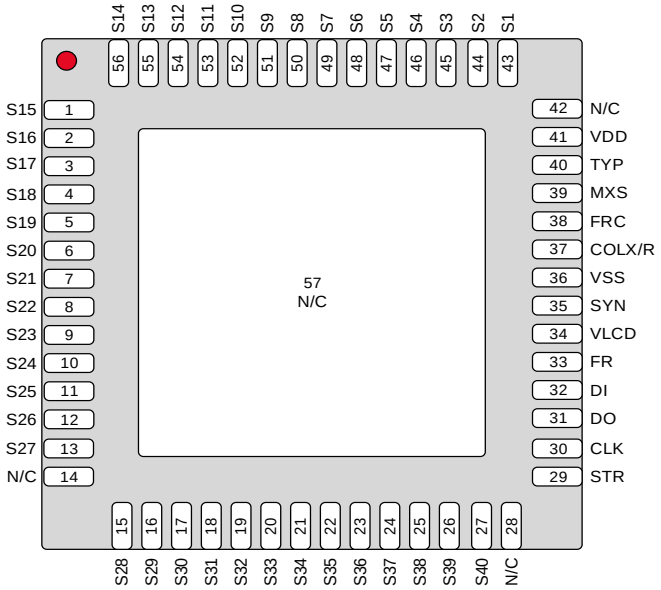


Figure 3 – CLC2622 - Package QFN56

2.3 PIN DESCRIPTIONS

Table 1 - PIN Description

		Bumped Die Coordinates				
Signal Name	**QFN56 Pin No.**	**Pad. No**	**X/µm**	**Y/µm**	**Type**	**Function**
-	42	-	-	-	-	n/c
VDD	41	1	2906	2340	PWR	Digital supply voltage
TYP	40	2	2906	2190	IN	Version selection (static or mux mode)
MXS	39	3	2906	2040	IN	Master/Slave selection input
FRC	38	4	2906	1890	IN	FR clock selection input
COLX/R	37	5	2906	1740.5	IN	Column mode selection (mux mode)
VSS	36	6	2906	1590	PWR	Ground
SYN	35	7	2906	1440	IN/OUT	Synchronize signal input/output
VLCD	34	8	2906	1290	PWR	LCD supply voltage input
FR	33	9	2906	1140	IN/OUT	FR clock input/output
DI	32	10	2906	990.5	IN	Serial data input
DO	31	11	2906	840	OUT	Serial data output
CLK	30	12	2906	690.5	IN	Shift clock for serial interface
STR	29	13	2906	540.5	IN	Strobe input pin
-	28	-	-	-	-	n/c
S40	27	14	2341	125	OUT	Row/column driver outputs
S39	26	15	2191	125	OUT	Row/column driver outputs
S38	25	16	2041	125	OUT	Row/column driver outputs
S37	24	17	1891	125	OUT	Row/column driver outputs
S36	23	18	1741	125	OUT	Row/column driver outputs
S35	22	19	1591	125	OUT	Row/column driver outputs
S34	21	20	1441	125	OUT	Row/column driver outputs
S33	20	21	1291	125	OUT	Row/column driver outputs
S32	19	22	1141	125	OUT	Row/column driver outputs
S31	18	23	991	125	OUT	Row/column driver outputs
S30	17	24	841	125	OUT	Row/column driver outputs
S29	16	25	691	125	OUT	Row/column driver outputs
S28	15	26	541	125	OUT	Row/column driver outputs
-	14	-	-	-	-	n/c
S27	13	27	126	540	OUT	Row/column driver outputs
S26	12	28	126	690	OUT	Row/column driver outputs
S25	11	29	126	840	OUT	Row/column driver outputs
S24	10	30	126	990	OUT	Row/column driver outputs
S23	9	31	126	1140	OUT	Row/column driver outputs
S22	8	32	126	1290	OUT	Row/column driver outputs
S21	7	33	126	1440	OUT	Row/column driver outputs
S20	6	34	126	1590	OUT	Row/column driver outputs
S19	5	35	126	1740	OUT	Row/column driver outputs
S18	4	36	126	1890	OUT	Row/column driver outputs
S17	3	37	126	2040	OUT	Row/column driver outputs
S16	2	38	126	2190	OUT	Row/column driver outputs
S15	1	39	126	2340	OUT	Row/column driver outputs
S14	56	40	541	2755	OUT	Row/column driver outputs
S13	55	41	692	2755	OUT	Row/column driver outputs
S12	54	42	841	2755	OUT	Row/column driver outputs
S11	53	43	991	2755	OUT	Row/column driver outputs
S10	52	44	1141	2755	OUT	Row/column driver outputs

Bumped Die Coordinates						
Signal Name	**QFN56 Pin No.**	**Pad. No**	**X/µm**	**Y/µm**	**Type**	**Function**
S9	51	45	1291	2755	OUT	Row/column driver outputs
S8	50	46	1441	2755	OUT	Row/column driver outputs
S7	49	47	1591	2755	OUT	Row/column driver outputs
S6	48	48	1741	2755	OUT	Row/column driver outputs
S5	47	49	1891	2755	OUT	Row/column driver outputs
S4	46	50	2041	2755	OUT	Row/column driver outputs
S3	45	51	2191	2755	OUT	Row/column driver outputs
S2	44	52	2341	2755	OUT	Row/column driver outputs
S1	43	53	2491	2755	OUT	Row/column driver outputs

3 ABSOLUTE MAXIMUM RATINGS

Table 2 - Absolut Maximum Rating

Parameter	Symbol	Conditions	Min.	Max.	Unit
Logic supply voltage range	V_{DD}		-0.3	6	V
LCD supply voltage range	V_{LCD}		-0.3	9	V
Voltage at DI, DO, CLK, STR, FR, COLX, MXS, SYN, FRC	V_{LOGIC}		-0.3	V_{DD}+0.3	V
Voltage at S1 to S40	V_S		-0.3	V_{LCD}+0.3	V
Storage temperature range	$\vartheta_{storage}$		-65	150	°C
Soldering Profile	$t_{soldering}$	ϑ_{sol_max} = 260 °C		12	s
ESD Protection	V_{ESD}	According to MIL-STD-883C method 3015	1		kV
Permanent current into ESD protection diodes	I_{DC_ESD}	For forward biased ESD diodes only!		1	mA

4 ELECTRICAL CHARACTERISTICS

4.1 OPERATING CONDITIONS

Table 3 - Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operation temperature range	ϑ_{op}		-40		85	°C
Logic supply voltage	V_{DD}		3		6	V
LCD supply voltage	V_{LCD}		3		9	V

4.2 DC CHARACTERISTICS

Test conditions unless otherwise specified: 25 °C, VDD = 5V, VLCD = 7V
Electrical characteristics are valid for the whole specified temperature and supply voltage range.

Table 4 - DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
1. Power supply						
LCD supply input current	I_{LCD}	note 1)			250	uA
Supply current / external FR	I_{DD}	note 1)		50		uA
Supply current	I_{DD}	note 2)			250	uA
Supply current / internal FR	I_{DD}	note 3)			1	mA
2. Digital inputs DI, CLK, STR, FR, COLX, MXS, SYN, FRC, TYP						
Input leakage	I_{IN}	$0 < V_{IN} < V_{DD}$	-5		5	uA
Input capacitance	C_{IN}				10	pF
Low level input voltage	V_{IL}		V_{SS}		$0.3 \cdot V_{DD}$	V
Low level input voltage	V_{IH}		$0.7 \cdot V_{DD}$		V_{DD}	V
3. Digital outputs DO, SYN, FR						
High level output voltage	V_{OH}	I_{OUTH} = 4 mA	V_{DD} - 0.5			V
Low level output voltage	V_{OL}	I_{OUTL} = 4 mA			V_{SS} + 0.5	V
4. Driver outputs S1 – S40						
DC output voltage	V_{DC}	V_{LCD} = 5V	-50		50	mV
Driver impedance	R_{OUT}	I_L = 20uA, note 4)		10		kΩ

1) All outputs open, FR = 0 - 400 Hz external, all other inputs at VDD
2) All outputs open, FR = 0 - 400 Hz external, f_{CLK} = 1MHz, all other inputs at VDD
3) All outputs open, FR clock generation internal, f_{CLK} = 1MHz, all other inputs at VDD
4) Resistance of output drivers with I_L=20uA. Outputs measured one at a time.

4.3 AC CHARACTERISTICS

4.3.1 AC Characteristics for V_{DD} = 4.5 to 5.5V

Conditions: V_{DD} = 4.5 to 5.5V, V_{LCD} = 3 to 7V, T_A = -40 °C to 85 °C

Table 5 – Conditions 4.5 to 5.5V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
1. Timing						
Clock high pulse width	t_{CH}		120			ns
Clock low pulse width	t_{CL}		120			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}	note 1)	20			ns
Data input hold time	t_{DH}	note 1)	30			ns
Data output propagation	t_{PD}	C_{LOAD} = 50pF			100	ns
STR pulse width	t_{STR}		100			ns
Clock falling to STR rising	t_P		10			ns
STR falling to Clock falling	t_D		200			ns
FR frequency (2/4/8)	f_{FR}	FR clock external		128/256/512		Hz
2. On chip FR clock generation						
FR frequency in static mode	$f_{FR-STAT}$		50	100	150	Hz
FR frequency in mux mode 2	$f_{FR-MUX2}$		100	200	300	Hz
FR frequency in mux mode 4	$f_{FR-MUX4}$		200	400	600	Hz
FR frequency in mux mode 8	$f_{FR-MUX8}$		400	800	1200	Hz

1) t_{DS} + t_{DH} must be >= 100ns.
2) The FR frequency must be n times the desired LCD refresh rate where n is the mux mode number.

4.3.2 AC Characteristics for V_{DD} = 3 to 6V

Conditions: V_{DD} = 3 to 6V, V_{LCD} = 3 to 9V, T_A = -40 °C to 85 °C

Table 6 – Conditions 3 to 6V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
1. Timing						
Clock high pulse width	t_{CH}		120			ns
Clock low pulse width	t_{CL}		120			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}	note 1)	20			ns
Data input hold time	t_{DH}	note 1)	30			ns
Data output propagation	t_{PD}	C_{LOAD} = 50pF			100	ns
STR pulse width	t_{STR}		100			ns
Clock falling to STR rising	t_P		10			ns
STR falling to Clock falling	t_D		200			ns
FR frequency (2/4/8)	f_{FR}	FR clock external		128/256/512		Hz
2. On chip FR clock generation						
FR frequency in static mode	$f_{FR-STAT}$		50	100	150	Hz
FR frequency in mux mode 2	$f_{FR-MUX2}$		100	200	300	Hz
FR frequency in mux mode 4	$f_{FR-MUX4}$		200	400	600	Hz
FR frequency in mux mode 8	$f_{FR-MUX8}$		400	800	1200	Hz

1) t_{DS} + t_{DH} must be >= 500ns.
2) The FR frequency must be n times the desired LCD refresh rate where n is the mux mode number.

4.3.3 Timing Waveforms

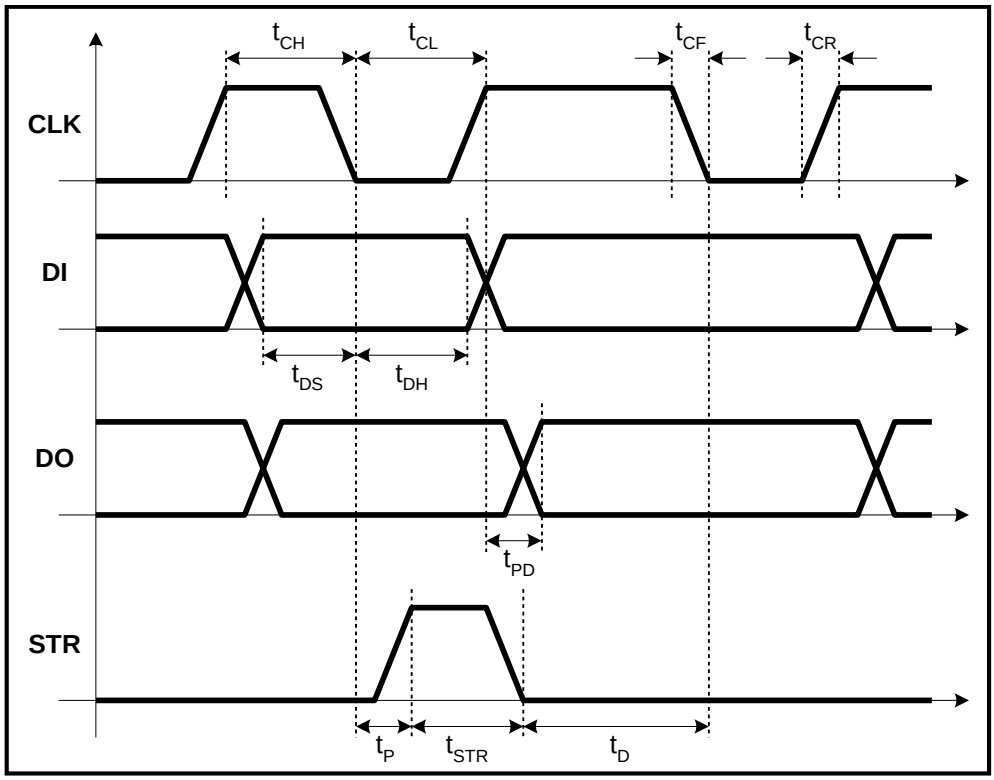


Figure 4 - CLC2622 - Timing Waveforms

5 FUNCTIONAL DESCRIPTION

5.1 OVERALL FUNCTIONAL DESCRIPTION

The CLC2622 is a low power CMOS LCD controller driver, designed to drive a graphic display with 2, 4 or 8 rows and 38, 36 or 32 columns in muxed mode or up to 40 segments in static mode. All necessary functions for the display are provided in a single chip, including on-chip generation of the LCD bias voltages, display refresh and FR clock generation, resulting in a minimum of external components.

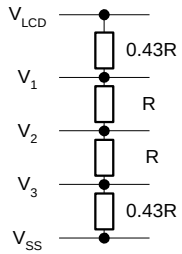
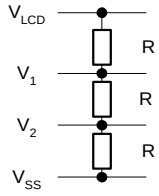
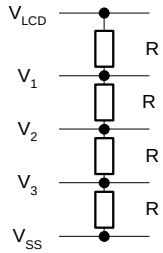
In mux mode the 2, 4 or 8 way multiplex is digitally programmable by the control byte. The display refresh is handled via 2 selectable 8 x 40 bit RAMs. The LCD pixels (segments) are addressed on a one to one basis with the 8 x 40 bit display RAMs (a set bit corresponds to an activated pixel).

In static mode the circuit drives up to 40 LCD segments from a serial clocked input. The serial data is parallel loaded into 40 latches under control of the strobe pin. The latched data determines which segments are ON or OFF. A blank function is provided to clear the display.

5.2 LCD BIAS VOLTAGE GENERATOR (MUX MODE ONLY)

The intermediate bias voltages for the LCD display are generated and buffered on-chip. This removes the need for an external resistor bias chain.

Table 7 - LCD Voltage Bias Levels

*) $V_{OP} = V_{LCD} - V_{SS}$	LCD drive type	Bias configuration	V_{OP}/V_{OFF}(rms) *)	V_{ON}(rms)/V_{OFF}(rms)
	n = 2 1 : 2 MUX	5 levels	$\sqrt{\frac{2n}{1-\sqrt{\frac{1}{n}}}} = 3.69$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 2.41$
	n = 4 1 : 4 MUX	4 levels	3	$\sqrt{1+\frac{8}{n}} = 1.73$
	n = 8 1 : 8 MUX	5 levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n+15}{n+3}} = 1.446$

5.3 TYP INPUT

The TYP input is used to select if the device is in static or mux mode. When TYP = logic 0 the device is configured to function as a static driver. With TYP = logic 1 the mux mode functionality is selected.

Table 8 - Function mode selection

TYP	Function
0	Static driver
1	Mux mode driver

5.4 MXS INPUT (mux mode version only)

The MXS input is used to determine if the device is in slave or in master configuration. Difference between the master and the slave mode is the synchronization of the device (see SYN Input/Output).

Table 9 - Mux mode selection

MXS	Function
0	Master device
1	Slave device

5.5 SYN INPUT/OUTPUT (mux mode version only)

In master configuration (MXS = logic 0) this pin is configured to function as a output for the internally generated synchronize signal. A synchronize pulse is always generated at the beginning of a new time frame. In cascaded applications this signal should be used to synchronize the devices.
If the circuit is in slave configuration the SYN pin is an input. If the SYN input is high the slave device starts with row 1 of the selected RAM on the next falling edge of the FR signal.
When cascading devices, all SYN lines must be tied together. In static mode configuration this pin has no function.

5.6 FR INPUT/OUTPUT

The FR signal controls the segment output frequency generation. To avoid having DC on the display, the FR clock must have 50% duty cycle. The frequency of the FR signal must be n times the desired display refresh rate.

5.7 FRC INPUT / INTERNAL OSCILLATOR

The FRC input is used to select if the FR clock source is external or if an internal oscillator is used to generate the FR clock. If FRC = logic 1 the pin FR is an input for the external clock signal. With FRC = logic 0 the FR pin is the output for the internally generated frame clock.

Table 10 - FR control input

FRC	Pin type	Clock source
0	OUT	internal
1	IN	external

5.8 COLX/R INPUT

When COLX/R is logic 1 in static configuration, the display is blanked (all segment outputs are tied to V_{SS}). R does not clear the information in the output latches.
In mux mode configuration the device will function only as a column driver if the COLX/R signal is logic 0 (see Tab. 14). In cascaded application, one device should be used in row/column configuration (COLX/R = logic 1) and the rest as pure column drivers. Note when cascading devices never cascade one mux mode with another.

Table 11 - COLX/R INPUT Selection

COLX/R	Type	
1	STATIC	Display blanc
0	MUX MODE	COLUMN Driver
1	MUX MODE	COLUMN / ROW Driver

5.9 DATA INPUT/OUTPUT

The data input pin DI is used to load serial data into the shift register. The data is clocked in a rate determined by the clock input frequency at pin CLK. The serial data word length is 48 bit in mux mode and 40 bit in static mode (see Tab.13). Data are loaded in inverse numerical order, the data for bit 47 (39) is loaded first and bit 0 last.

The data output pin DO is equal to the data at DI delayed by 48 clock cycles in mux mode respectively 40 cycles in static mode.

The first 40 bits of the serial data are the display data. In static mode a logic 1 on the STR input transfers the data to the corresponding output latch. In mux mode the falling edge of STR is used to write the data to the selected RAM address.

In mux mode the last 8 bits of the serial data are the control word (see Tab. 15, 16 and 17). Bit 7 (BLANK) forces all column outputs to “0” (display OFF). Bit 6 (SET) forces all column output to “1” (display ON). If both bits are active the BLANK function has priority. The BLANK and the SET bit are activated when logic 1. The bits 5 to 3 represent the RAM address for the display data. Command bit 2 (W) is used for RAM selection. If bit 2 = logic 0, then RAM 1 can be written and RAM2 is read. If bit 2 = logic 1, then RAM2 can be written and RAM1 is read. If the device is in master mode switching between the RAMs occurs after RAM address 0 is written. If the device is in slave mode switching occurs if the synchronize input SYN = logic 1. The switching will set effective on the first falling edge of the FR signal from the next time frame. A time frame begins with row 1 and ends with row 2, 4 or 8 according to the mux ratio. The bits 1 and 0 of the control word are used to select the actual mux ratio.

5.10 MUX MODE WITH COLX = INACTIVE (LOGIC 1)

Table 12 - Data transfer cycle

	Bit 47 ... Bit 8	Bit 7 ... Bit 0
Mux 8 mode	COL32 to 1, ROW 8 to 1	COMMAND 7 to 0
Mux 4 mode	COL36 to 1, ROW 4 to 1	COMMAND 7 to 0
Mux 2 mode	COL38 to 1, ROW 2 to 1	COMMAND 7 to 0

5.11 MUX MODE WITH COLX = ACTIVE (LOGIC 0)

	Bit 47 ... Bit 8	Bit 7	Bit 0
All mux modes	COL40 to 1		COMMAND 7 to 0

5.12 STATIC MODE

Bit 39 ... Bit 0
SEG40 to 1

Table 13 - Data assignment

Driver name	COLX/R=1			COLX/R=0
	Mux 2	Mux4	Mux 8	
S1	Row1	Row1	Row1	Col1
S2	Row2	Row2	Row2	Col2
S3	Col1	Row3	Row3	Col3
S4	Col2	Row4	Row4	Col4
S5	Col3	Col1	Row5	Col5
S6	Col4	Col2	Row6	Col6
S7	Col5	Col3	Row7	Col7
S8	Col6	Col4	Row8	Col8
S9…S40	Col7…38	Col5…36	Col1…32	Col9…40

Table 14 - Command byte

Command bits 7 to 0

7	6	5	4	3	2	1	0
BLANK	SET	RAM address			W	Mux ratio	

BIT7: The BLANK bit forces all column outputs OFF.
BIT6: The SET bit forces all column outputs ON.
BIT2: If W = 0, RAM1 can be written and RAM2 is read, if W = 1, RAM2 can be written and RAM1 is read.

Table 15 - Mux mode selection

Mux ratio (bit1, bit0)

BIT 1	BIT 0	Mux ratio
0	0	2
0	1	---
1	0	4
1	1	8

Table 16 - RAM addressing

RAM address selection

Command bit 5 to 3			RAM address	LCD row
Mux mode				
Mux 2	Mux4	Mux 8		
000	000	000	00000001	1
100	100	100	00000010	2
---	010	010	00000100	3
---	110	110	00001000	4
---	---	001	00010000	5
---	---	101	00100000	6
---	---	011	01000000	7
---	---	111	10000000	8

5.13 CLK INPUT

The CLK input is used to clock the serial data into the shift register and to clock the serial data out. Loading and shifting of the data occurs at the falling edge of the clock, outputting of the data at the rising edge. When cascading devices, all clock lines should be tied together.

5.14 STR INPUT

In static mode configuration the STR input is used to latch the input data shifted into the 40-bit shift register. The latched data is held for display. A logic 1 on the STR input transfers the data from the shift register to the corresponding latches. The latches are transparent during the whole time STR remains at logic 1.

In mux mode configuration the STR input is used to write to the display RAM, to blank the LCD and to synchronize the master device (writing address 0 of RAM1 or RAM2). The STR input when logic 1 blanks the LCD display by pulling the segment outputs S1 to S40 up to V_{LCD}.

On the falling edge of the STR signal the data loaded to shift register is written to the selected display RAM address. If the display address is 0 and the device is in master mode a synchronization flag is set. If it is necessary this flag will cause a change of the selected display ram at the beginning of the next time frame. Also a synchronization pulse is generated and at the SYN pin. This pulse will synchronize the slave devices in cascaded applications.

5.15 DRIVER OUTPUTS S1 TO S40

There are 40 LCD driver outputs available on the device. In static mode or in mux mode with COLX/R active (logic 0) the outputs S1 to S40 function as column (segment) drivers. If the device is in mux mode configuration with COLX/R inactive (logic 1) the outputs S1 to Sn function as row drivers and the remaining outputs as column drivers, where n is the mux mode number (2, 4 or 8). There is a one to one relationship between the selected RAM (output latch) and the LCD driver outputs. Setting the bit turns the segment “ON” and clearing it turns it “OFF”.

6 ROW AND COLUMN MULTIPLEXING WAVEFORMS

6.1 MUX 2 MODE CONFIGURATION

$V_{OP} = V_{LCD} – V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

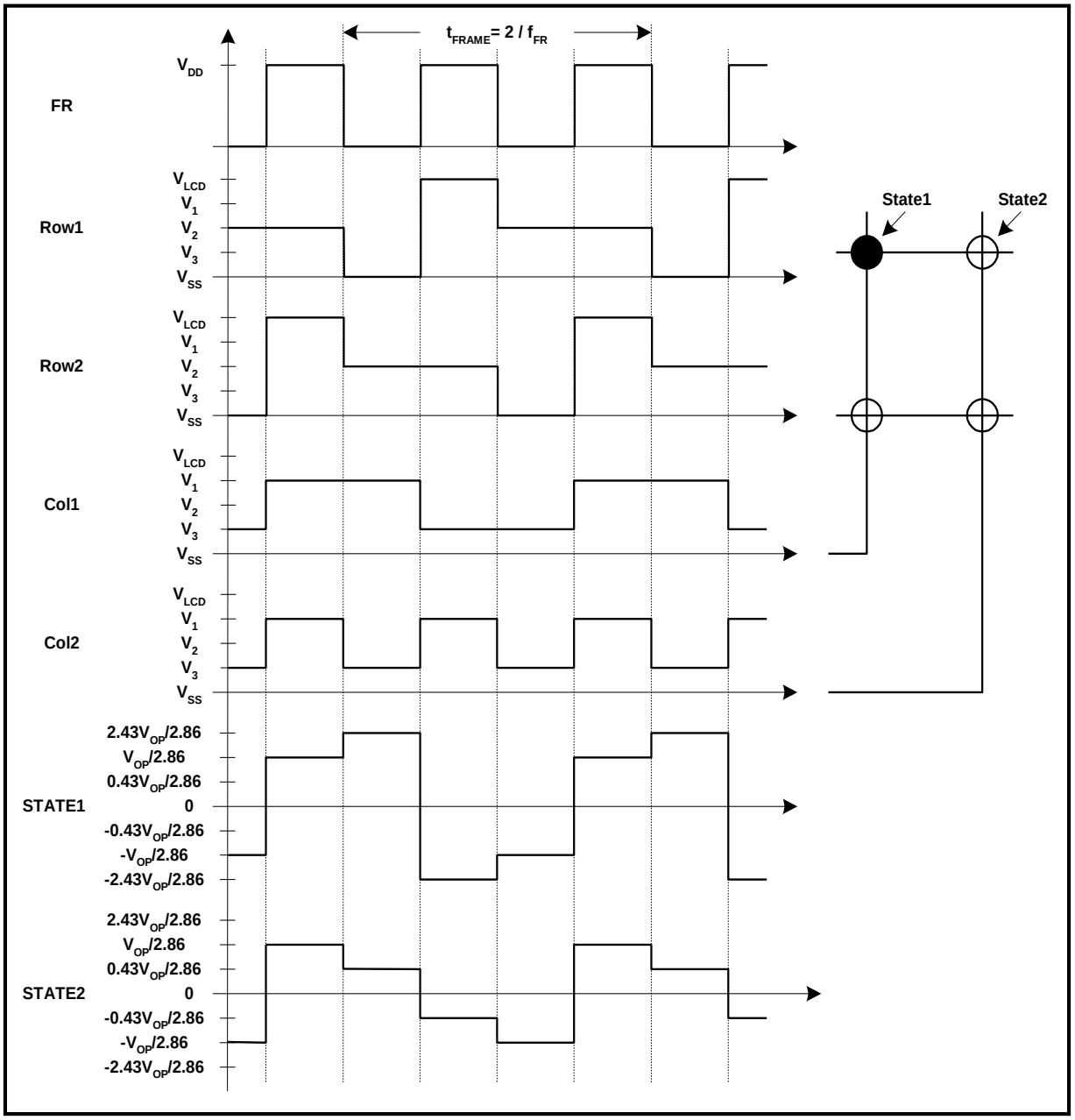


Figure 5

6.2 MUX 4 MODE CONFIGURATION

$V_{OP} = V_{LCD} – V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

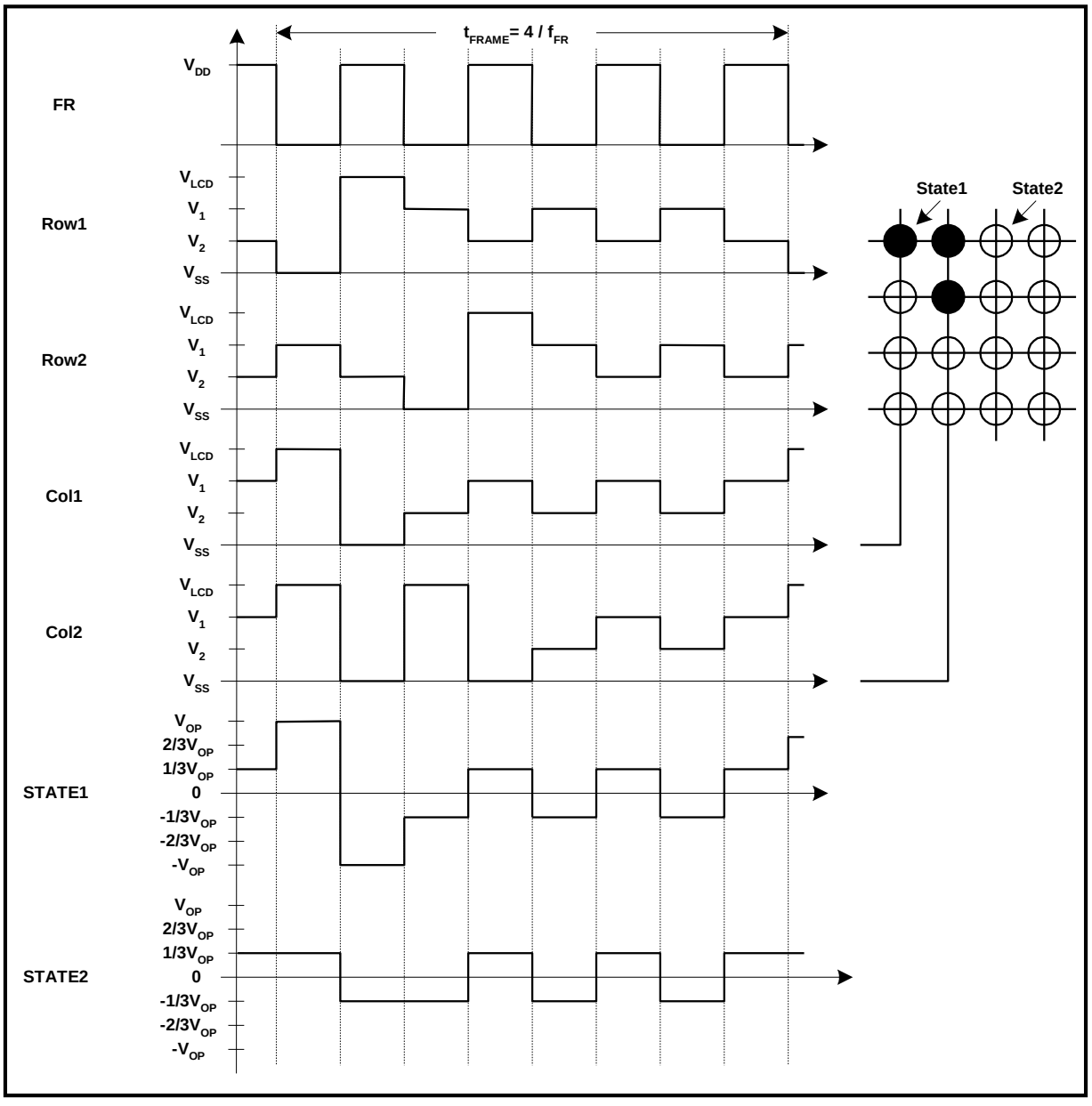


Figure 6

6.3 MUX 8 MODE CONFIGURATION

$V_{OP} = V_{LCD} – V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

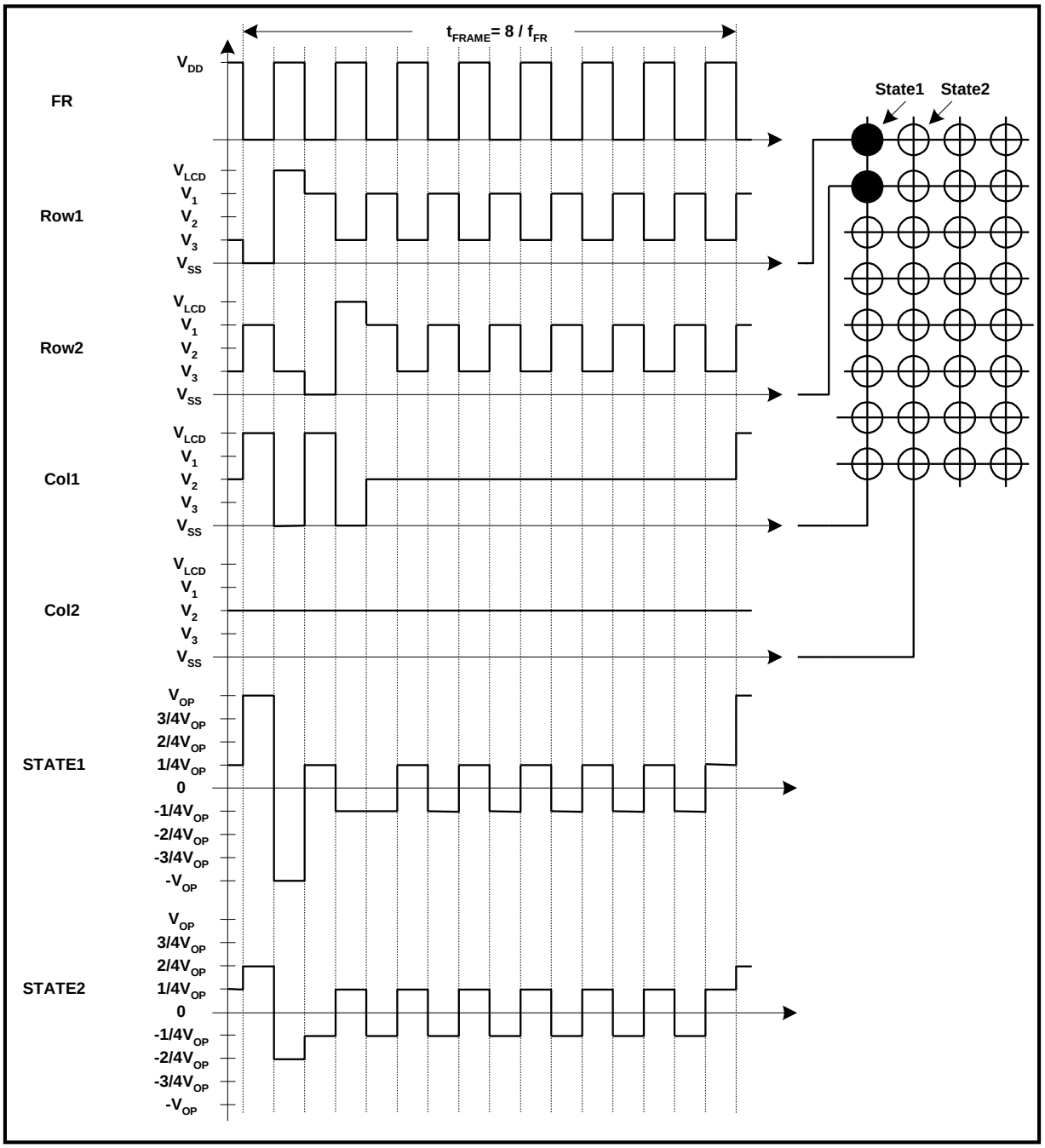


Figure 7

6.4 MUX 8 MODE CONFIGUTATION

Table 17 - Segment switching table

Latched data (DI) 0 = VIL, 1 = VIH	FR	Segment voltage 0 = VSS, 1 = VLCD
0	0	0
0	1	1
1	0	1
1	1	0

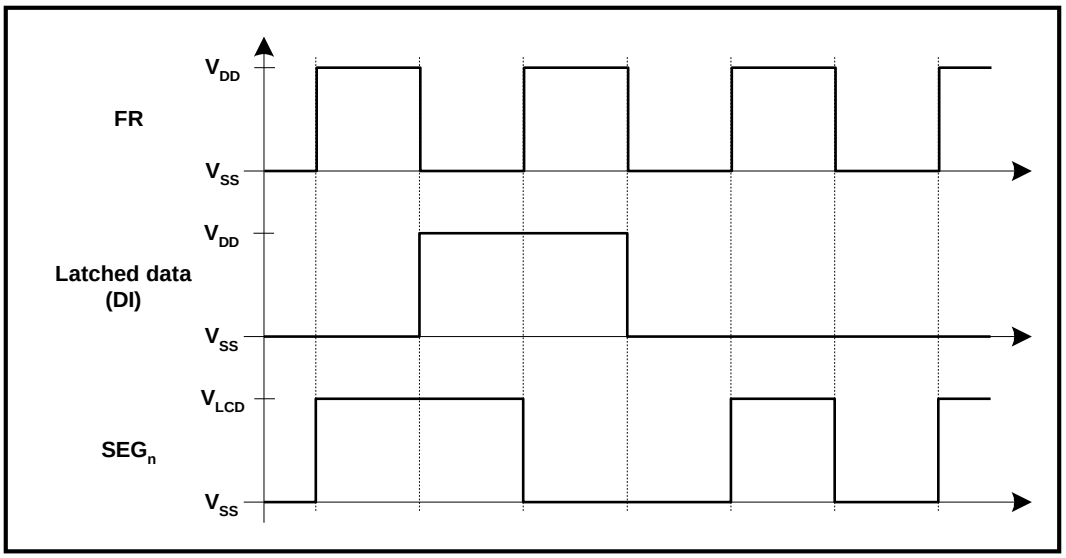


Figure 8

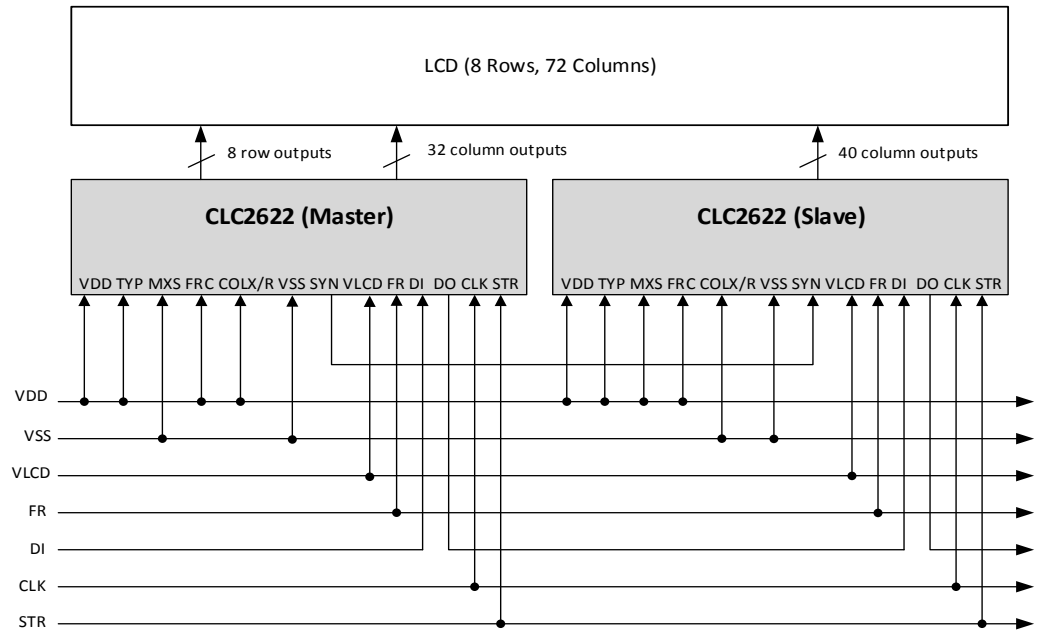


Figure 9 - Application Circuit with MUX8 Mode Configuration

7 PACKAGE OUTLINE

7.1 BUMPED DIE

Table 18 - Bonding Pad Dimensions

Die Size	X Y 3140 x 2980	µm
Pad pitch	150	µm
Pad size	100 x 100	µm
Bump height (gold)	16	µm
Die thickness	625 ± 25	µm

7.2 QFN56 PACKAGE

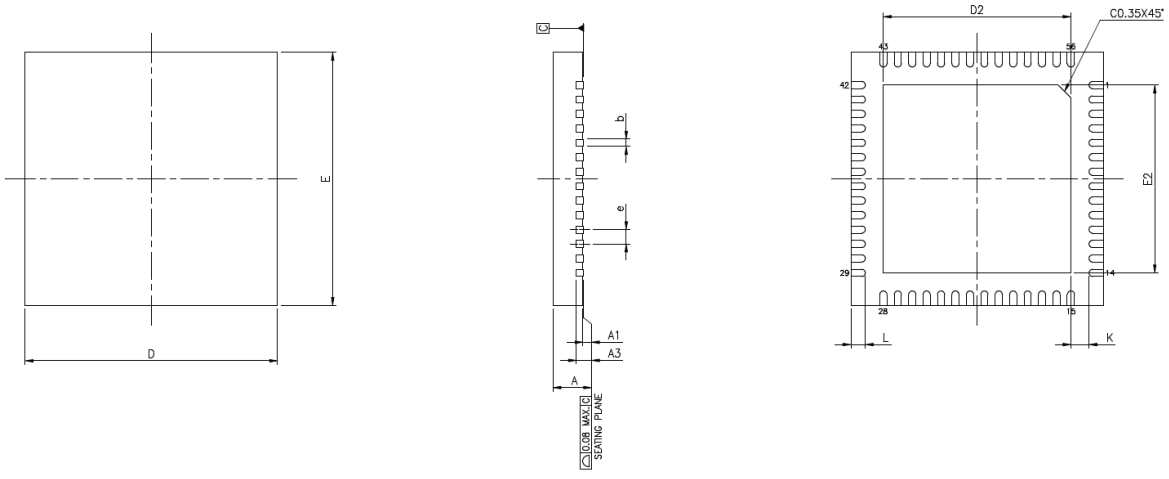


Figure 10 - QFN56 Package

Symbol	A	A1	A3	b	D	E	e	L	K	D2	E2
Min	0.50	0.00	0.150 REF.	0.15	7.00 BSC.	7.00 BSC.	0.40 BSC.	0.35	0.20	5.15	5.15
Typ	0.55	0.02		0.20				0.40	-	5.20	5.20
Max	0.60	0.05		0.25				0.45	-	5.25	5.25

UNIT : mm

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

8 TAPE AND REEL / WAFFLE PACK INFORMATION

8.1 WAFFLE PACK (BUMPED DIE)

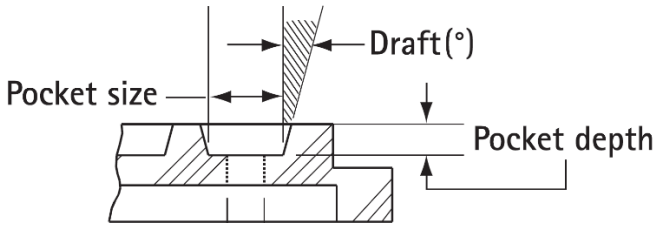


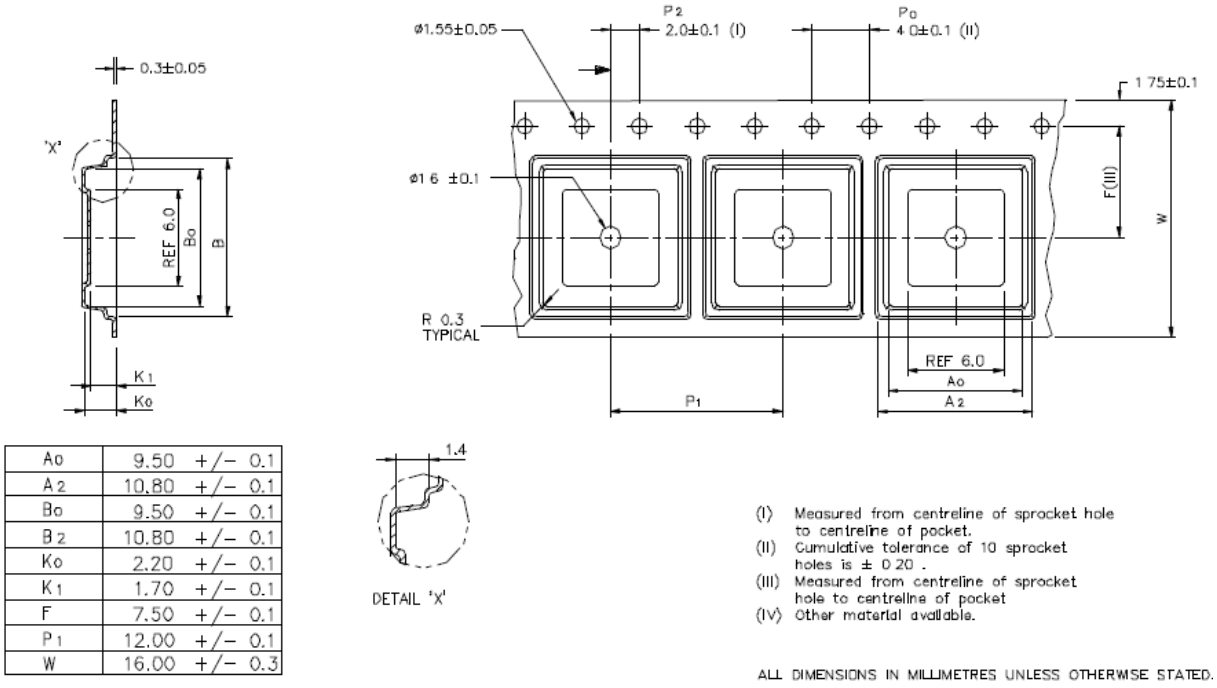
Figure 11 - Waffle Pack Cavity

Table 19 - Tray Sizes and Tolerances

Overall Size (sq.)	Overall Height	Flatness	Pocket Size	Pocket Depth	Pocket Draft	Capacity	Color
50.673 ±0.254 mm (1.995 ±0.010")	3.937 ±0.076 mm -0.127 mm (0.155 +0.003"/-0.005")	0.305 mm (0.012")	3.23 mm x 3.51 mm (0.127" x 0.138")	0.86 mm (0.034")	10°	100	black

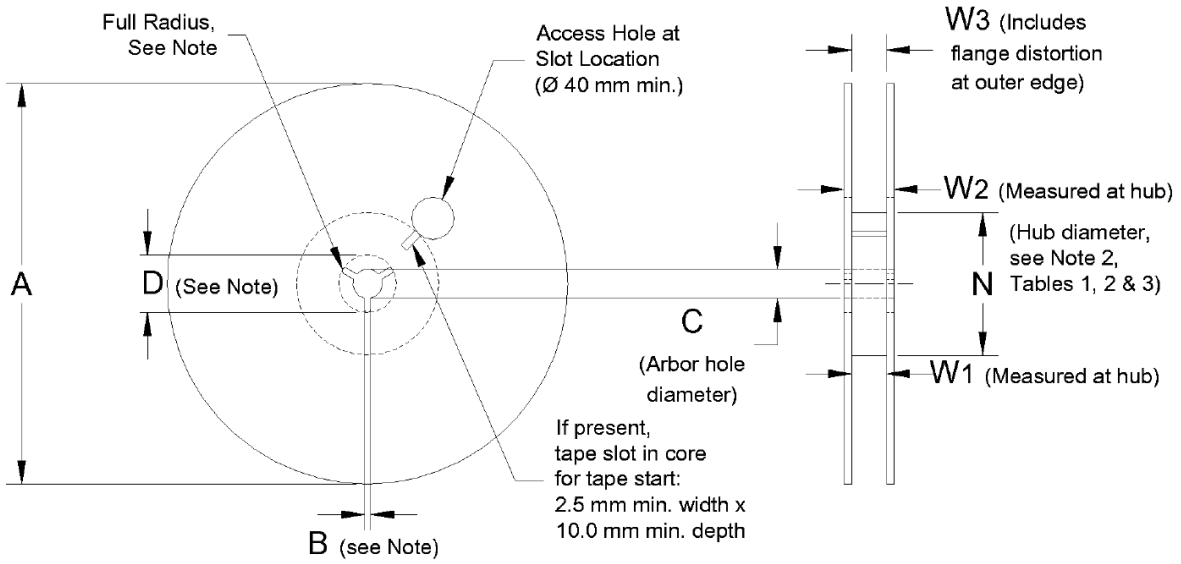
Die Orientation: Die ID "CLC2622" bottom left, beveled edge waffle pack top right

8.2 TAPE AND REEL QFN56 PACKAGE



Ao	9.50 +/− 0.1
A2	10.80 +/− 0.1
Bo	9.50 +/− 0.1
B2	10.80 +/− 0.1
Ko	2.20 +/− 0.1
K1	1.70 +/− 0.1
F	7.50 +/− 0.1
P1	12.00 +/− 0.1
W	16.00 +/− 0.3

Table 20 - Reel Information



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 21 - Reel Information

Symbol	A	B	C	D	W_1
Min	-	1.5	12.8	20.2	17.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	17.75

UNIT: mm

9 ORDERING INFORMATION

Table 22 - Ordering Information

Part	Order No.	Package	Delivery	Quantity
CLC2622	CLC2622_BD	Bumped Die	Waffle Pack	ca. 1.500 parts per tray
CLC2622	CLC2622_QFN56	QFN56 7 x 7 mm	Tape & Reel	5.000 parts per reel

10 REVISION HISTORY

Revision	Date	Author	Item
1.0	24.02.2016	Kw	New release

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