CCG6001 - 433 MHz ASK Receiver IC

1. FEATURES

- Superheterodyne ASK receiver
- LNA & Mixer
- Integrated LP filter and Dataslicer
- Integrated Bandgap reference voltage source
- Integrated PLL
- 0,6 µm BiCMOS process
- TSSOP24 (173mil) RoHS-conform

1. BLOCK DIAGRAM

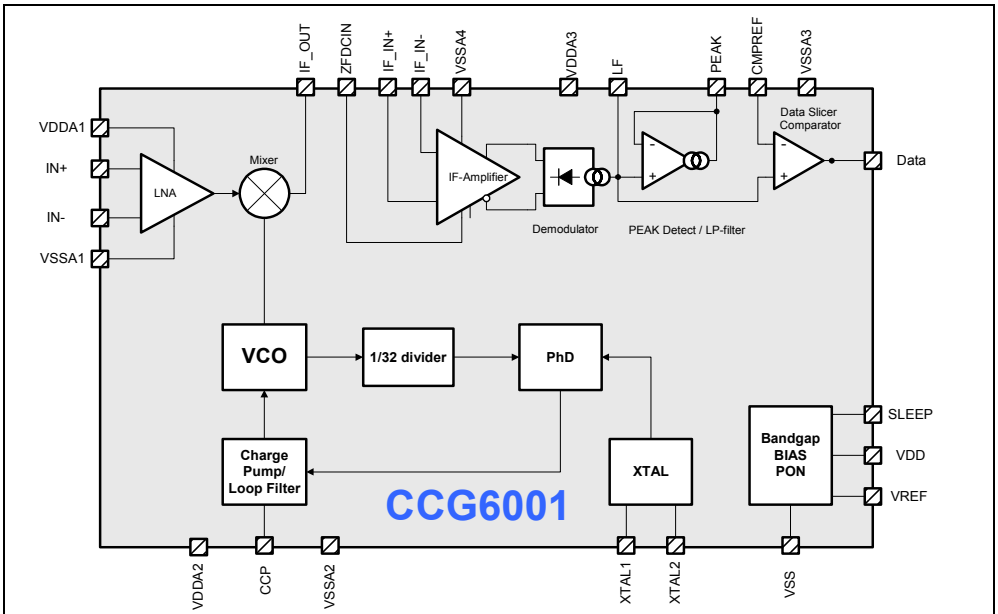


Figure1: CCG6001 block diagram

2. PINOUT:

Pin no.	name	Type	PAD cell	Function	Remarks
1	VDDA1	PWR	L	Analogue supply 1	Supply for LNA, Mixer
2	IN+	IN	A	RF input *	
3	IN-	IN	E	RF input	
4	VSSA1	PWR	M	Analogue ground 1	Supply for LNA, Mixer
5	IFOUT	OUT	E	IF output	
6	VSSA4	PWR	M	Analogue ground 4	Supply for IF-Amplifier
7	IFIN+	IN	E	IF amplifier input	
8	IFIN-	IN	E	IF amplifier input	
9	ZFDCIN	IN	L	DC amplifier input	
10	LF	OUT	B	Low frequency output	
11	VDDA3	PWR	L	Analogue supply 3	Supply Data Slicer, Filter
12	PEAK	OUT	B	Output data signal averager	
13	CMPREF	IN	B	Data slicer threshold input	
14	VSSA3	PWR	M	Analogue ground 3	Supply Data Slicer, Filter
15	DATA	OUT	G	Data output (raw data)	
16	SLEEP	IN	F	Standby mode control pin	
17	VREF	OUT	B	Reference voltage output	
18	VSSA2	PWR	M	Analogue ground 2	Supply for PLL
19	CCP	INOUT	E	PLL Charge pump out	
20	VDDA2	PWR	L	Analogue supply 2	Supply for PLL
21	VDD	PWR	L	Digital supply voltage	Supply for Logic, Reference BIAS
22	XTAL1	IN	E	Crystal oscillator1	
23	XTAL2	OUT	E	Crystal oscillator2	
24	VSS	PWR	M	Digital ground	Supply for Logic, Reference BIAS

*) All Pads consists ESD protection circuits except the input IN+

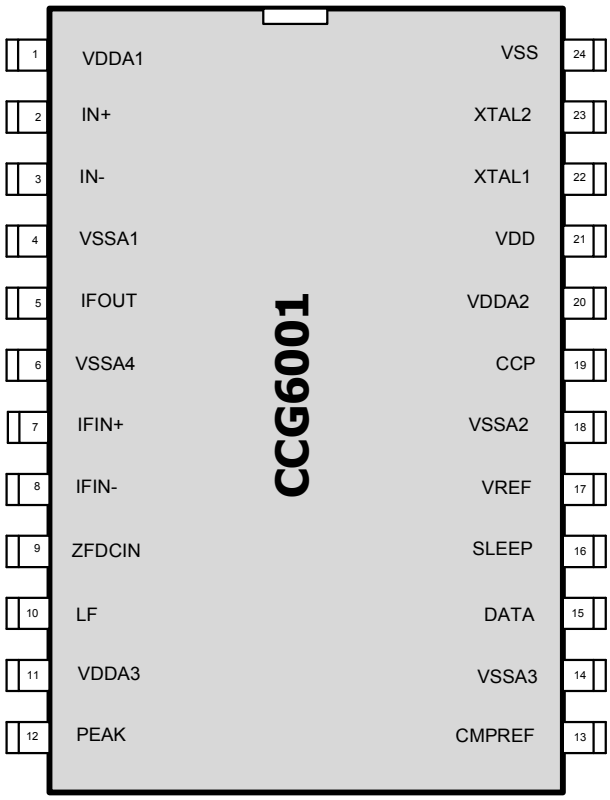


Figure 3: CCG6001 - Pin out

3.1 I/O PAD TYPES:

PAD cell	Description	Buffer name	Equivalent Circuit*
A	RF Input pin		a
B	Analogue PAD passive	BC06AI	b
D	Digital CMOS Input	BC06I	b
E	Analogue PAD	BC06OA	c
F	Digital CMOS Input with internal pull-up current source	BC06IPU	e
G	Digital CMOS Output, 2mA output current	BC06O2	d
L	Power Supply PAD (VDD)	BC06PP	f
M	Power Ground PAD (VSS)	BC06PG	f

*) Suitable for ESD consideration only – not detailed circuit schematic !

3.2 EQUIVALENT INPUT/OUTPUT CIRCUITS:

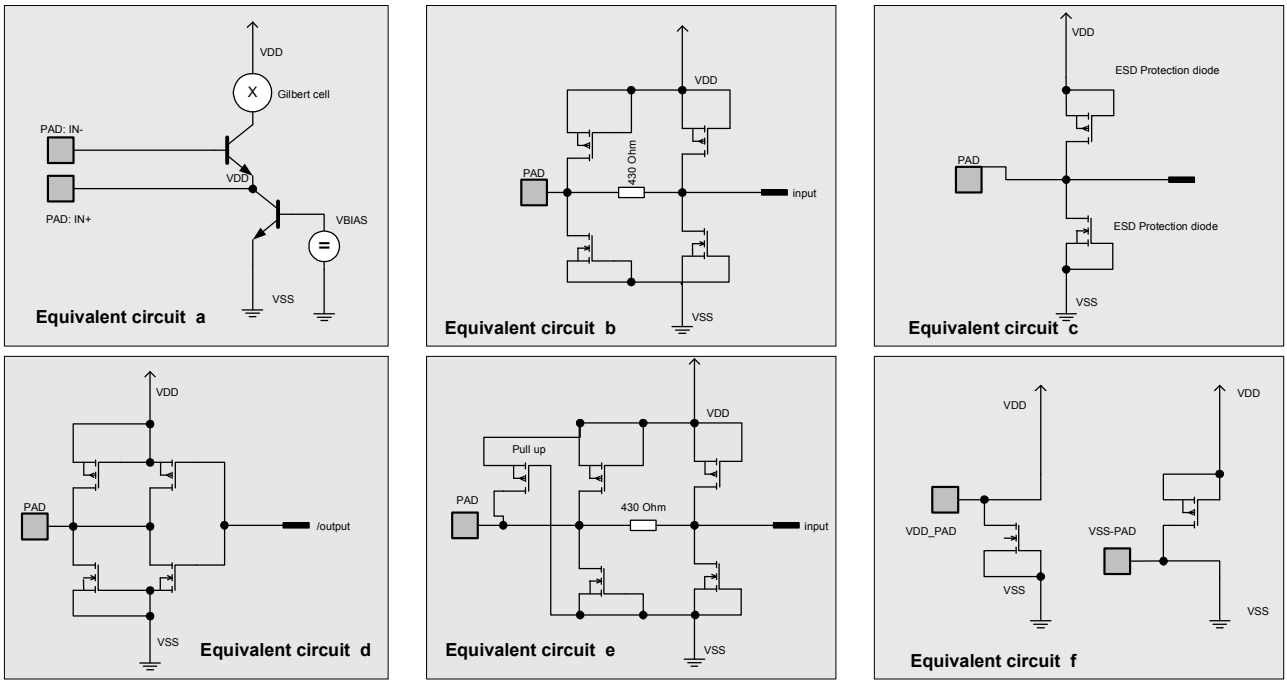


Figure 3: CCG6001 - Equivalent input circuits

4. ABSOLUTE MAXIMUM RATINGS:

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	$V_{DD} - V_{SS}$		-0,70	6,5	V
Total power dissipation	P_{TOT}	@ ϑ_{op} = 85 °C		600*[1]	mW
Operation temperature range	ϑ_{op}		-20	85	°C
Storage temperature range	$\vartheta_{storage}$		-55	150	°C
Soldering Profile	$t_{soldering}$	ϑ_{sol_max} = 260 °C		12	s
ESD Protection	V_{ESD}	Human Body model JEDEC JESD22 Method A114B Class2	2		kV
Permanent current into ESD-protection diodes	I_{DC_ESD}	Only in case of forward biased ESD diodes. Input voltage above VCC or below VSS !		2	mA
Reliability	**MTBF**	(VDD –VSS) < 5.5 V	10^5		h

*[1]) mounted on a multilayer PCB

5. ELECTRICAL CHARACTERISTICS:

Test conditions unless otherwise specified: 27 °C, $V_{DD} - V_{SS}$=5V, f_{XTAL} = 13,21 MHz
Electrical characteristics are valid for the whole specified temperature and supply voltage range

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
1. Power supply						
Supply voltage	$V_{DD} - V_{SS}$		4,5	5	6[*1]	V
Current Consumption	I_{DDMAX}	$V_{DD} - V_{SS}$ = 5,5V, with typical application circuit, no external load currents, under worst case conditions (Voltage & temperature range, L_{INMAX})		2.5	3	mA
Standby mode current consumption	$I_{DDsleep}$	No function except mode detection SLEEP Pin high or open			100	nA
2. LNA/Mixer						
Input impedance	Z_{in}	Real input impedance		50		Ω
Sensivity	S_{IN}	50 Ω input impedance 20 dB SNR @ LF out 100% ASK (OOK) with EPCOS front end filter	-95			dBm
Intercept point	IP3	50 Ω input	-10			dBm
Maximal input level	L_{INMAX}	@ ASIC input (pin2,3), I_{DDMAX} not guaranteed @ larger levels			-6	dBm
3. IF amplifier/Demodulator						
Input resistance	Z_{IFin}			330		Ω
-3 dB corner frequency of IF amplifier gain	f_{GHP}	high pass corner frequency	5		8	MHz
	f_{GLP}	Low pass corner frequency	12		16	MHz
IF filter			Ceramic filter: for instance SFECV10.7MA5S (Murata)			
If filter in/out impedance	$Z_{IFFin/out}$	No internal termination		330		Ω
Gain reduction	ΔS_{IN}	Pin grounded = min.gain		75		dB
	ΔS_{IN}	Pin = VCC/2 ± 0,5 V		40		dB
	ΔS_{IN}	Pin = VCC or open		0		dB
Pull up current @ HI_GAIN	I_{PULLUP}		30	60	120	µA
4. LP-Filter /Dataslicer						
Input impedance			1			MΩ
External capacitors		with 0603 or 0805 SMD parts			1	µF
Bandgap reference voltage			1,22	1,235	1,25	V
Datarate				1		kBaud
Pulse width			512	1024		µs
Group delay time					100	µs
5. PLL						
Multiplier factor	n			32		
Lock-in frequency	f_{lock}	$f_{lock} \approx 0.5 (f_{max}-f_{min})$		433		MHz
Lock-in frequency range	$\Delta f = f_{max}-f_{min}$		100			MHz
Startup/Lock in time	t_{lockin}				5	ms
Jitter	t_{jitter}	Referred to the reference clock (XTAL clock)			2	ns
External C	CCP				100	nF
6. Logic outputs						
Low output voltage	V_{OL}	I_{OUTL} = 2 mA Pin type G			VSS + 0.5	V
High output voltage	V_{OH}	I_{OUTH} = 2 mA, Pin type G	VDD – 0.5			V
Output leakage current	I_{OLEAK}	Pin types G	-5		5	µA
Output capacitance	C_{OUT_O}	Pin types G	3		10	pF

7. Logic inputs						
Low input voltage	V_{IL}		1.9	2	2.1	V
High input voltage	V_{IH}		2.85	3	3.15	V
Input leakage current	I_{ILEAK}		-5		5	µA
Input capacitance	C_{IN_IN}	Pin types F	3		10	pF

*1.) Supply voltage up to 6V is not covered by process spec. That will yield a to 89% reduced MTBF

8. APPLICATION CIRCUIT:

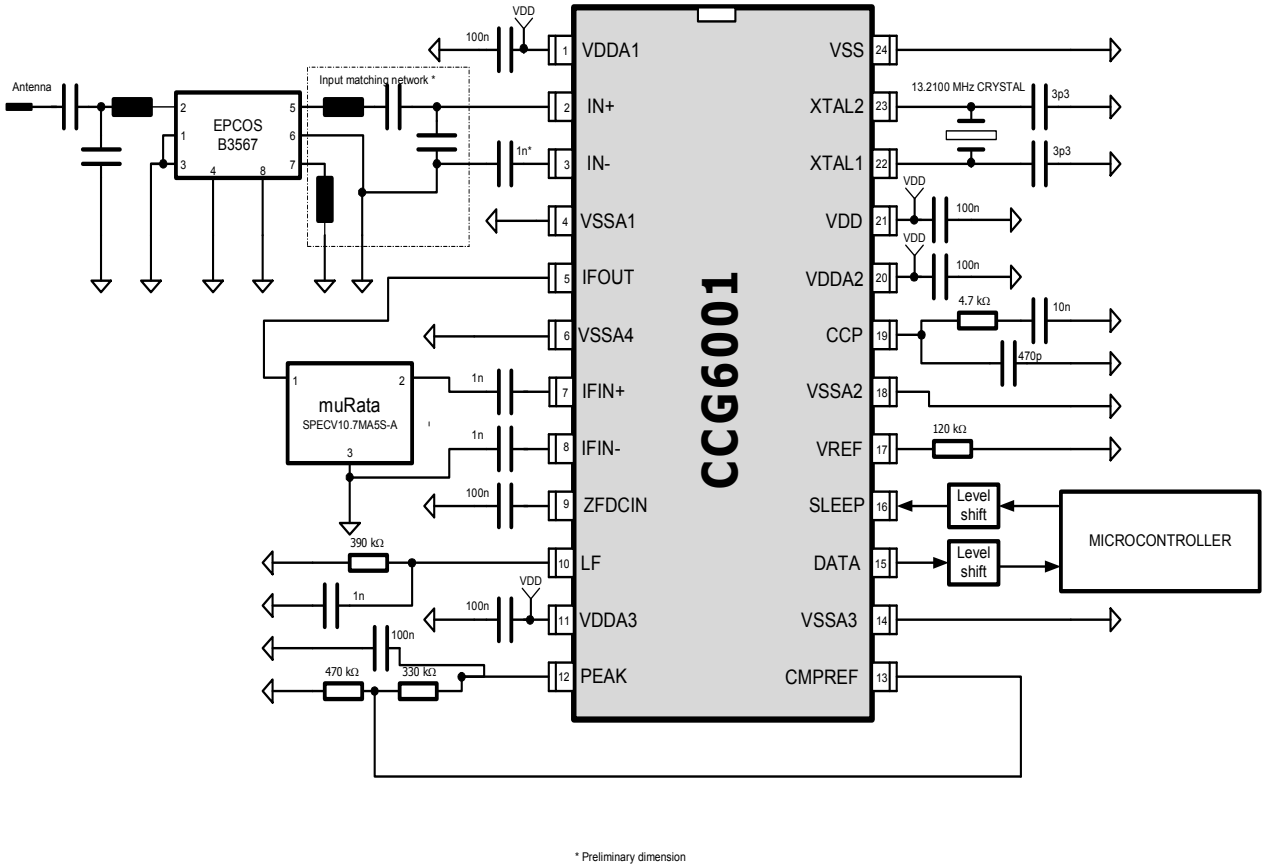
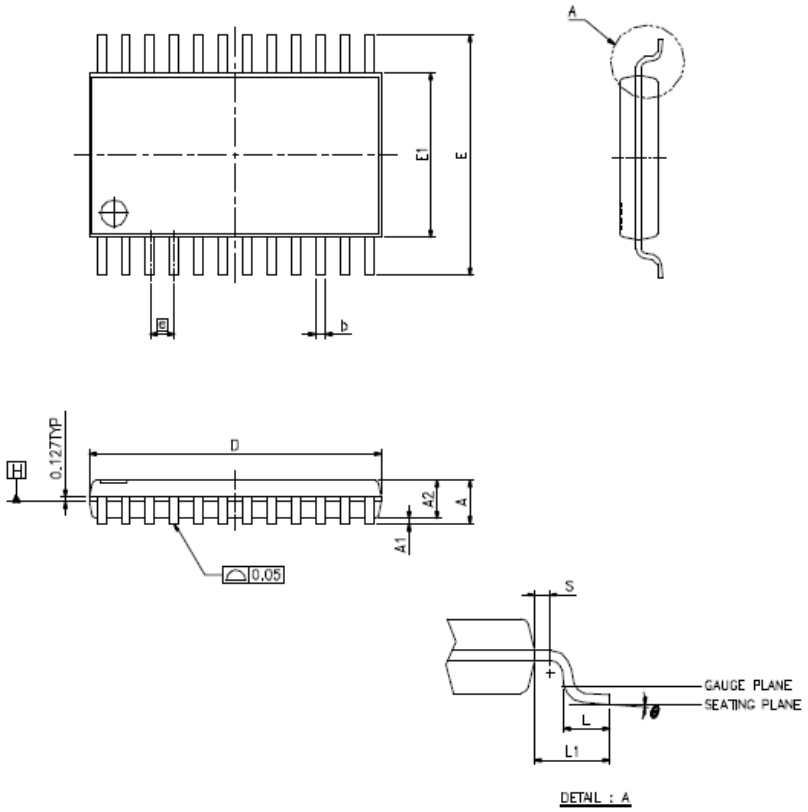


Figure 4: CCG6001 – Application circuit

9. PACKAGE OUTLINE DRAWING :

Chip PAD Layout according to Flip Chip mounting rules!



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. JEDEC OUTLINE : MO-153 AD
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION "D 22" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "D 22" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS "D" AND "E1" TO BE DETERMINED AT DATUM PLANE H .

Figure 5: CCG6000 – package outline drawing (according JEDEC MO-153)

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10. REVISION HISTORY

Revision	Date	Author	Item
1.1	08.02.2006	JSC, Ro	Block diagram, Electrical Spec.; Application circuit, package outline drawing